## Description

The PT7C4339D real-time clock is a low-power clock/calendar device with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I²C bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock supports either the 24-hour or 12-hour format with AM/PM indicator. The PT7C4339D has a built-in power-sensing circuit that detects power failures and automatically switches to the backup supply, maintaining time, date, and alarm operation.

## Features

- Real-Time Clock (RTC) Including Time (Seconds, Minutes and Hours) and Calendar (Day, Date, Month and Year with Leap-Year Compensation Valid Up to 2100) counter functions (BCD code)
- I²C Serial Interface supports I²C-Bus's high speed mode (400kHz)
- Programmable square wave output signal, defaults to 32 kHz on Power-up
- Two Time-of-Day Alarms
- Oscillator Stop Flag
- Automatic Power-Fail Detect and Switch Circuitry
- Temperature Range: -40°C to +85°C
- Supports max 100KΩ ESR 32.768KHz crystal
- Supports I2C bus time out
- Packaging (Pb-free & Green):
  - 8-pin, MSOP (U)
  - 8-pin, SOIC (W)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

**Table 1. Diverse Functions of RTC Circuits**

| Item | Function | | | PT7C4339D |
|---|---|---|---|---|
| 1 | Oscillator | Source | External crystal | External crystal |
| | | Oscillator enable/disable | | √ |
| | | Oscillator fail detect | | √ |
| 2 | Time | Time display | 12-hour | √ |
| | | | 24-hour | √ |
| | | Century bit | | √ |
| | | Time count chain enable/disable | | √ |
| 3 | Interrupt | Alarm interrupt output | | √2 |
| 4 | Programmable square wave output (Hz) | | | 1, 4.096k, 8.192k, 32.768k |
| 5 | Communication | | 2-wire I²C bus | √ |
| 6 | Power failure detect | | | √ |

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.


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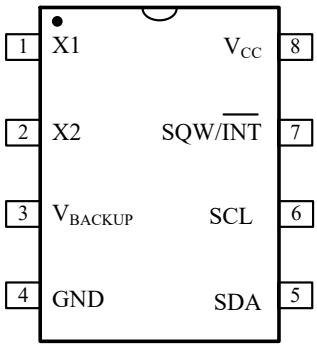
## Pin Configuration




SOIC-8
MSOP8

## Pin Description

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 1 | X1 | I | **Oscillator Circuit Input.** Together with X1, 32.768kHz crystal is connected between them. Or external clock input. |
| 2 | X2 | O | **Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them. When 32.768kHz external input, X2 must be float. |
| 6 | SCL | I | **Serial Clock Input.** SCL is used to synchronize data movement on the $I^2C$ serial interface. The pull up voltage may be up to 5.5V regardless of the voltage on $V_{CC}$. |
| 5 | SDA | I/O | **Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor. The pull up voltage may be up to 5.5V regardless of the voltage on $V_{CC}$. |
| 3 | $V_{BACKUP}$ | O | **Secondary Power Supply.** Supply voltage must be held between 1.3V and 3.7V for proper operation. This pin can be connected to a primary cell, such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used in conjunction with the trickle-charge feature. Due to internal LDO, backup battery charging voltage from VCC by internal trickle charger will be limited to max 3.0V. Diodes should not be placed in series between the backup source and the $V_{BACKUP}$ input, or improper operation will result. If a backup supply is not required, $V_{BACKUP}$ must be grounded. |
| 7 | SQW /INT | O | **Square-Wave/Interrupt Output.** Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pull up resistor. The pull up voltage may be up to 5.5V regardless of the voltage on $V_{CC}$. If not used, this pin may be left unconnected. |
| 8 | $V_{CC}$ | P | **Power.** When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected and $V_{CC}$ is below $V_{PF}$, reads and writes are inhibited. The timekeeping and alarm functions operate when the device is powered by $V_{CC}$ or $V_{BACKUP}$. |
| 4 | GND | P | **Ground.** |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## Maximum Ratings

| | |
|---|---|
| Storage Temperature | -55°C to +125°C |
| Junction Temperature | Max. 125°C |
| Supply Voltage to Ground Potential ($V_{CC}$ to GND) | -0.3V to +6.0V |
| DC Input (All Other Inputs except $V_{CC}$ & GND) | -0.3V to $V_{CC}$ +0.3V |
| DC Output Voltage (SDA, SQW /INT pins) | -0.3V to +6.0V |
| Power Dissipation | 320mW (depend on package) |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operating Conditions

| Symbol | Description | Min. | Type. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.0 | 3.3 | 5.5 | V |
| $V_{BACKUP}$ | Backup Supply Voltage | 1.3 | 3.0 | 3.7 | V |
| $V_{IH}$ | Input high level | $0.7V_{CC}$ | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Input low level | -0.3 | | $0.3V_{CC}$ | V |
| $V_{PF}$ | Power-Fail Voltage | 1.60 | 1.72 | 1.88 | V |
| $T_A$ | Operation Temperature | -40 | | 85 | °C |

## DC Electrical Characteristics

Unless otherwise specified, $V_{CC}$ = MIN to MAX, $V_{BACKUP}$ = MIN to MAX, $T_A$ = -40°C to +85°C

| Symbol | Item | Pin | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| ILI | Input Leakage | SCL | VIN = VCC or GND | -1 | | 1 | µA |
| ILO | I/O Leakage | SDA, SQW/INT | | -1 | | 1 | µA |
| IOL1 | Logic 0 Out VOL = 0.4V; VCC> VCCMIN | SQW/INT | | 1.0 | 3.0 | | mA |
| IOL2 | | SDA, | | 1.5 | 3.0 | | mA |
| IOL1 | Logic 0 Out VOL = 0.2V; VBACKUP ≥ VBACKMIN | SQW/INT | VCC absent, BBSQI = 1 | | 0.25 | | mA |
| ICCA | VCC Active Current | | (1) | | 80 | 250 | µA |
| ICCS | VCC Standby Current(2) | VCC = 3.3V | | | 40 | 100 | µA |
| | | VCC = 5.5V | | | | 150 | |
| R1 | Trickle-Charger Resistor Register10h = A5h, VCC = Typ, VBACKUP = 0 | | (3) | | 200 | | Ω |
| R2 | Trickle-Charger Resistor Register10h = A6h, VCC = Typ, VBACKUP = 0 | | | | 2000 | | Ω |
| R3 | Trickle-Charger Resistor Register10h = A7h, VCC = Typ, VBACKUP = 0 | | | | 4000 | | Ω |
| IBKLKG | VBACKUP Leakage Current | VBACKUP | | | 25 | 100 | nA |


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## DC Electrical Characteristics

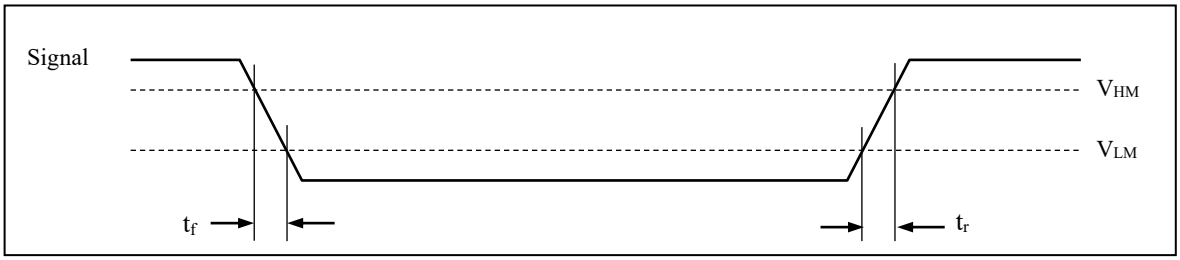
Unless otherwise specified, $V_{CC}$ = 0, $V_{BACKUP}$ = MIN to MAX, $T_A$ = -40°C to +85°C

| Symbol | Item | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{BKOSC}$ | $V_{BACKUP}$ Current, /EOSC = 0, SQW Off | (4, 5) | | 300 | 600 | nA |
| $I_{BKSQW}$ | $V_{BACKUP}$ Current, /EOSC = 0, SQW On | (4) | | 400 | 900 | nA |
| $I_{BKDR}$ | $V_{BACKUP}$ Current, /EOSC = 1 | (6) | | 10 | 100 | nA |

**Note:**
1. SCL clocking at max frequency = 400 kHz, $V_{IL}$ = 0.0V, $V_{IH}$ = VCC, trickle charger disabled.
2. Specified with 2-wire bus inactive, $V_{IL}$ = 0.0V, $V_{IH}$ = VCC, trickle charger disabled.
3. $V_{CC}$ must be less than 3.63V if 200Ω resistance is selected.
4. Using recommended crystal on X1 and X2.
5. Specified with the SQW function disabled by setting INTCN = 1.
6. Crystal oscillator is disabled.

## AC Electrical Characteristics

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $V_{HM}$ | Rising and falling threshold voltage high | 0.8 $V_{CC}$ | V |
| $V_{HL}$ | Rising and falling threshold voltage low | 0.2 $V_{CC}$ | V |




## Over the Operating Range

**(Figure 1)**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | | 400 | kHz |
| $t_{SU;STA}$ | START condition set-up time | 0.6 | | | µs |
| $t_{HD;STA}$ | START condition hold time | 0.6 | | | µs |
| $t_{SU;DAT}$ | Data set-up time (RTC read/write) | 200 | | | ns |
| $t_{HD;DAT1}$ | Data hold time (RTC write) | 35 | | | ns |
| $t_{HD;DAT2}$ | Data hold time (RTC read) | 0 | | | µs |
| $t_{SU;STO}$ | STOP condition setup time | 0.6 | | | µs |
| $t_{BUF}$ | Bus idle time between a START and STOP condition | 1.3 | | | µs |
| $t_{LOW}$ | When SCL = "L" | 1.3 | | | µs |
| $t_{HIGH}$ | When SCL = "H" | 0.6 | | | µs |
| $t_r$ | Rise time for SCL and SDA | | | 0.3 | µs |
| $t_f$ | Fall time for SCL and SDA | | | 0.3 | µs |
| $t_{SP}$* | Allowable spike time on bus | | | 50 | ns |
| $C_B$ | Capacitance load for each bus line | | | 400 | pF |
| $C_{I/O}$* | I/O Capacitance (SDA, SCL) | | | 10 | pF |
| $T_{OSF}$ | Oscillator Stop Flag (OSF) Delay | | | 100 | ms |

* **Note:** only reference for design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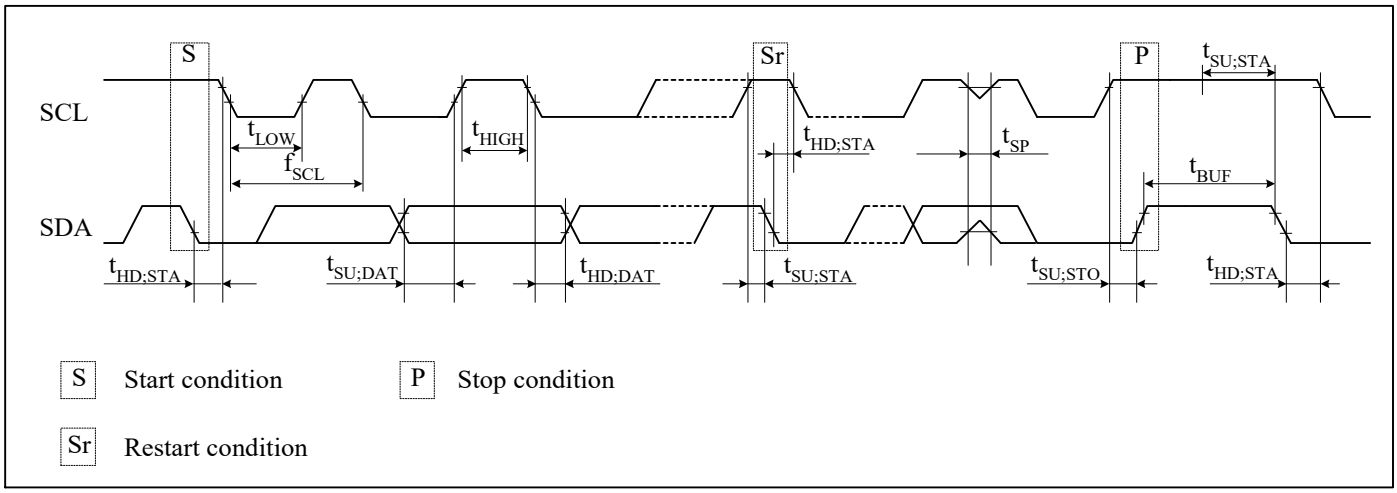


**Figure 1. I²C Timing**


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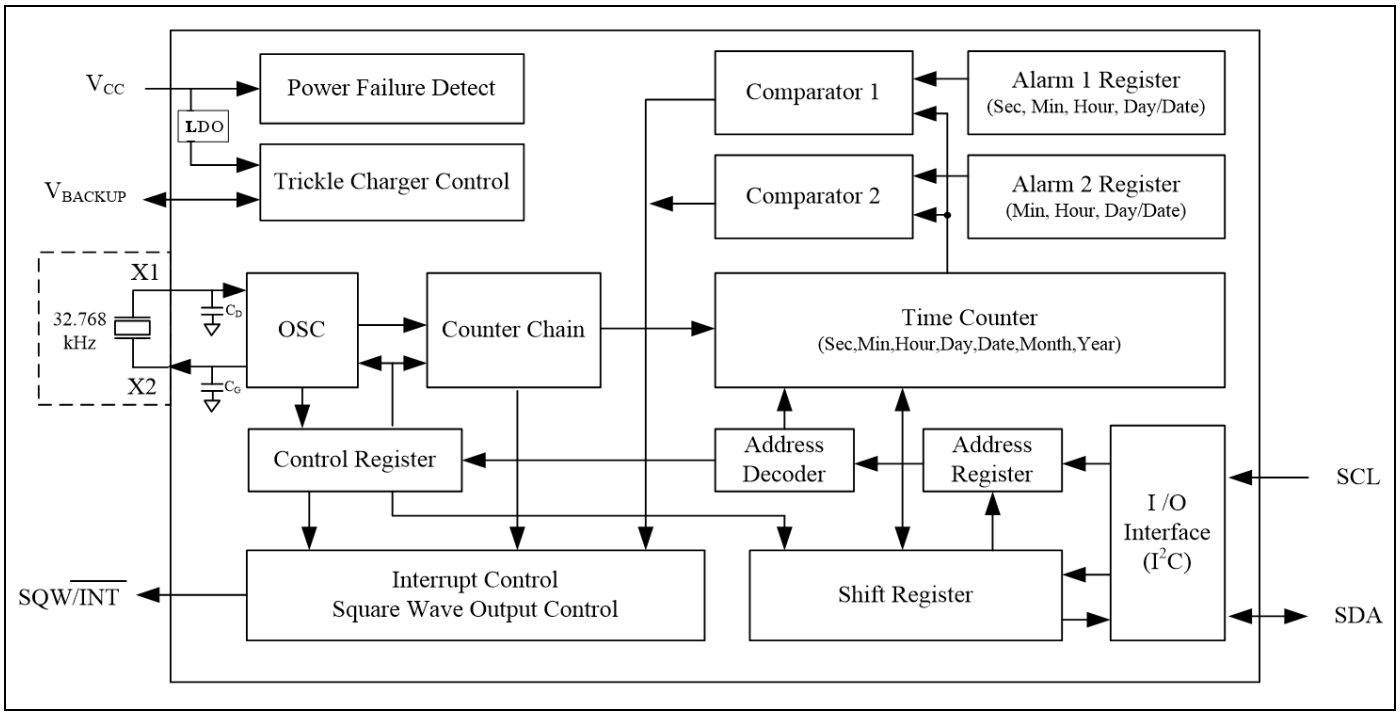
## Functional Block Diagram




## Oscillator Circuit

The PT7C4339D uses an external 32.768 kHz crystal. Table 3 specifies several crystal parameters for the external crystal. The *Block Diagram* shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

**Table 2. Built-in Capacitors Specifications and Recommended External Capacitors**

| Symbol | Parameter | | Typ. | Unit |
|---|---|---|---|---|
| $C_G$ | Build-in capacitors | X1 to GND | 10 | pF |
| $C_D$ | | X2 to GND | 10 | pF |
| $C_1$ | Recommended External capacitors | X1 to GND | 10 | pF |
| $C_2$ | | X2 to GND | 10 | pF |

**Note**: The frequency of crystal can be optimized by external capacitor $C_1$ and $C_2$, for frequency=32.768Hz, $C_1$ and $C_2$ should meet the equation as below:

$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] = C_L$

Cpar is all parasitical capacitor between X1 and X2.

$C_L$ is crystal's load capacitance.

**Table 3. Crystal Specifications**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_O$ | Nominal Frequency | | 32.768 | | kHz |
| ESR | Series Resistance | | | 100 | kΩ |
| $C_L$ | Load Capacitance | | 12.5 | | pF |

**Note:** The crystal, traces, and crystal input pins should be isolated from RF generating signals.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### Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 2 shows a typical PC board layout for isolating the crystal and oscillator from noise.

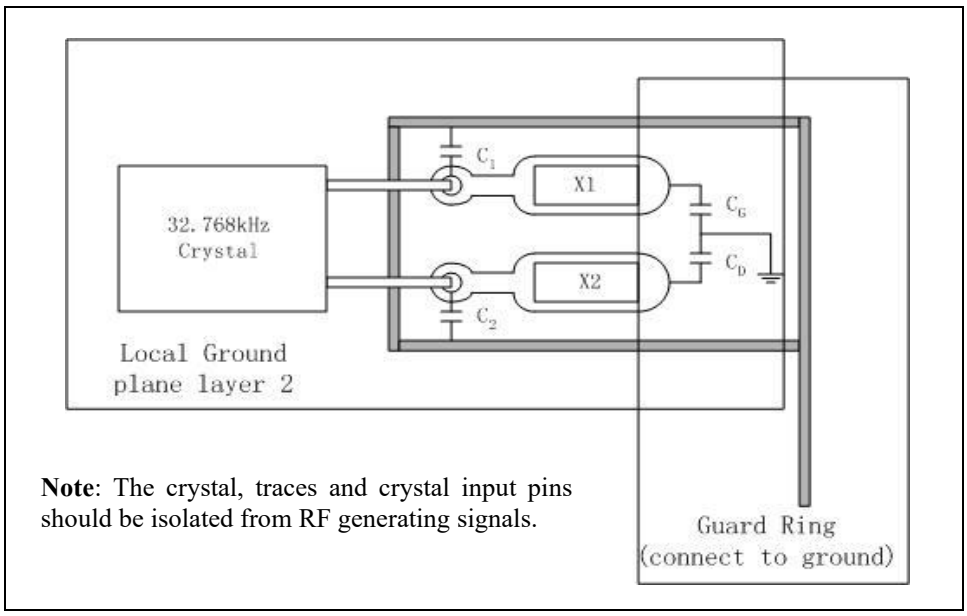


**Figure 2. Recommended Layout for Crystal**

## Functional Description

### Overview of Functions

#### Clock Function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.
For PT7C4339D on a power-on reset (POR), the time and date are set to 00:00:00 01/01/00 (hh:mm:ss DD/MM/YY) and the Day register is set to 01. Please note before reading time counter, user needs to set the date/time when the OSF bit is 1 first.

#### Alarm Function

This device has two alarm systems (Alarm 1 and Alarm 2) that outputs interrupt signals from SQW/INT to CPU when the date, day of the week, hour, minute or second correspond to the setting. Each of them may output interrupt signal separately at a specified time. The alarm is be selectable between on and off for matching alarm or repeating alarm.

#### Programmable Square Wave Output

A square wave output enable bit controls square wave output at pin 7. Frequencies are selectable: 1, 4.096k, 8.192k, 32.768 kHz.

#### Interface with CPU

Data is read and written via the I2C bus interface using two signal lines: SCL (clock) and SDA (data).
Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.
The SCL's maximum clock frequency is 400 kHz, which supports the I2C bus's high-speed mode.

#### Oscillator Fail Detect

When oscillator fail, PT7C4339D OSF bit will be set.


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### Oscillator Enable/Disable

Oscillator can be enabled or disabled at the same time by /EOSC bit.

## Operation

The PT7C4339D operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when $V_{CC}$ is greater than $V_{PF}$. However, when $V_{CC}$ falls below $V_{PF}$, the internal clock registers are blocked from any access. If $V_{PF}$ is less than $V_{BACKUP}$, the device power is switched from $V_{CC}$ to $V_{BACKUP}$ when $V_{CC}$ drops below $V_{PF}$. If $V_{PF}$ is greater than $V_{BACKUP}$, the device power is switched from $V_{CC}$ to $V_{BACKUP}$ when $V_{CC}$ drops below $V_{BACKUP}$. The registers are maintained from the $V_{BACKUP}$ source until $V_{CC}$ is returned to nominal levels.

## Power Control

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the $V_{CC}$ level. The device is fully accessible and data can be written and read when $V_{CC}$ is greater than $V_{PF}$. However, when $V_{CC}$ falls below $V_{PF}$, the internal clock registers are blocked from any access. If $V_{PF}$ is less than $V_{BACKUP}$, the device power is switched from $V_{CC}$ to $V_{BACKUP}$ when $V_{CC}$ drops below $V_{PF}$. If $V_{PF}$ is greater than $V_{BACKUP}$, the device power is switched from $V_{CC}$ to $V_{BACKUP}$ when $V_{CC}$ drops below $V_{BACKUP}$. The registers are maintained from the $V_{BACKUP}$ source until $V_{CC}$ is returned to nominal levels (Table 4). After $V_{CC}$ returns above $V_{PF}$, read and write access is allowed after $t_{REC}$ (Figure 1). On the first application of power to the device the time and date registers are reset to 01/01/00 01 00:00:00 (MM/DD/YY DOW HH:MM:SS).

**Table 4. Power Control Supply Condition**

| Power Control Supply Condition | Read/Write Access | Power by |
|---|---|---|
| $V_{CC} < V_{PF}$, $V_{CC} < V_{BACKUP}$ | No | $V_{BACKUP}$ |
| $V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$ | Yes | $V_{CC}$ |
| $V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$ | Yes | $V_{CC}$ |


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## Registers

### Allocation of Registers

| Addr. (hex) *1 | Function | Register Definition | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 00 | Seconds (00-59) | 0 | S40 | S20 | S10 | S8 | S4 | S2 | S1 |
| 01 | Minutes (00-59) | 0 | M40 | M20 | M10 | M8 | M4 | M2 | M1 |
| 02 | Hours (00-23 / 01-12) | 0 | 12, /24 | H20 or P, /A | H10 | H8 | H4 | H2 | H1 |
| 03 | Days of the week (01-07) | 0 | 0 | 0 | 0 | 0 | W4 | W2 | W1 |
| 04 | Dates (01-31) | 0 | 0 | D20 | D10 | D8 | D4 | D2 | D1 |
| 05 | Months (01-12) | Century | 0 | 0 | MO10 | MO8 | MO4 | MO2 | MO1 |
| 06 | Years (00-99) | Y80 | Y40 | Y20 | Y10 | Y8 | Y4 | Y2 | Y1 |
| 07 | Alarm 1: Seconds | A1M1*2 | S40 | S20 | S10 | S8 | S4 | S2 | S1 |
| 08 | Alarm 1: Minutes | A1M2*2 | M40 | M20 | M10 | M8 | M4 | M2 | M1 |
| 09 | Alarm 1: Hours | A1M3*2 | 12, /24 | H20 or P, /A | H10 | H8 | H4 | H2 | H1 |
| 0A | Alarm 1: Day, Date | A1M4*2 | Day, /Date | 0, D20 | 0, D10 | 0, D8 | W4, D4 | W2, D2 | W1, D1 |
| 0B | Alarm 2: Minutes | A2M2*3 | M40 | M20 | M10 | M8 | M4 | M2 | M1 |
| 0C | Alarm 2: Hours | A2M3*3 | 12, /24 | H20 or P, /A | H10 | H8 | H4 | H2 | H1 |
| 0D | Alarm 2: Day, Date | A2M4*3 | Day, /Date | 0, D20 | 0, D10 | 0, D8 | W4, D4 | W2, D2 | W1, D1 |
| 0E | Control | /EOSC*4 | 0 | BBSQI | RS2*5 | RS1*5 | INTCN*6 | A2IE*7 | A1IE*7 |
| 0F | Status | OSF*9 | 0 | 0 | 0 | 0 | 0 | A2F*8 | A1F*8 |
| 10 | Trickle charger | TCS3 | TCS2 | TCS1 | TCS0 | DS1 | DS0 | ROUT1 | ROUT0 |

**Caution points:**

*1. PT7C4339D uses 8 bits for address. For excess 10H address, PT7C4339D will not respond (no acknowledge signal was given).
*2. Alarm 1 mask bits. Select alarm repeated rate when an alarm occurs.
*3. Alarm 2 mask bits. Select alarm repeated rate when an alarm occurs.
*4. Oscillator enable/disable bit.
*5. Square wave output frequency select.
*6. Interrupt output pin select bit.
*7. Alarm 1 and alarm 2 enable bits.
*8. Alarm 1 and alarm 2 flag bits.
*9. Oscillators stop flag.
*10. All bits marked with "0" are read-only bits. Their value when read is always "0".


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## Control and Status Register

| Addr. (hex) | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0E | Control | /EOSC | 0 | BBSQI | RS2 | RS1 | INTCN | A2IE | A1IE |
| | (default) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0F | Status | OSF | 0 | 0 | 0 | 0 | 0 | A2F | A1F |
| | (default) | 1 | 0 | 0 | 0 | 0 | 0 | Undefined | Undefined |

**Oscillator Related Bits**

**/EOSC**

**Enable Oscillator Bit.**

| /EOSC | Data | Description | |
|---|---|---|---|
| Read / Write | 0 | Starts the oscillator. | Default |
| | 1 | The oscillator is stopped. | |

**BBSQI**

**Battery-Backed Square-Wave and Interrupt Enable Bit.**

| BBSQI | Data | Description |
|---|---|---|
| Read / Write | 0 | The SQW/INT pin goes high impedance when VCC falls below the power-fail trip point. Default |
| | 1 | Enables the square wave or interrupt output when VCC is absent and the PT7C4339D is being powered by the VBACKUP pin. |

**Square Wave Frequency Selection Bits**

**RS2, RS1**

Square wave Rate Select. These bits control the frequency of the square-wave output when the square wave has been enabled.

| RS2, RS1 | Data | SQW output freq. (Hz) |
|---|---|---|
| Read / Write | 00 | 1 |
| | 01 | 4.096k |
| | 10 | 8.192k |
| | 11 | 32.768k Default |

**OSF**

**Oscillator Stop Flag**

Logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on VCC is insufficient to support oscillation.
3) The /EOSC bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.


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**Interrupt Related Bits**

**INTCN**

Interrupt Output pin select bit. This bit controls the relationship between the two alarms and the interrupt output pins.

| INTCN | Data | Description |
|---|---|---|
| Read/write | 1 | A match between the timekeeping registers and the alarm 1 or alarm 2 registers activate the SQW/INT pin (provided that the alarm is enabled). |
| | 0 | In this configuration, a square wave is output on the SQW/INT pin. Default |

**A1IE**

Alarm 1 Interrupt Enable.

| A1IE | Data | Description |
|---|---|---|
| Read/write | 0 | The A1F bit does not initiate the SQW/INT signal. Default |
| | 1 | Permits the alarm 1 flag (A1F) bit in the status register to assert SQW/INT. |

**A1F**

Alarm 1 Flag.

| A1F | Data | Description |
|---|---|---|
| Read / Write | 0 | The time does not match the alarm 1 registers. Default |
| Read | 1 | A logic 1 in the Alarm 1 Flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/INT pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged. |

**A2IE**

Alarm 2 Interrupt Enable.

| A2IE | Data | Description |
|---|---|---|
| Read/write | 0 | The A2F bit does not initiate an interrupt signal. Default |
| | 1 | Permits the alarm 2 flag (A2F) bit in the status register to assert SQW/INT (when INTCN = 1). |

**A2F**

Alarm 2 Flag.

| A1F | Data | Description |
|---|---|---|
| Read / Write | 0 | The time does not match the alarm 2 registers. Default |
| Read | 1 | A logic 1 in the Alarm 2 Flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/INT pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged. |


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## Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
  - Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

| Addr. (hex) | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00 | Seconds | 0 | S40 | S20 | S10 | S8 | S4 | S2 | S1 |
| | (default) | 0 | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 01 | Minutes | 0 | M40 | M20 | M10 | M8 | M4 | M2 | M1 |
| | (default) | 0 | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 02 | Hours | 0 | 12, /24 | H20 or P,/A | H10 | H8 | H4 | H2 | H1 |
| | (default) | 0 | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |

**Note:** Any registered imaginary time should be replaced with correct time, otherwise it will cause the clock counter malfunction. Before reading time counter, user needs to set the date/time when the OSF bit is 1 first.

### 12, /24 bit

This bit is used to select between 12-hour clock system and 24-hour clock system.

| 12, /24 | Data | Description |
|---|---|---|
| Read / Write | 0 | 24-hour system |
| | 1 | 12-hour system |

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

| 12, /24 | Description | Hours Register |
|---|---|---|
| 0 | 24-hour time display | |
| 1 | 12-hour time display | |

| 24-hour clock | 12-hour clock | 24-hour clock | 12-hour clock |
|---|---|---|---|
| 00 | 52 ( AM 12 ) | 12 | 72 ( PM 12) |
| 01 | 41 ( AM 01 ) | 13 | 61 ( PM 01 ) |
| 02 | 42 ( AM 02 ) | 14 | 62 ( PM 02 ) |
| 03 | 43 ( AM 03 ) | 15 | 63 ( PM 03 ) |
| 04 | 44 ( AM 04 ) | 16 | 64 ( PM 04 ) |
| 05 | 45 ( AM 05 ) | 17 | 65 ( PM 05 ) |
| 06 | 46 ( AM 06 ) | 18 | 66 ( PM 06 ) |
| 07 | 47 ( AM 07 ) | 19 | 67 ( PM 07 ) |
| 08 | 48 ( AM 08 ) | 20 | 68 ( PM 08 ) |
| 09 | 49 ( AM 09 ) | 21 | 69 ( PM 09 ) |
| 10 | 50 ( AM 10 ) | 22 | 70 ( PM 10 ) |
| 11 | 51 ( AM 11 ) | 23 | 71 ( PM 11 ) |

* Be sure to select between 12-hour and 24-hour clock operation before writing the time data.


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### Days of the Week Counter

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

| Addr. (hex) | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 03 | Days of the week | 0 | 0 | 0 | 0 | 0 | W4 | W2 | W1 |
| | (default) | 0 | 0 | 0 | 0 | 0 | Undefined | Undefined | Undefined |

### Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  - Range from 1 to 30 (for April, June, September and November).
  - Range from 1 to 29 (for February in leap years).
  - Range from 1 to 28 (for February in ordinary years).
  - Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

| Addr. (hex) | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 04 | Dates | 0 | 0 | D20 | D10 | D8 | D4 | D2 | D1 |
| | (default) | 0 | 0 | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 05 | Months | Century*1 | 0 | 0 | M10 | M8 | M4 | M2 | M1 |
| | (default) | Undefined | 0 | 0 | Undefined | Undefined | Undefined | Undefined | Undefined |
| 06 | Years | Y80 | Y40 | Y20 | Y10 | Y8 | Y4 | Y2 | Y1 |
| | (default) | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |

***1:** The century bit is toggled when the years register overflows from 99 to 00.

### Alarm Register

#### Alarm 1, Alarm 2 Register

| Addr. | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 07 | Alarm 1: Seconds | A1M1*1 | S40 | S20 | S10 | S8 | S4 | S2 | S1 |
| | (default) | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 08 | Alarm 1: Minutes | A1M2*1 | M40 | M20 | M10 | M8 | M4 | M2 | M1 |
| | (default) | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 09 | Alarm 1: Hours | A1M3*1 | 12, /24 | H20 or P,/A | H10 | H8 | H4 | H2 | H1 |
| | (default) | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 0A | Alarm 1: Day, Date | A1M4*1 | Day, /Date*1 | 0, D20 | 0, D10 | 0, D8 | W4, D4 | W2, D2 | W1, D1 |
| | (default) | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 0B | Alarm 2: Minutes | A2M2*2 | M40 | M20 | M10 | M8 | M4 | M2 | M1 |
| | (default) | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 0C | Alarm 2: Hours | A2M3*2 | 12, /24 | H20 or P,/A | H10 | H8 | H4 | H2 | H1 |
| | (default) | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 0D | Alarm 2: Day, Date | A2M4*2 | Day, /Date*2 | 0, D20 | 0, D10 | 0, D8 | W4, D4 | W2, D2 | W1, D1 |
| | (default) | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |

***1** Note: Alarm mask bit, using to select Alarm 1 alarm rate.

***2** Note: Alarm mask bit, using to select Alarm 2 alarm rate.


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## Alarm Function

**Related Register**

| Addr. (hex) | Function | Register Definition | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 00 | Seconds | 0 | S40 | S20 | S10 | S8 | S4 | S2 | S1 |
| 01 | Minutes | 0 | M40 | M20 | M10 | M8 | M4 | M2 | M1 |
| 02 | Hours | 0 | 12, /24 | H20 or A, /P | H10 | H8 | H4 | H2 | H1 |
| 03 | Days of the week | 0 | 0 | 0 | 0 | 0 | W4 | W2 | W1 |
| 04 | Dates | 0 | 0 | D20 | D10 | D8 | D4 | D2 | D1 |
| 07 | Alarm 1: Seconds | A1M1 | S40 | S20 | S10 | S8 | S4 | S2 | S1 |
| 08 | Alarm 1: Minutes | A1M2 | M40 | M20 | M10 | M8 | M4 | M2 | M1 |
| 09 | Alarm 1: Hours | A1M3 | 12, /24 | H20 or A, /P | H10 | H8 | H4 | H2 | H1 |
| 0A | Alarm 1: Day, Date | A1M4 | Day, /Date | 0, D20 | 0, D10 | 0, D8 | W4, D4 | W2, D2 | W1, D1 |
| 0B | Alarm 2: Minutes | A2M2 | M40 | M20 | M10 | M8 | M4 | M2 | M1 |
| 0C | Alarm 2: Hours | A2M3 | 12, /24 | H20 or A, /P | H10 | H8 | H4 | H2 | H1 |
| 0D | Alarm 2: Day, Date | A2M4 | Day, /Date | 0, D20 | 0, D10 | 0, D8 | W4, D4 | W2, D2 | W1, D1 |
| 0E | Control | /EOSC | 0 | BBSQI | RS2 | RS1 | INTCN | A2IE | A1IE |
| 0F | Status | OSF | 0 | 0 | 0 | 0 | 0 | A2F | A1F |

**Note:** Alarm function does not support different hour system adopted in time and alarm register.

The PT7C4339D contains two time-of-day/date alarms. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes - each alarm can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits.
When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h ~ 04h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 5 and Table 6 show the possible settings.

The Day, /Date bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 ~ 5 of that register reflects the day of the week or the date of the month. If the bit is written to logic 0, the alarm is the result of a match with date of the month. If the bit is written to logic 1, the alarm is the result of a match with day of the week.

When the PT7C4339D register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output (SQW/INT) signals. The match is tested on the once-per-second update of the time and date registers.

**Table 5. Alarm 1 Mask Bits**

| Day, /Date | Alarm 1 Register Mask Bits | | | | Alarm Rate |
|---|---|---|---|---|---|
| | A1M4 | A1M3 | A1M2 | A1M1 | |
| × | 1 | 1 | 1 | 1 | Alarm once per second |
| × | 1 | 1 | 1 | 0 | Alarm when seconds match |
| × | 1 | 1 | 0 | 0 | Alarm when minutes and seconds match |
| × | 1 | 0 | 0 | 0 | Alarm when hours, minutes, and seconds match |
| 0 | 0 | 0 | 0 | 0 | Alarm when date, hours, minutes, and seconds match |
| 1 | 0 | 0 | 0 | 0 | Alarm when day, hours, minutes, and seconds match |
| Others | | | | | Ignored. |


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**Table 6. Alarm 2 Mask Bits**

| Day, /Date | Alarm 2 Register Mask Bits | | | Alarm Rate |
|---|---|---|---|---|
| | A2M4 | A2M3 | A2M2 | |
| × | 1 | 1 | 1 | Alarm once per minute (00 seconds of every minute) |
| × | 1 | 1 | 0 | Alarm when minutes match |
| × | 1 | 0 | 0 | Alarm when hours, minutes |
| 0 | 0 | 0 | 0 | Alarm when date, hours, and minutes match |
| 1 | 0 | 0 | 0 | Alarm when day, hours, and minutes match |
| Others | | | | Ignored. |

## Trickle Charger Register (10h)

The simplified schematic in Figure 3 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode-select (DS) bits (bits 2 and 3) select whether or not a diode is connected between VCC and VBACKUP. The ROUT bits (bits 0 and 1) select the value of the resistor connected between VCC and VBACKUP. Table 7 shows the bit values.

**Table 7. Trickle Charger Register (10h)**

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | Function |
|---|---|---|---|---|---|---|---|---|
| TCS3 | TCS2 | TCS1 | TCS0 | DS1 | DS0 | ROUT1 | ROUT0 | |
| X | X | X | X | 0 | 0 | X | X | Disabled |
| X | X | X | X | 1 | 1 | X | X | Disabled |
| X | X | X | X | X | X | 0 | 0 | Disabled |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | No diode, 200Ω resistor |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | One diode, 200Ω resistor |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | No diode, 2kΩ resistor |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | One diode, 2kΩ resistor |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | No diode, 4kΩ resistor |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | One diode, 4kΩ resistor |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Initial power-up values |

**Warning: The ROUT value of 200Ω must not be selected whenever $V_{CC}$ is greater than 3.63V.**

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a 3.3V system power supply is applied to VCC and a super cap is connected to VBACKUP. Also assume that the trickle charger has been enabled with a diode and resistor R2 between VCC and VBACKUP. The maximum current IMAX would therefore be calculated as follows:

IMAX = (3.3V - diode drop) / R2 ≈ (3.3V - 0.7V) / 2kΩ ≈ 1.3mA

As the super cap or battery charges, the voltage drop between VCC and VBACKUP decreases and therefore the charge current decreases.


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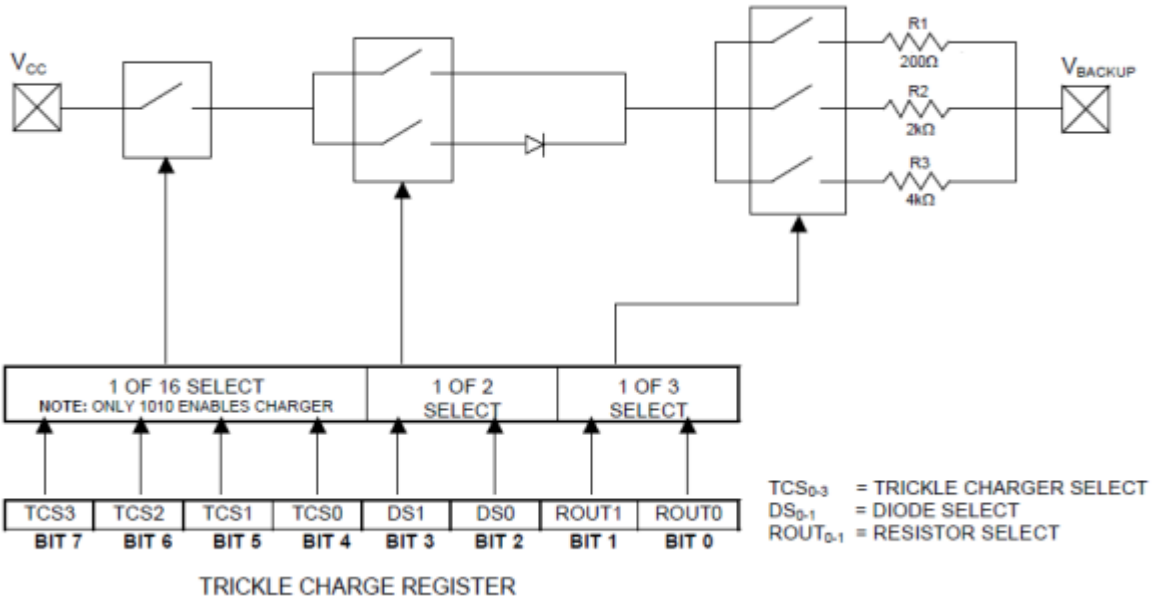


**Figure 3. Programmable Trickle Charger**

## I²C Bus Interface

### Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

### System Configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the VCC line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).


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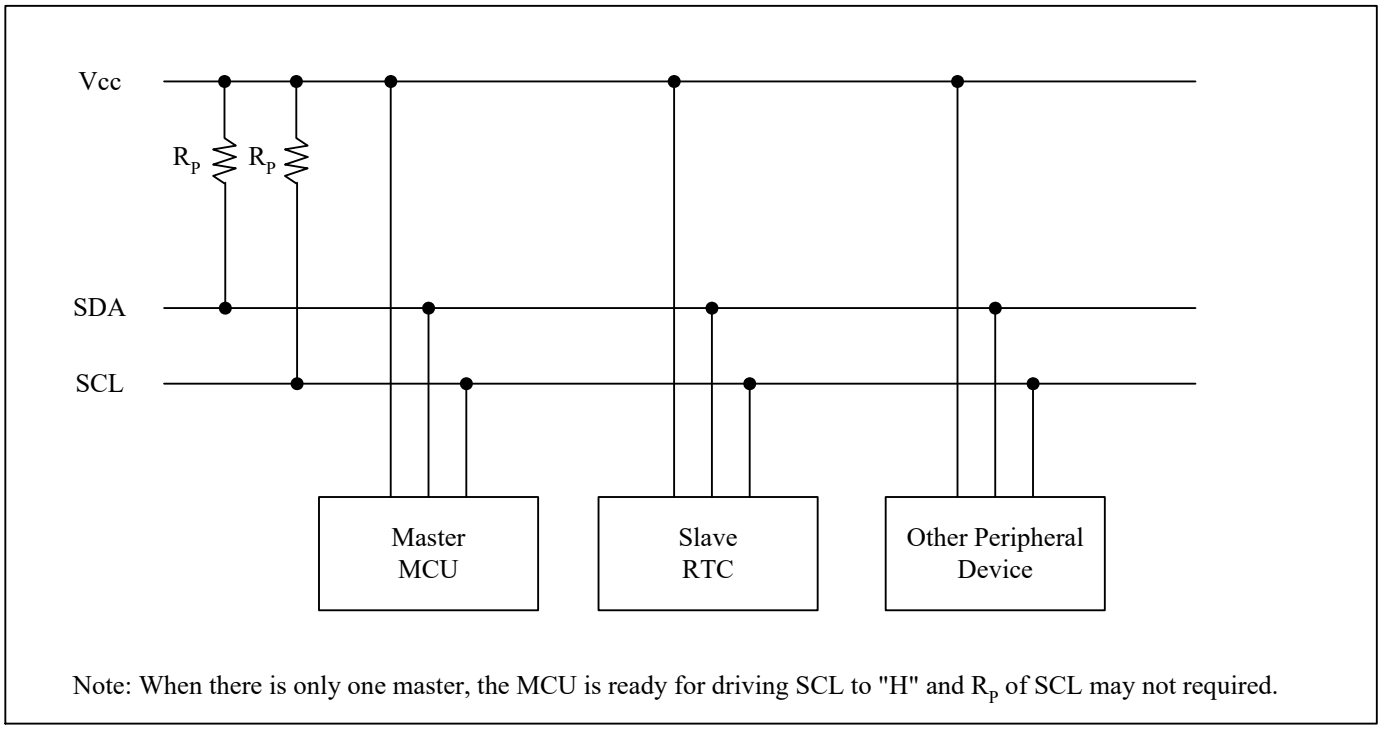


Note: When there is only one master, the MCU is ready for driving SCL to "H" and $R_P$ of SCL may not required.

**Figure 4. System Configuration**

## Starting and Stopping I2C Bus Communications

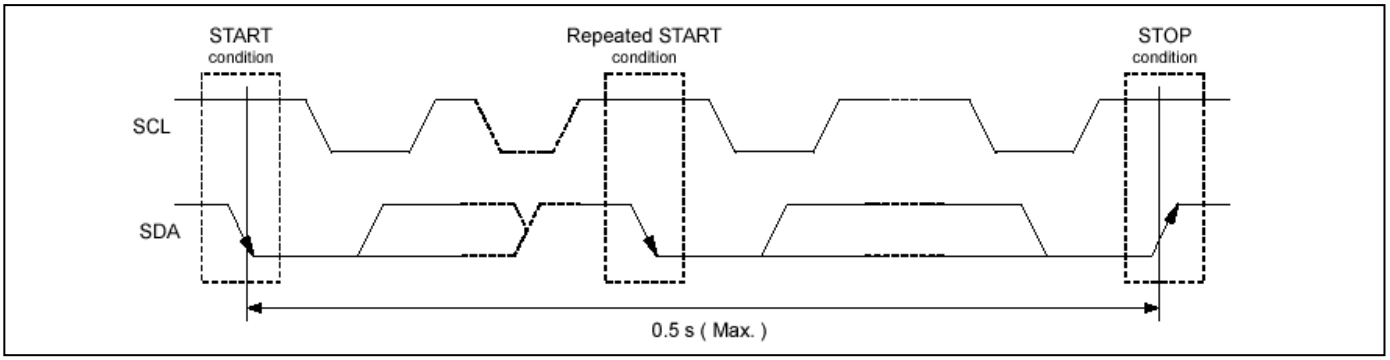


**Figure 5. Starting and Stopping on $I^2C$ bus**

### 1) START Condition, Repeated START Condition, and STOP Condition

**a) START Condition**

SDA level changes from high to low while SCL is at high level

**b) STOP Condition**

SDA level changes from low to high while SCL is at high level

**c) Repeated START Condition (RESTART Condition)**

In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.


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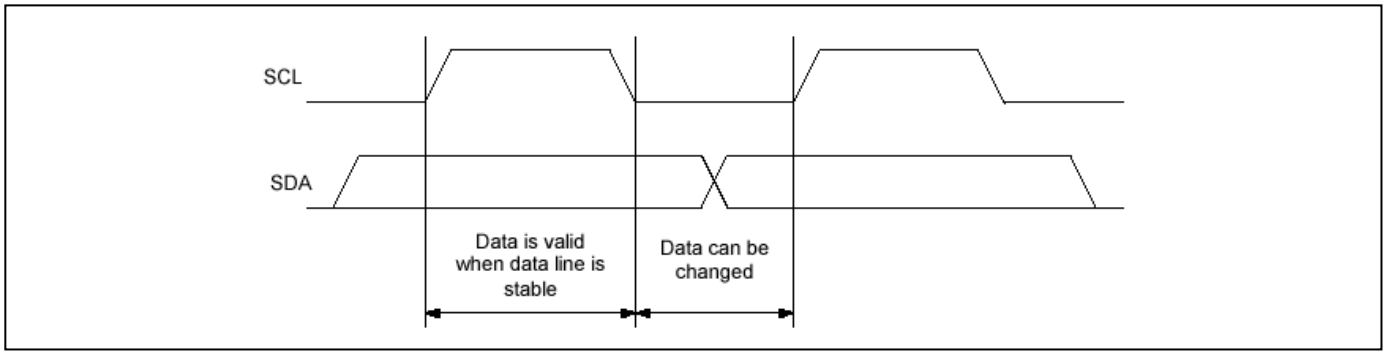
### 2) Data Transfers and Acknowledge Responses during I²C-BUS Communication

#### a) Data Transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
The address auto increment function operates during both write and read operations.
Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.
The receiver (receiving side) captures data while the SCL line is at high level.

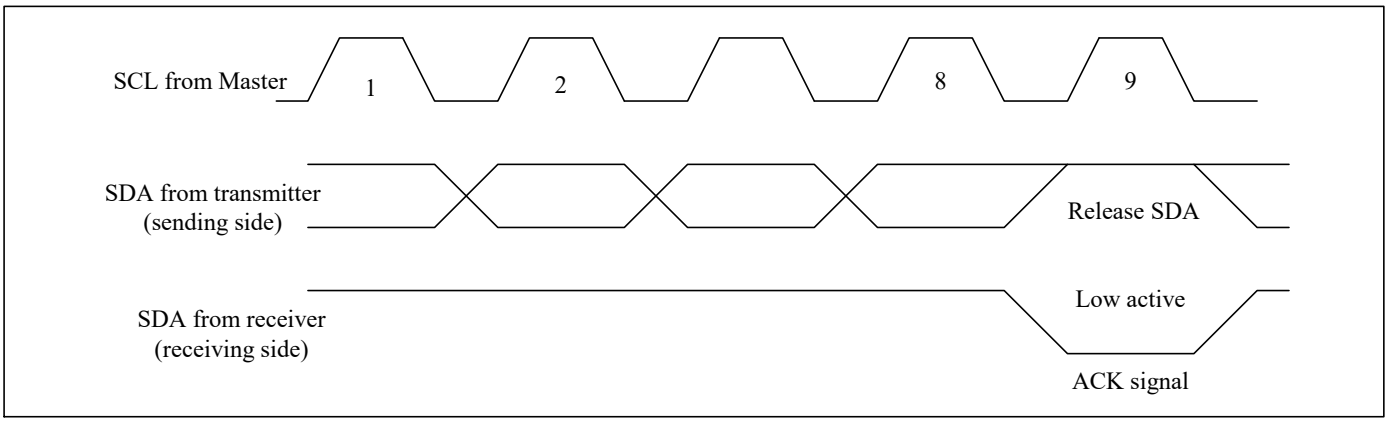



***Note:** with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

#### b) Data Acknowledge Response (ACK Signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.




After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.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## Slave Address

The I2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.

All communications begin with transmitting the [START condition] + [slave address (+ R/$\overline{W}$ specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

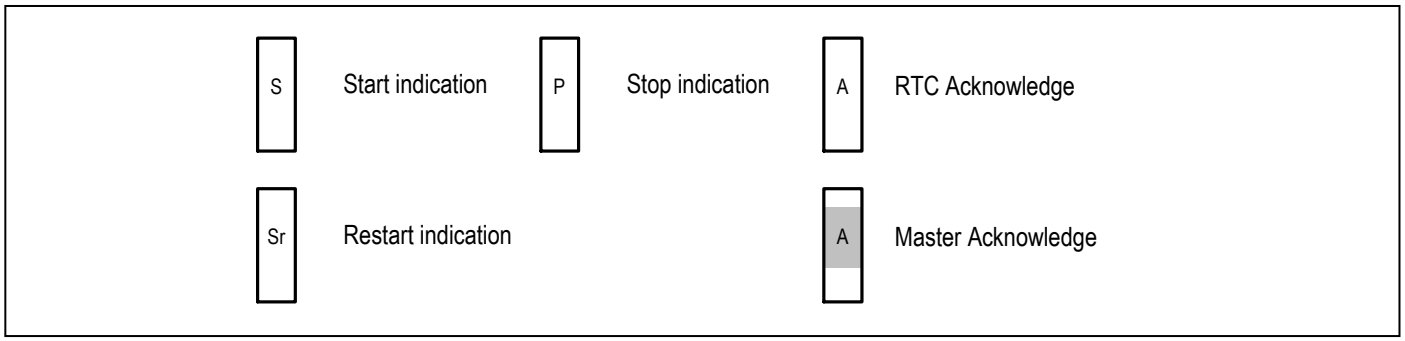
Slave addresses have a fixed length of 7 bits. See table for the details.

An R/$\overline{W}$ bit is added to each 7-bit slave address during 8-bit transfers.

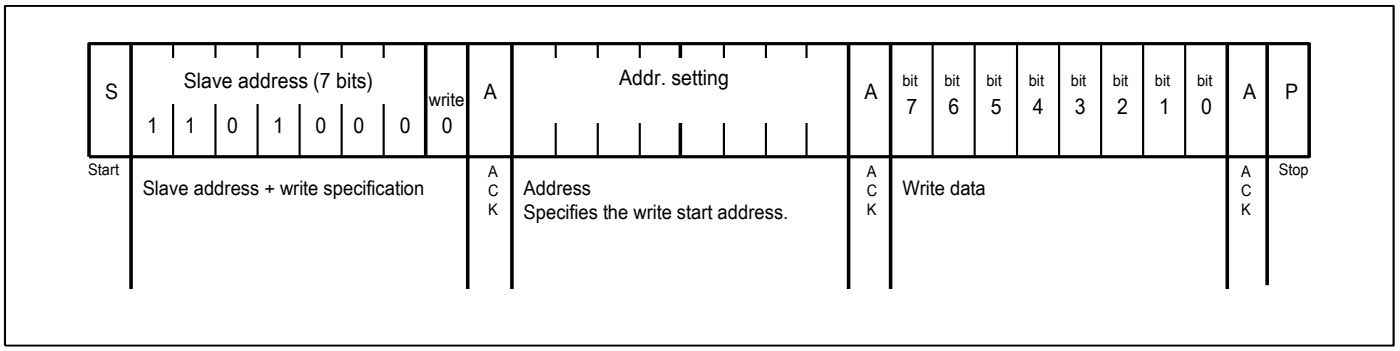
**Table 8. Slave Address**

| Operation | Transfer Data | Slave Address | | | | | | | R/W Bit |
|---|---|---|---|---|---|---|---|---|---|
| | | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| Read | D1 h | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 (= Read) |
| Write | D0 h | | | | | | | | 0 (= Write) |

## I²C Bus's Basic Transfer Format




### 1) Write via I²C Bus





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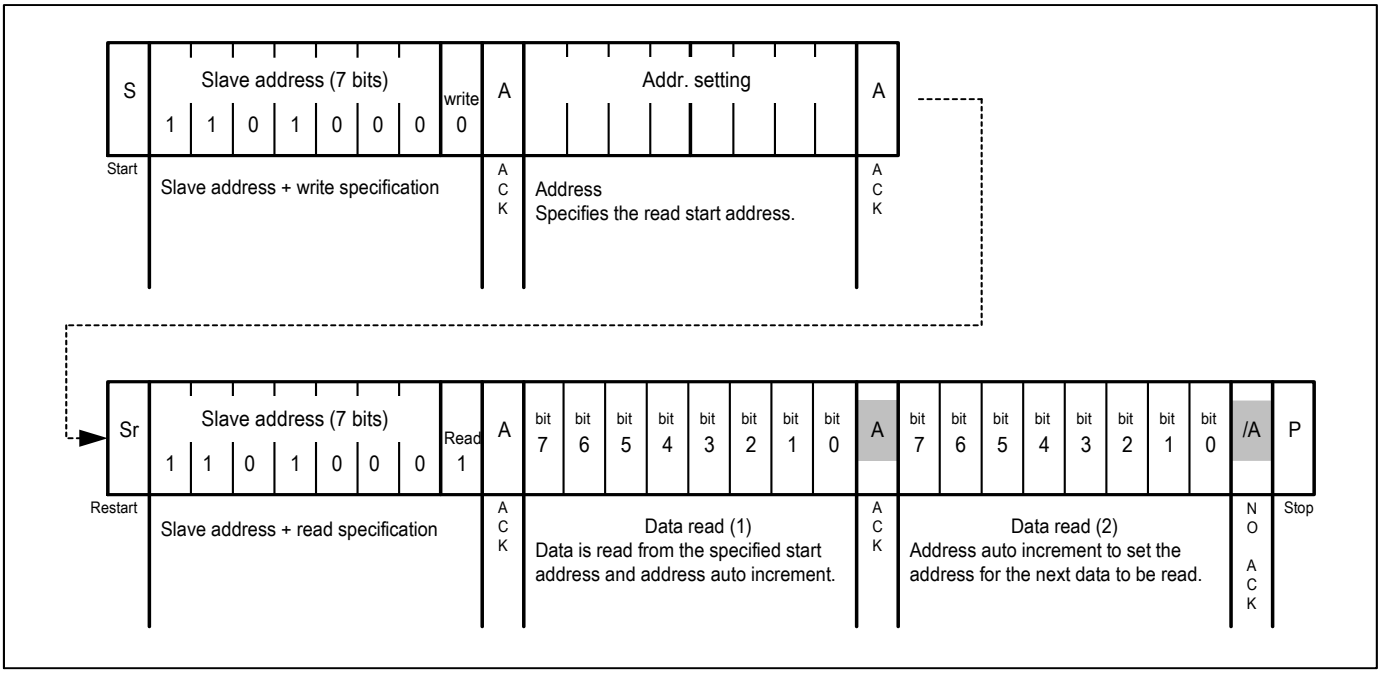
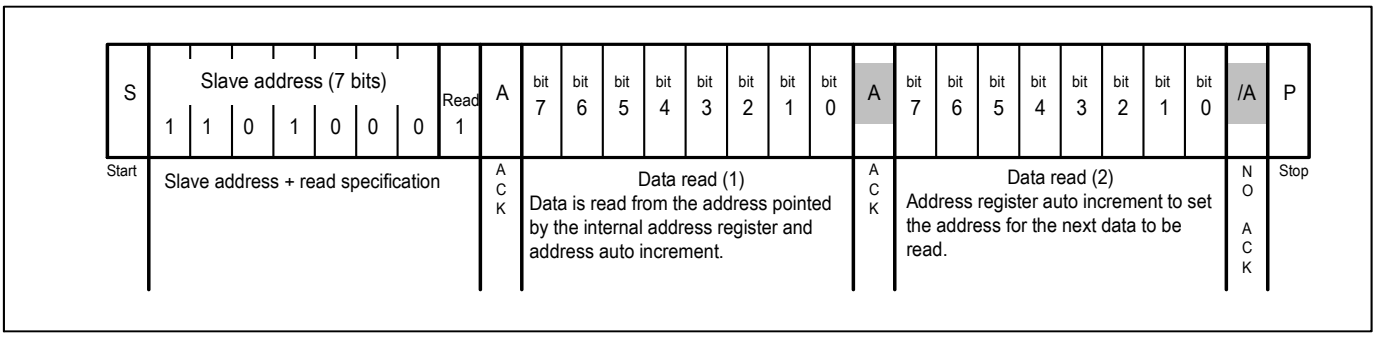
## 2) Read via I²C Bus

### (1) Standard Read




### (2) Simplified Read




**Note:**

1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.
2. 49H, 4AH are used as test mode address. Customer should not use the addresses.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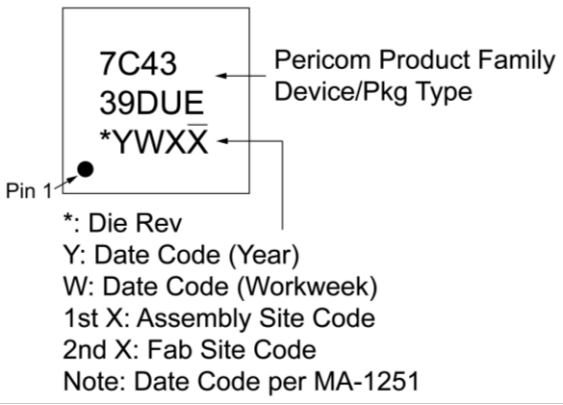
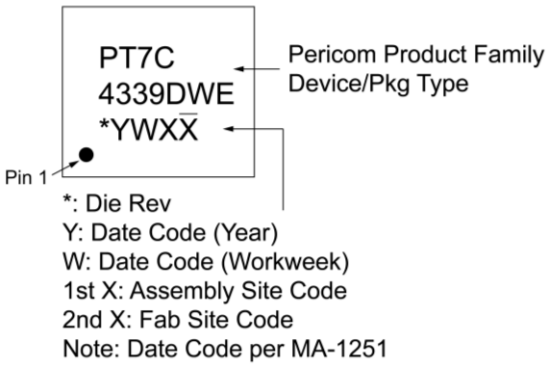
## Part Marking

**U Package**




**W Package**





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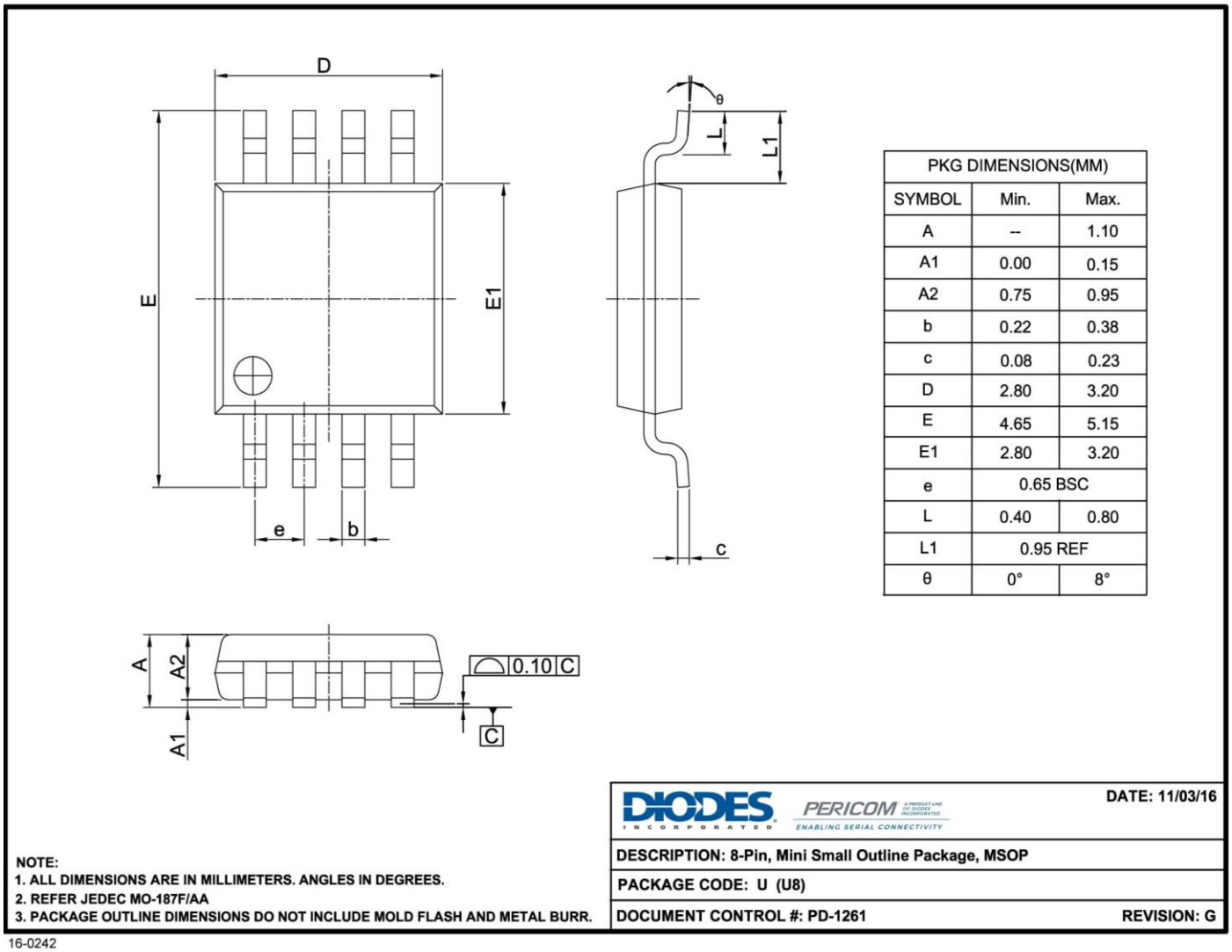
## Packaging Mechanical

**MSOP-8 (U)**




| PKG DIMENSIONS(MM) | | |
|---|---|---|
| SYMBOL | Min. | Max. |
| A | -- | 1.10 |
| A1 | 0.00 | 0.15 |
| A2 | 0.75 | 0.95 |
| b | 0.22 | 0.38 |
| c | 0.08 | 0.23 |
| D | 2.80 | 3.20 |
| E | 4.65 | 5.15 |
| E1 | 2.80 | 3.20 |
| e | 0.65 BSC | |
| L | 0.40 | 0.80 |
| L1 | 0.95 REF | |
| θ | 0° | 8° |

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. REFER JEDEC MO-187F/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

DATE: 11/03/16

DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP

PACKAGE CODE: U (U8)

DOCUMENT CONTROL #: PD-1261 REVISION: G

16-0242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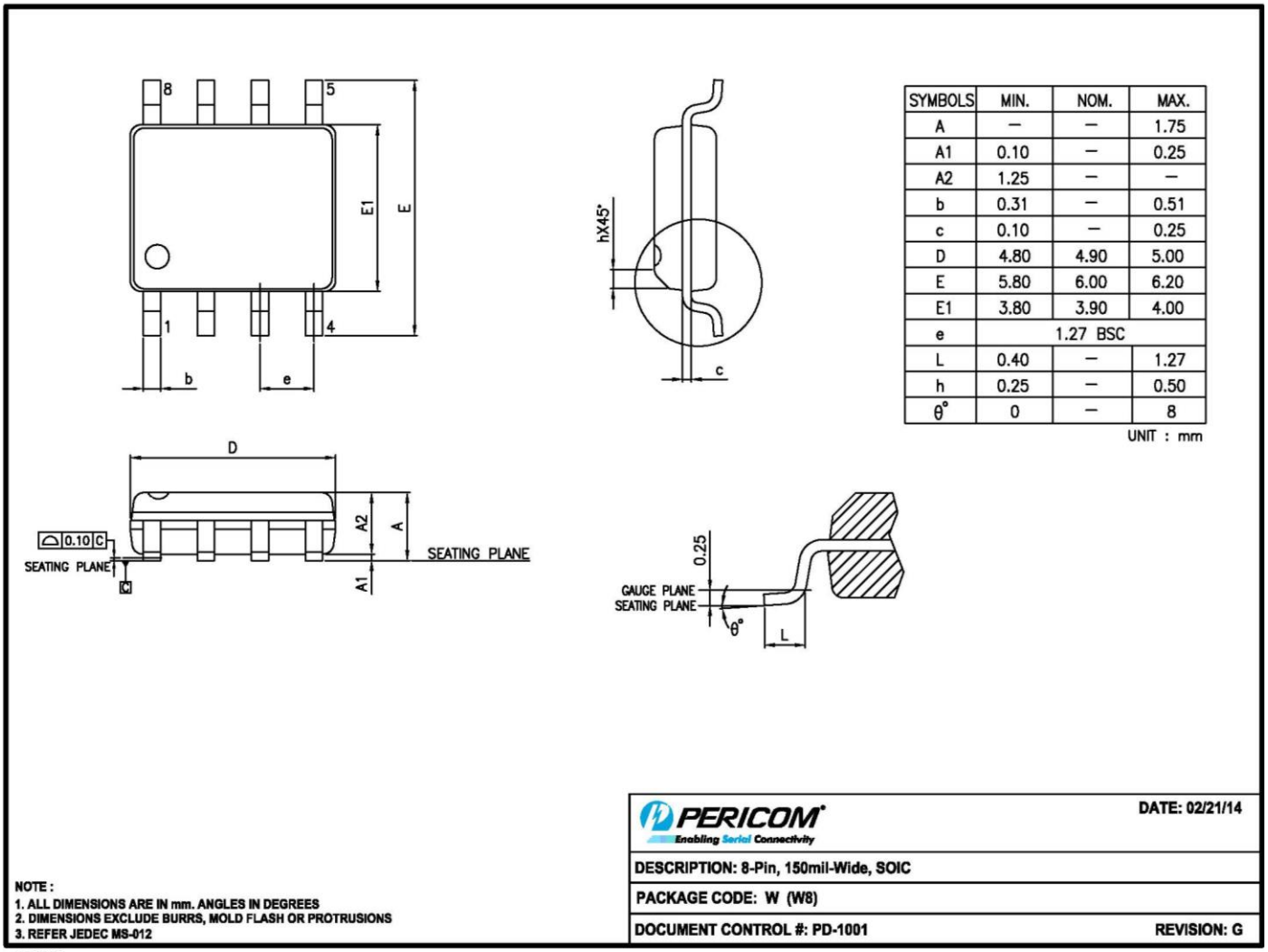
**SOIC-8 (W)**




| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | — | — | 1.75 |
| A1 | 0.10 | — | 0.25 |
| A2 | 1.25 | — | — |
| b | 0.31 | — | 0.51 |
| c | 0.10 | — | 0.25 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27 BSC | | |
| L | 0.40 | — | 1.27 |
| h | 0.25 | — | 0.50 |
| θ° | 0 | — | 8 |

UNIT : mm

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012

PERICOM Enabling Serial Connectivity — DATE: 02/21/14

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 — REVISION: G

15-0103

**For latest package info.**
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

## Mechanical Data

8-MSOP (U)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin (Sn) Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.02743 grams (Approximate)

8-SOIC (W)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin (Sn) Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.078719 grams (Approximate)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## Ordering Information

| Orderable Part Numbers | Package Code | Package Description |
|---|---|---|
| PT7C4339DUEX | U | 8-pin, Mini Small Outline Package (MSOP) |
| PT7C4339DWEX | W | 8-pin, 150mil Wide (SOIC) |

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel


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