A Product Line of
Diodes Incorporated

PI6CXG06F62a

FlexOut Ultra Low Jitter Clock Generator

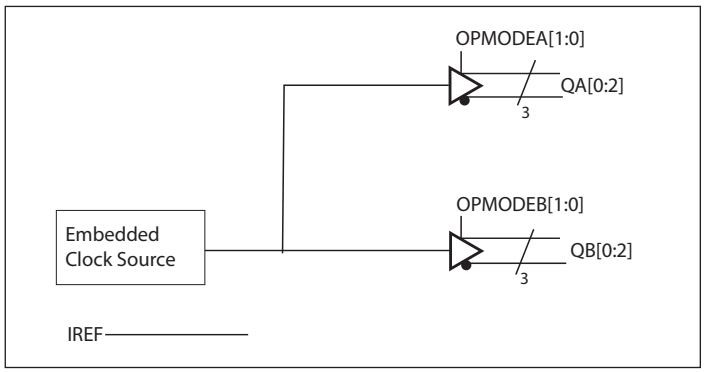
Description

The PI6CXG06F62a is part of Diodes' FlexOut clock generator family. FlexOut generators combine a low jitter high performance clock generator along with fanout capabilities. It also integrates a unique feature with user configurable output signaling standards on per bank basis which provide great flexibility to users. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

Application(s)

- Networking systems including switches and routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Features

- Ultra low jitter 156.25MHz clock generator <0.1ps max (12k to 20MHz) in LVPECL configuration
- 6 differential outputs with 2 banks
- User configurable output signaling standard for each bank: LVDS or LVPECL or HCSL
- Separate supply voltages for customized output levels
- Low skew between outputs within banks (<40ps)
- 2.5V / 3.3V power supply
- Industrial temperature support
- Packaging (Pb-free & Green):
  - 48-pin, LQFP (FBE)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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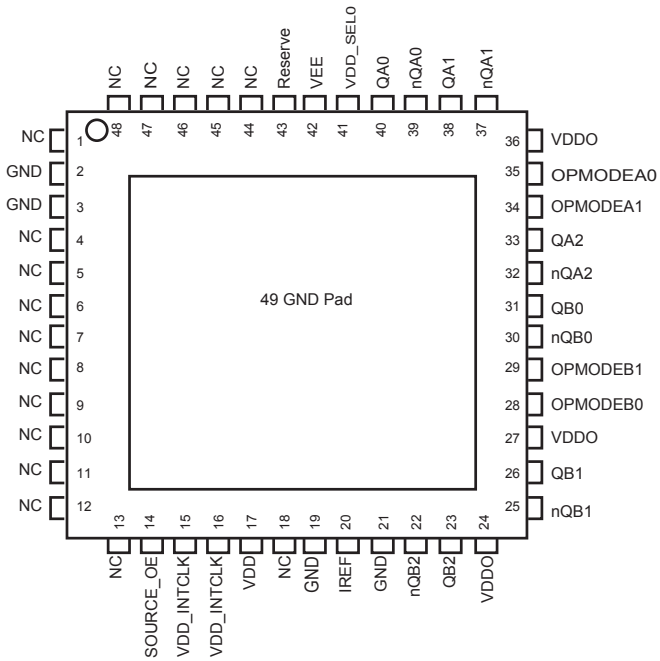
Pin Configuration



Pin Description

Pin Number	Pin Name	Type	Description
2, 3, 19, 21	GND	Power	Connect to Ground
14	SOURCE_OE	Input	Control of embedded clock source ON/ OFF
15, 16	VDD_INTCLK	Power	Voltage supply for embedded clock source
17	VDD	Power	Power supply for core
20	IREF	Output	Reference current for HCSL output tuning. Typically connected with external 475Ω resistor to GND
22, 23	nQB2 QB2	Output	Bank B differential output pair. Pin selectable LVPECL/LVDS/HCSL interface levels.
24, 27, 36	VDDO	Power	Power supply for output buffers
25, 26	nQB1 QB1	Output	Bank B differential output pair. Pin selectable LVPECL/LVDS/HCSL interface levels.
28	OPMODEB0	Input	Bank B output selection pin
29	OPMODEB1	Input	Bank B output selection pin
30, 31	nQB0 QB0	Output	Bank B differential output pair. Pin selectable LVPECL/LVDS/HCSL interface levels.

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Pin Number	Pin Name	Type	Description
32, 33	nQA2 QA2	Output	Bank A differential output pair. Pin selectable LVPECL/LVDS/HCSL interface levels.
34	OPMODEA1	Input	Bank A output selection pin
35	OPMODEA0	Input	Bank A output selection pin
37, 38	nQA1 QA1	Output	Bank A differential output pair. Pin selectable LVPECL/LVDS/HCSL interface levels.
39, 40	nQA0 QA0	Output	Bank A differential output pair. Pin selectable LVPECL/LVDS/HCSL interface levels.
41	VDD_SEL0	Power	Connect to power supply, tie high
42	VEE	Power	Connect to Negative power supply
43	Reserve	Output (Do not connect)	Embedded source debug pin. To be left open and not connected in application.
49	GND Pad	Power	Exposed pad to be connected to Ground
1, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 18, 44, 45, 46, 47, 48	NC	-	No connect

Table 1. Output Mode Select Function

OPMODEA/B [1]	OPMODEA/B [0]	Output Bank A / Bank B Mode
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

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Maximum Ratings

Above which the useful life may be impaired. For user guidelines, not tested

Storage temperature	-55 to +150°C
Supply Voltage to Ground Potential (All VDD, VDDO)	-0.5 to +4.6V
Inputs (Referenced to GND)	-0.5 to VDD+0.5V
Clock Output (Referenced to GND)	-0.5 to VDD+0.5V
V_{EE}	-0.5V
Latch up	±200mA
ESD Protection	2000 V min (HBM)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}, V_{DD_X}	Supply Voltage		3.135		3.465	V
			2.375		2.625	V
V_{DDO}	Output Supply Voltage		3.135		3.465	V
			2.375		2.625	V
V_{EE}	Negative Supply Voltage		-0.5		0	V
I_{DD}	Core Power Supply Current	All outputs unloaded		85	110	mA
I_{DDO}	Output Power Supply Current	All LVPECL outputs unloaded		69	100	
		All LVDS outputs loaded		82	100	
		All HCSL outputs unloaded		51	70	
$I_{DDTOTAL}$	Total Power Supply Current	All outputs unloaded			210	
T_A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
V_{IH}	Input high voltage	V_{DD} = 3.3V	2.0		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD} = 3.3V	-0.3		0.8	V
V_{IH}	Input high voltage	V_{DD} = 2.5V	1.7		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD} = 2.5V	-0.3		0.7	V

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DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	V_{DD} = 3.3V	2.1		2.6	V
		V_{DD} = 2.5V	1.3		1.6	
V_{OL}	Output Low voltage	V_{DD} = 3.3V	1.3		1.8	V
		V_{DD} = 2.5V	0.5		0.8	

DC Electrical Specifications- LVDS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage			1.433		V
V_{OL}	Output Low voltage			1.064		V
Vocm	Output common mode voltage			1.25		V
DVocm	Change in Vocm between output states				55	mV
Ro	Output impedance		85		140	W

DC Electrical Specifications- HCSL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		520	800		mV
V_{OL}	Output Low voltage			0	150	mV

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency			156.25		MHz
F_{STAB}	Frequency stability				±25	ppm
T_r	Output rise time	From 20% to 80%		150		ps
T_f	Output fall time	From 80% to 20%		150		ps
T_{ODC}	Output duty cycle	Generator mode	45		55	%
V_{PP}	Output swing Single-ended	LVPECL outputs	400			mV
		LVDS outputs	250			
		HCSL outputs	520			
T_{PHASEJ}	Phase jitter RMS	LVPECL		0.07	0.1	ps
		LVDS		0.09	0.12	
		HCSL		0.09	0.15	
V_{CROSS}	Absolute crossing voltage	HCSL	160		460	mV

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Parameter	Description	Conditions	Min.	Typ.	Max.	Units
DV_{CROSS}	Total variation of crossing voltage	HCSL			140	mV
T_{SK}	Output Skew	6 outputs devices, outputs in same bank, with same load, at DUT.		40		ps
T_{OD}	Valid to HiZ		200			ns
T_{OE}	HiZ to valid		200			ns
T_{start}	Start-Up Time	Counted from V_{DD} reaches 90%			10	ms

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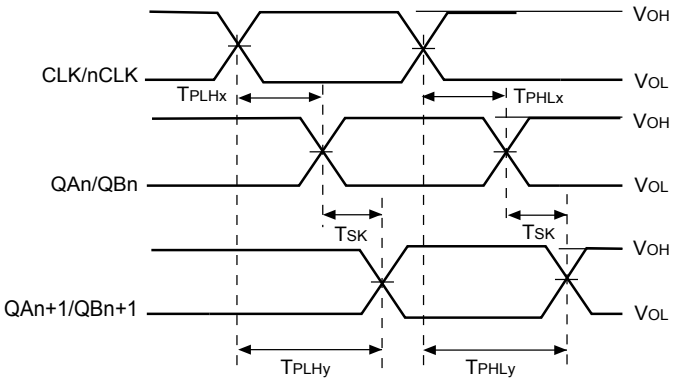
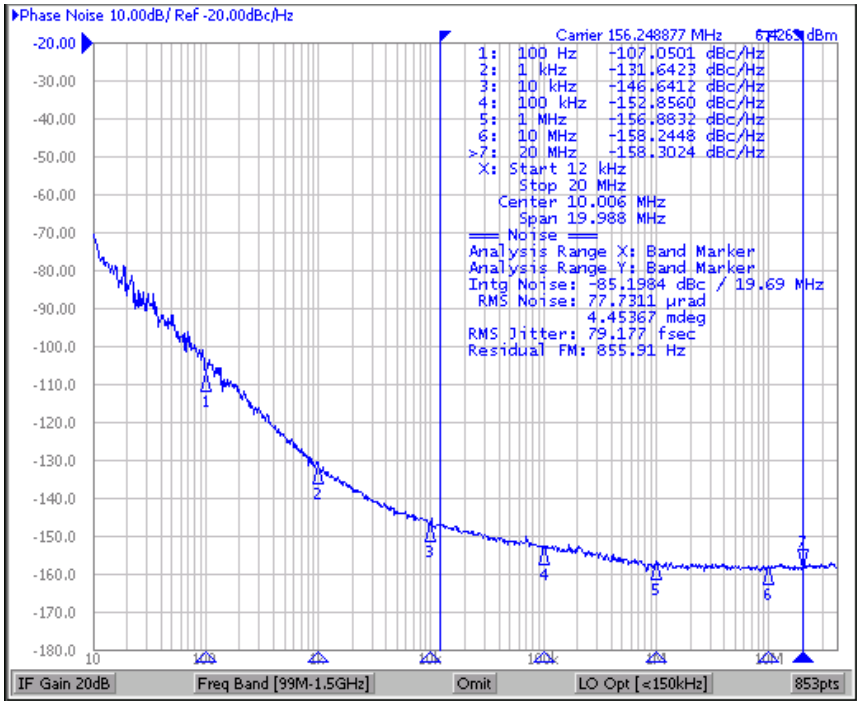


$T_{SK} = T_{PLHy} - T_{PLHx}$ or $T_{SK} = T_{PHLy} - T_{PHLx}$

Figure 1. Output Skew

Phase Noise Plots

LVPECL



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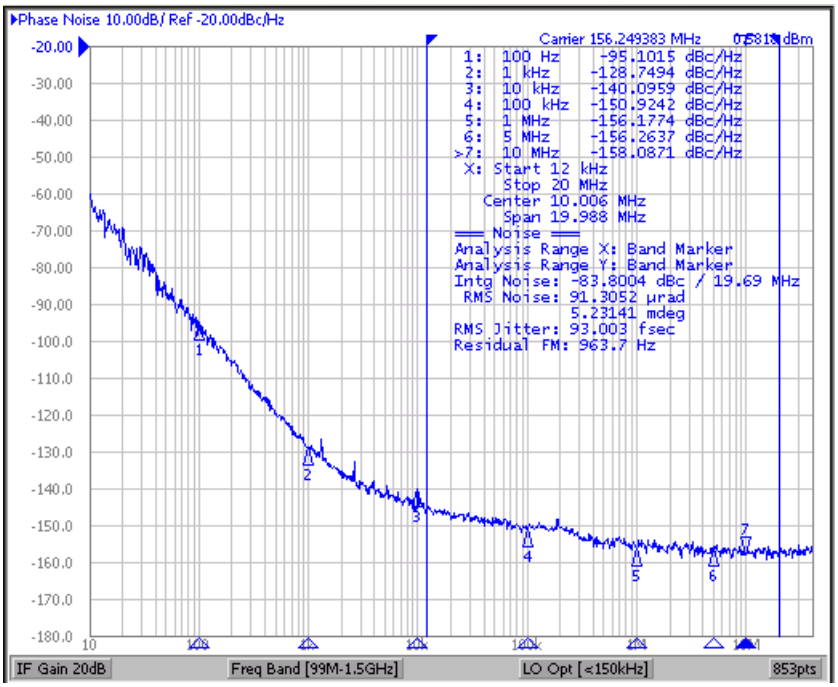
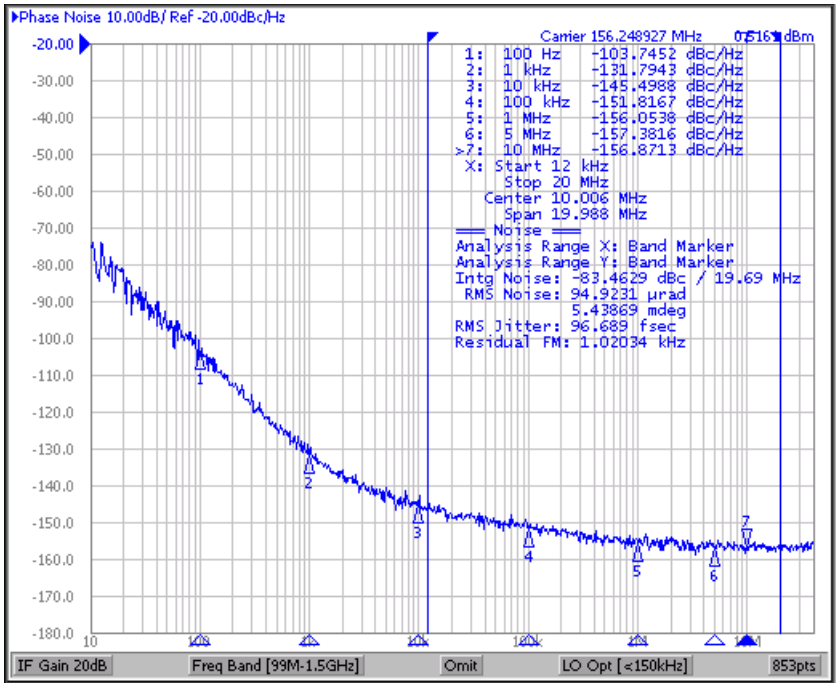
LVDS



HCSL



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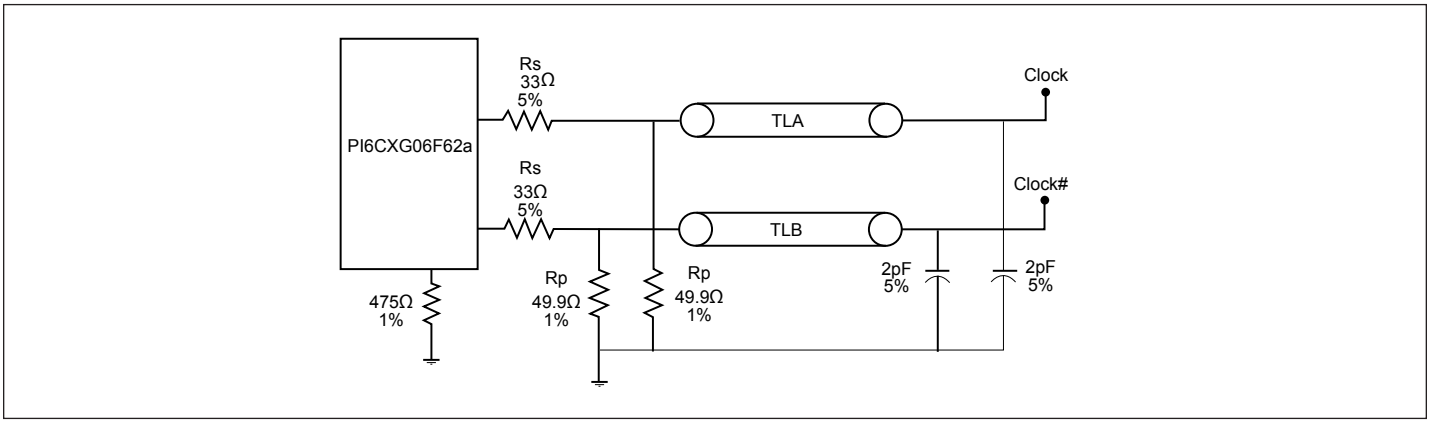

Figure 2. Configuration Test Load Board Termination for HCSL Outputs

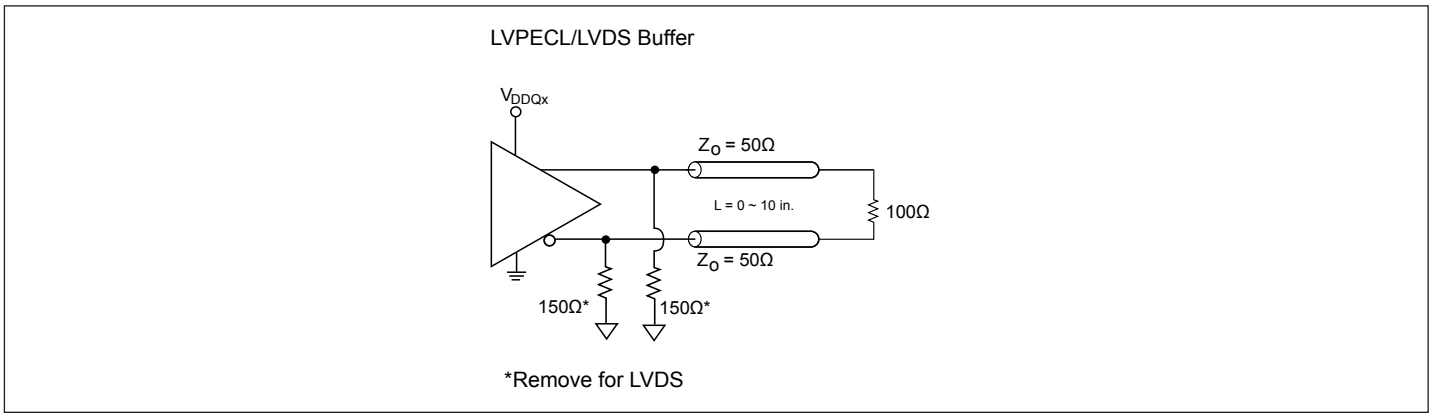

Figure 3. Configuration Test Load Board Termination for LVPECL/ LVDS Outputs

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Application Information

Suggest for Unused Inputs and Outputs

LVCMOS Input Control Pins

It is suggested to add pull-up=4.7k and pull-down=1k for LVCMOS pins even though they have internal pull-up/down but with much higher value (>=50k) for higher design reliability.

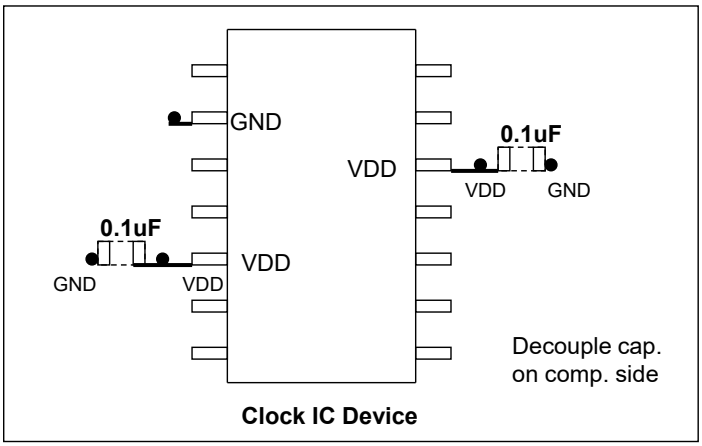
Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power supply power.

Power Decoupling & Routing

VDD Pin Decoupling

As general design rule, each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as below.

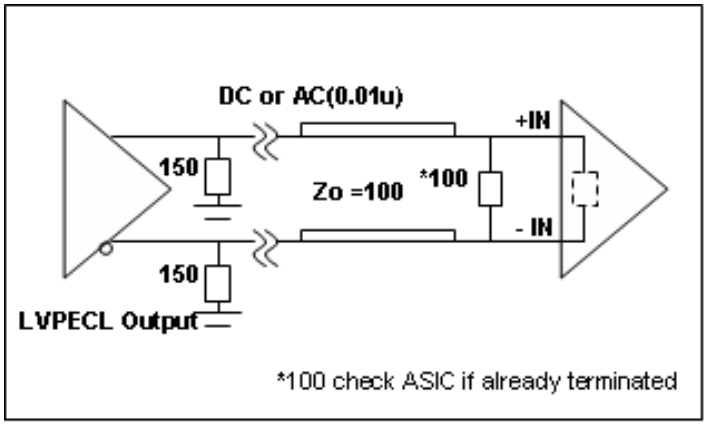


Placement of Decoupling caps

Device LVPECL Output Terminations

LVPECL Output Popular Termination

The most popular LVPECL termination is 150Ω pull-down bias and 100Ωacross at RX side. Please consult ASIC datasheet if it already has 100Ω or equivalent internal termination. If so, do not connect external 100Ω across. This popular termination's advantage is that it does not allow any bias through from V_{DD}. This prevents V_{DD} system noise coupling onto clock trace.



LVPECL Output Popular Termination

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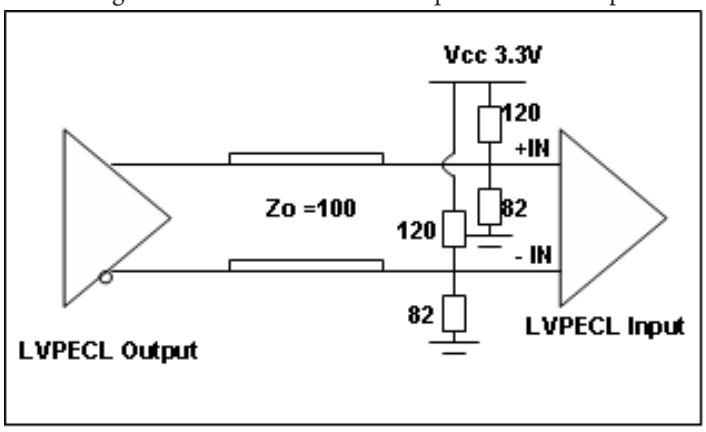
LVPECL Output Thevenin Termination

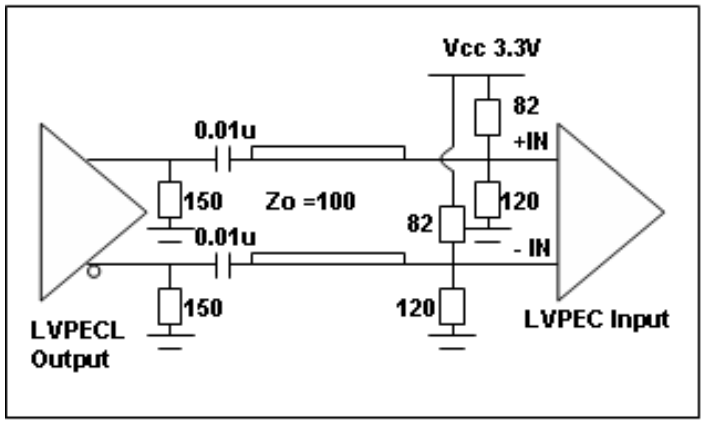
Below is an LVPECL output Thevenin termination which is used for shorter trace drive (<5in.), but it takes V_{DD} bias current and V_{DD} noise can get onto clock trace. It also requires more component count. So it is seldom used today.



LVPECL Thevenin Output Termination

LVPECL Output AC Thevenin Termination

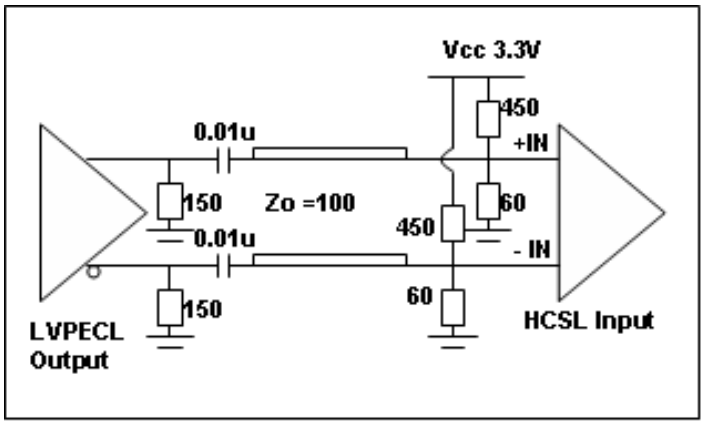
LVPECL AC Thevenin terminations require a 150Ω pull-down before the AC coupling capacitor at the source as shown below. Note that pull-up/down resistor value is swapped compared to the previous example. This circuit is good for short trace (<5in.) application



LVPECL Output AC Thenvenin Termination

LVPECL Output Drive HCSL Input

Using the LVPECL output to drive a HCSL input can be done using a typical LVPECL AC Thenvenin termination scheme. Use pull-up/down 450/60Ω to generate Vcm=0.4V for the HCSL input clock. This termination is equivalent to 50Ω load as shown below.



LVPECL Output Drive HCSL Termination

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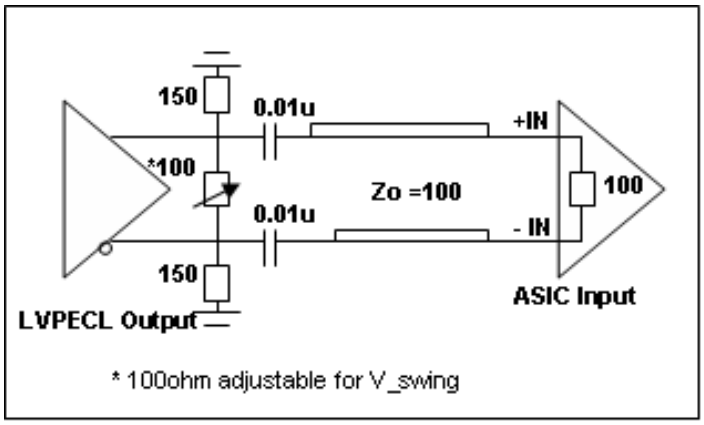
LVPECL Output V_swing Adjustment

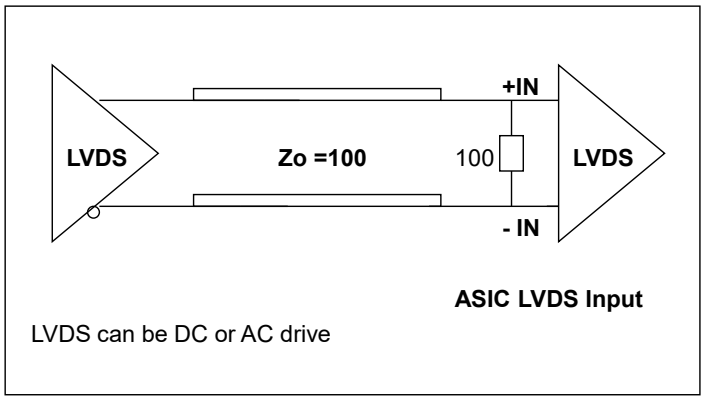
It is suggested to add another cross 100Ω at TX side to tune the LVPECL output V_swing without changing the optimal 150Ω pull-down bias in Fig. 12. This form of double termination can reduce the V_swing in ½ of the original at the RX side. By fine tuning the 100Ω resistor at the TX side with larger values like 150 to 200Ω, one can increase the V_swing by > 1/2 ratio.



LVPECL Output V_swing Adjustment

LVDS Output Termination

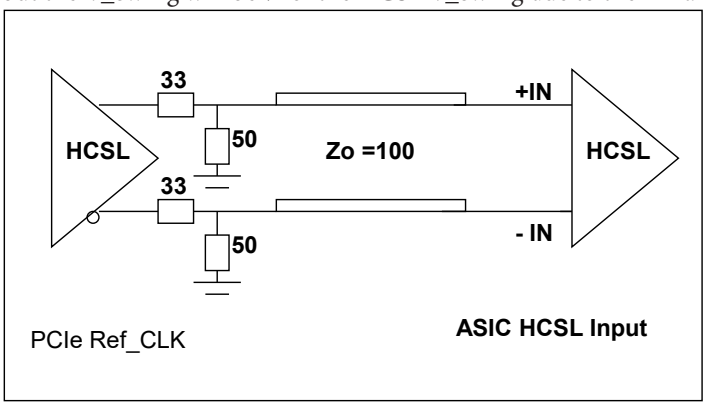
LVDS termination is different from LVPECL by removing the 150Ω pull-down bias. LVDS requires anRX termination equivalent of 100Ω across at the RX side. LVDS can be implemented via AC coupling if the ASIC has an internal termination with DC bias.



LVDS Output Driving LVDS Input

HCSL Output Termination

HCSL output is mostly used in PCIe reference clocking. It needs DC coupling to drive HCSL input with TX a 33/50Ω termination. To get better SI, it is better to put 33/50Ω termination on the component side. HCSL can AC drive LVPECL, LVDS and CML inputs too, but the V_swing will be ½ of the HCSL V_swing due to the TX and RX side double 50Ω termination.



HCSL Output Termination

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Clock Jitter Definitions

Total jitter= RJ + DJ

Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter: , where is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

Phase Jitter

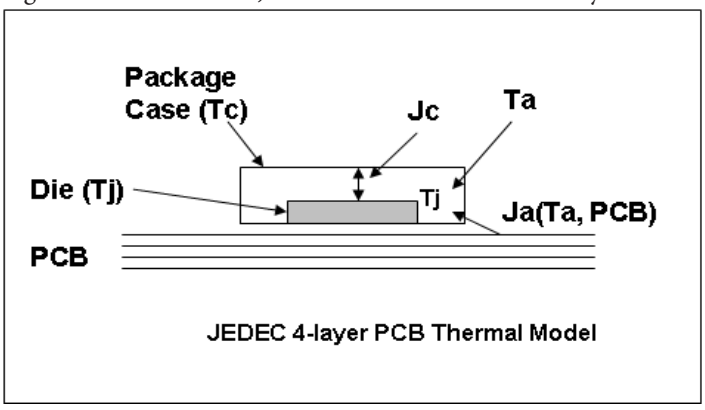
Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz@10kHz which is phase noise power in 1-Hz normalized bandwidth vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter <=1ps at 12k to 20MHz offset band as SONET standard specification.

PCIe Ref_CLK Jitter

PCIe reference clock jitter specification requires testing via the PCI-SIG jitter tool, which is regulated by US PCI-SIG organization. The jitter tool has PCIe Serdes embedded filter to calculate the equivalent jitter that relates to data link eye closure. Direct peak-peak jitter or phase jitter test data, normally is higher than jitter measure using PCI-SIG jitter tool. It has high-frequency jitter and low-frequency jitter spec. limit. For more information, please refer to the PCI-SIG website: http://www.pcisig.com/specifications/pciexpress/

Device Thermal Calculation

Figure below shows the JEDEC thermal model in a 4-layer PCB.



JEDEC IC Thermal Model

Important factors to influence device operating temperature are:

1) The power dissipation from the chip (P_chip) is after subtracting power dissipation from external loads. Generally it can be the no-load device Idd

2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker has better heat dissipation

3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature Tj

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The individual device thermal calculation formula:

Tj =Ta + Pchip x Ja

Tc = Tj - Pchip x Jc

Ja ___ Package thermal resistance from die to the ambient air in C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce Ja (still air) by 20~30%

Jc ___ Package thermal resistance from die to the package case in C/W unit

Tj ___ Die junction temperature in C (industry limit <125C max.)

Ta ___ Ambiant air température in C

Tc ___ Package case temperature in C

Pchip___ IC actually consumes power through Iee/GND current

Device Iee or GND current to calculate Tj, especially for LVPECL buffer ICs that have a 150Ω pull-down and equivalent 100Ω differential RX load.

Thermal Calculation Example

To calculate Tj and Tc of PI6CV304 in an SOIC-8 package:
Step 1: Go to Pericom web to find Ja=157 C/W, Jc=42 C/W
http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Step 2: Go to device datasheet to find Idd=40mA max.

I_{DD}	Supply Current	C_L = 33pF/33MHz		20		mA
		C_L = 33pF/66MHz		40		
		C_L = 22pF/80MHz		35		
		C_L = 15pF/100MHz		32		
		C_L = 10pF/125MHz		28		
		C_L = 10pF/155MHz		41		

Step 3: P_total= 3.3Vx40mA=0.132W
Step 4: If Ta=85°C
Tj= 85 + Ja xP_total= 85+25.9 = 105.7°C
Tc= Tj + Jc xP_total= 105.7- 5.54 = 100.1°C

Note:
The above calculation is directly using Idd current without subtracting the load power, so it is a conservative estimation. For more precise thermal calculation, use P_unload or P_chip from device Iee or GND current to calculate Tj, especially for LVPECL buffer ICs that have a 150Ω pull-down and equivalent 100Ω differential RX load.

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Part Marking



Z: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

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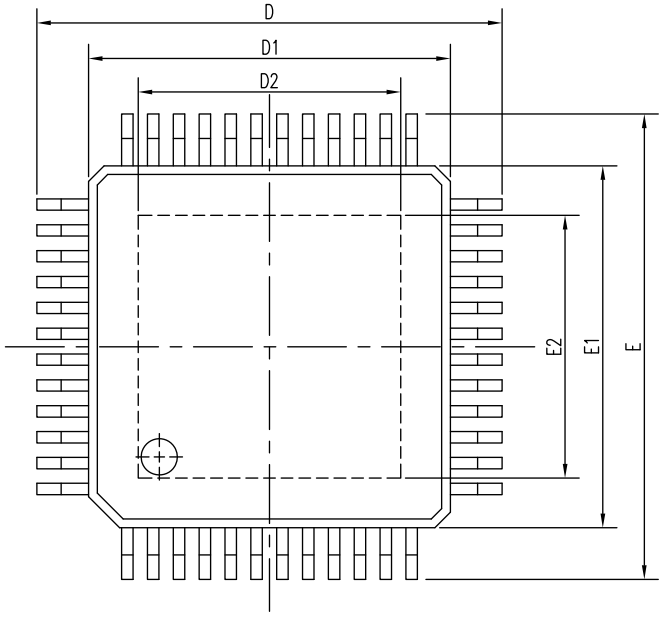
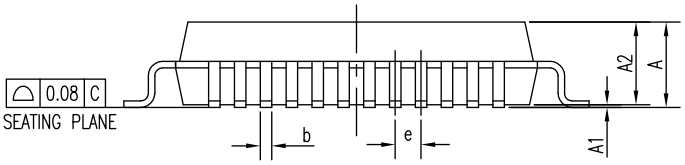
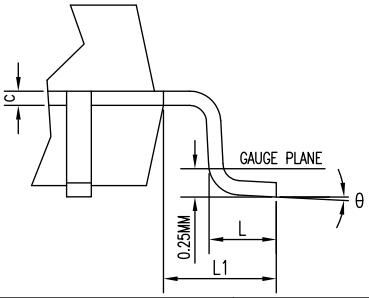
Packaging Mechanical

48-LQFP (FBE)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
D	8.90	9.00	9.10
D1	6.90	7.00	7.10
E	8.90	9.00	9.10
E1	6.90	7.00	7.10
c	0.09	--	0.20
b	0.17	0.22	0.27
e	0.50 BSC.		
L1	1.00 REF.		
L	0.45	0.60	0.75
θ	0	3.5	7
D2	4.88	5.08	5.28
E2	4.88	5.08	5.28





NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MS-026
4. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

PERICOM Enabling Serial Connectivity

DATE: 04/11/14

DESCRIPTION: 48-pin, Low Profile Quad Flat Package (LQFP) EPAD

PACKAGE CODE: FBE (FBE48)

DOCUMENT CONTROL #: PD-2185 REVISION: --

14-0045

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Orderable Part Number	Package Code	Package Description	Operating Temperature
PI6CXG06F62aFBEIEX	FBE	48-pin, Low Profile Quad Flat Package (LQFP) EPAD	-40 °C to 85 °C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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