X2600

AIoT Application Processor

Data Sheet

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1 Overview

X2600 is a low power consumption, high performance and high integrated application processor featuring a Xburst® 2 and a RISC-V Core. It integrates H264 decoder, JPEG Codec, 2D graphics engine, RGB/MIPI-DSI/LVDS display, security system and other peripherals.
DDR KGD is integrated on chip.

1.1 Block Diagram

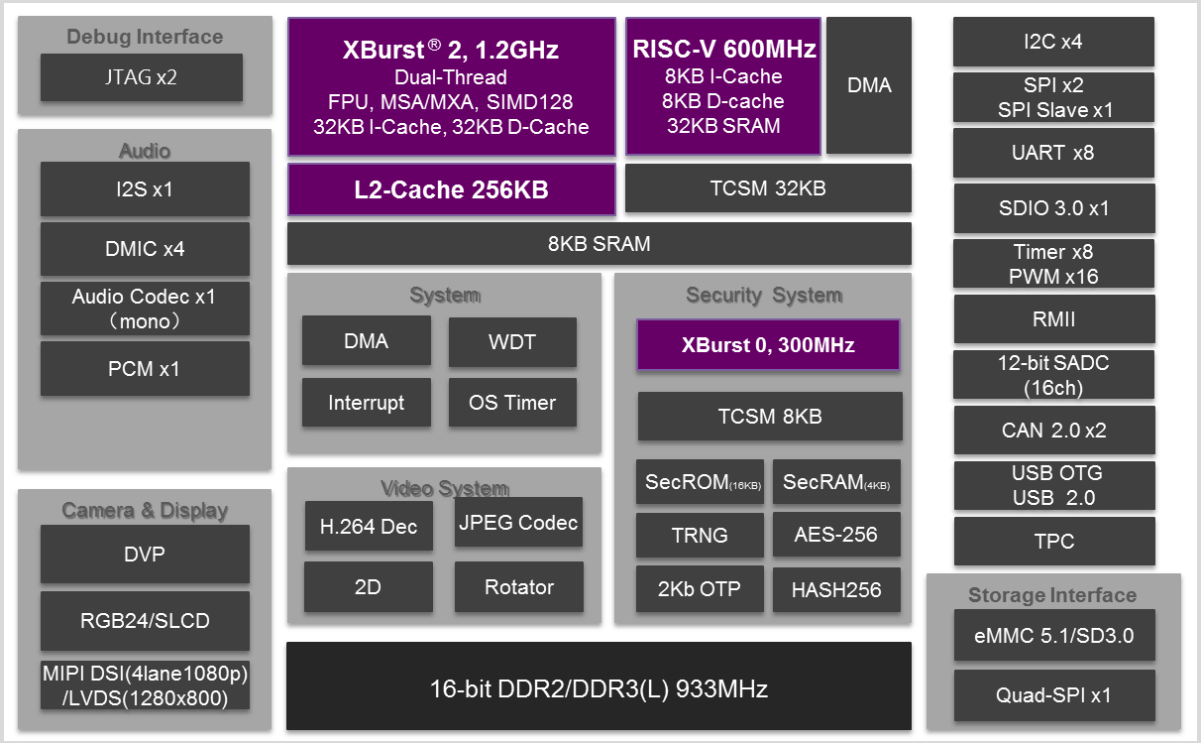


Figure 1-1 X2600 Diagram

1.2 Features

1.2.1 CPU Core

- XBurst® 2, Dual-thread, 1.2Ghz
  - 32KB L1 I-Cache, 32KB L1 D-Cache, 256 KB L2-Cache, 8KB SRAM
  - High-performance Floating-point Unit and SIMD Engine: FSE
    - 32 x 128-bit register set, 128-bit loads/stores to/from SIMD unit
    - IEEE-754 2008 compliant
  - MIPS32 ISA R2 plus MIPS SIMD instruction set architecture:128bit MSA

- Ingenic SIMD instruction set architecture: 128bit MXA
- Support JTAG

- RISC-V(LEP) 600Mhz
  - 8KB L1 D-cache +8K L1 I-cache, 32KB SRAM
  - Support JTAG

1.2.2 Memory Interface

- DDR3(L). See chapter5 for SIP DRAM size information.

1.2.3 Video process

- H.264 Decoder
  - Maximum resolution: 2560x2048
  - Decoding capabilities: 1920x1080@60fps
  - Output data format: NV12
- JPEG Decoder
  - Baseline DCT decoder according to JPEG ITU-T T.81 | ISO/IEC 10918-1 standard
  - Unlimited image size (specification up to 64Kx64K)
  - Decoding capabilities: 1920x1080@160fps(ARGB)
  - Input data format：ARGB, NV12, NV21, YUV422, RGB888, YUV444
- JPEG Encoder
  - Baseline DCT compression according to JPEG ITU-T T.81 | ISO/IEC 10918-1.
  - Unlimited image size (specification up to 64Kx64K)
  - Encoding capabilities：1920x1080@110fps(4:2:0 subsampling)
  - Output data format：ARGB, NV12, NV21, YUV422, RGB888, YUV444
- 2D Graphics Engine
  - LineDraw
  - Rectangle Fill
  - BitBLt
  - Color Space Conversion
  - Clipping
  - Alpha Blending
  - Rotation
  - Mirror
  - Scale

1.2.4 Display & Camera

- Display Controller
  - input：ARGB8888, RGB565, RGB555, ARGB1555, NV12, NV21, YUV422
  - output

- MIPI DSI interface
  - Support 2-lane, 4-lane
  - 1.5Gbps maximum data transfer rate per lane
  - Capabilities: 1920x1080@60Hz, 24BPP
- LVDS interface
  - Single channel 8bit
  - Display size up to 1280x800@60Hz, 24BPP
- RGB interface
  - Support 24bit/pixel(R:8bit, G:8bit, B:8bit)
  - Support 18bit/pixel(R:6bit, G:6bit, B:6bit)
  - Support 16bit/pixel(R:5bit, G:6bit, B:5bit)
  - Capabilities: 1280x720@60Hz, 24BPP
- 60/80-Type MCU Interface
  - Support 6800, 8080
  - Support 8/9/16/18/24-bit bus
  - Capabilities: 640x480@60Hz, 24BPP
- 3/4 wire SPI interface
  - Support Serial data transfer interface, 3/4line-spi
  - Support 8/12/16/24-bit bus

- Maximum resolution: 2047x2047

- Camera Controller
  - Support DVP 8bit input
  - Input data format：RGB888, RGB565, YCbCr 4:2:2, ITU656, RAW
  - Maximum resolution: 2047x2047
  - Capabilities: 640x480@60fps

1.2.5 Audio

- AIC Controller
  - Sample bit support: 24, 20, 18, 16 and 8 bit
  - Sample rate support: 8, 12, 16, 32, 44.1, 48, 96 Khz
  - Support I2S and MSB-Justified format
  - Support Master and Slave mode
- PCM Controller
  - Sample bit support: 16 and 8 bit
  - Sample rate support: 8, 12, 16, 32, 44.1, 48, 96 Khz
  - Support Master and Slave mode
- Internal Audio Codec
  - 24bit DAC with 90db SNR
  - 24bit ADC with 90db SNR
  - Sample bit support: 16, 20 and 24 bit
  - Sample rate support: 8, 12, 16, 32, 44.1, 48, 96 Khz

- Automatic Level Control (ALC) for smooth audio recording
- Mono Differential input/output
- Support loopback

- DMIC Controller
  - Support 1/2/3/4 channel digital MIC
  - SNR: 90dB, THD: -90dB @ FS-20dB
  - Sample bit support: 16 and 24 bit
  - Sample rate support: 8, 12, 16, 48, 96 Khz
  - Support DMIC clock frequency 2.4MHz and 3.072MHz
  - Support enable DMIC and AIC at the same time

1.2.6 System Functions

- WatchDog0/1
  - WDT0 generate full reset signal
  - WDT1 generate full interrupt
  - Each WDT has a half interrupt
  - Only EXCLK/512 can be used as the clock for counter
- OS timer
  - One 64bit global timer for system time
  - One 32bit event timer for one logical core
  - Only EXCLK can be used as the clock for counter
- Power On Reset(POR)
  - Monitor 1.8V supply for PLL and 0.9V for core

1.2.7 Security System

- XBurst® 0 MIPS-Based, 300Mhz
- 16KB Secret ROM
- 4KB Secret RAM
- True Random Number Generator
- MD5, SHA, SHA2
- AES 256/192/128-bit key size
- 2Kb OTP(EFUSE)
- Support secure boot

1.2.8 Storage Interface

- High Speed Synchronous serial interfaces (SFC)
  - SPI protocol support: Standard, Dual, Quad SPI
  - 7 transfer formats：Standard SPI, Dual-Input/Dual-Output SPI, Dual-I/O SPI, Full Dual I/O SPI, Quad-Input/Quad-Output SPI, Quad I/O SPI, Full Quad I/O SPI

- Maximum IO clock frequency of 80MHz

- SD/MMC/SDIO interface(MSC0/1)
  - Support SD 3.0/eMMC 5.1/SDIO 3.0
  - MSC0 support 1/4/8bit，MSC1 support 1/4bit
  - Maximum IO clock frequency of 180Mhz

1.2.9 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source triggered by high/low level or rising / falling edge or dual edge
  - Support shadow
- I2C x4
  - Three speeds：
    - Standard Mode(100Kb/s)
    - Fast Mode(400Kb/s)
    - High Mode(3.4Mb/s)
  - Master or slave I2C operation
  - 7/10-bit addressing
- SPI x2，SPI Slave x1
  - 3 protocols support: National’s Microwire, TI’s SSP, and Motorola’s SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
- UART x8
  - 5-, 6-, 7- or 8-bit characters
  - no parity or even or odd parity
  - 1, 1½, or 2 stop bits
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA1.1 specification
  - Maximum 3M baud rate
  - Support DMA mode
- TCU x2
  - 8 channels each channel has two pins
  - Support posedge / negedge / dualedge clock counting
  - Support gate counting(only count for gating signal)
  - Support direction counting(add / sub because of input signal)
  - Support quadrature counting
  - Support capture counting, output signal high-level time and total cycle time
  - Support exclk / gpio two clock source
- PWM x1
  - 16 channels, output signal ~50MHz, signal precision ~500MHz

- Cpu / dma mode to update config

- TPC x1
  - One print head control unit, SFT_CLKx1, SFT_DATAx8, LAT_x1, DSTx8
  - Support one 8-channel stepper motor control unit, or two 4-channel stepper motor control unit
  - Support one watchdog timer(WDT) unit
  - output signal ~50MHz, signal precision ~500MHz
- MAC x1
  - 10/100 Mbps operation
  - Supports RMII PHY interfaces
- SAR A/D Converter x1
  - Contains 16 input channels and outputs 12-bit conversion data. Up to 2MS/s sampling rate.
  - DNL < 1.5LSB, INL < 3LSB
  - Support three conversion sequences.
  - Support two conversion modes：
    - ◆ Scan conversion mode: Convert multiple analog channels one by one, and the delay time can be configured.
    - ◆ Continuous conversion mode:The sequence restarts automatically after all conversions are completed, and the restart interval can be configured.
  - Support three trigger modes: Register trigger, TCU trigger and GPIO trigger.
  - Setting the priority of the conversion sequences according to requirements can adjust the preemption strategy.
  - Support analog watchdog, interrupt is set if the analog voltage converted is below a low threshold or above a high threshold.
  - Support DMA transfers.
- CAN2.0 x2
  - Support CAN 2.0B protocol in ISO-11898-1:2003
  - Arbitration Bit Rate up to 1Mbps
  - Support DMA transfers
- USB2.0 x2
  - USB0 support OTG
  - USB1 do not support OTG，but support Device/Host by configuration
  - Fully compliant with USB specifications Rev2.0
    - ◆ high-spped（480Mbps）
    - ◆ full-speed（12Mbps）
    - ◆ low-speed （1.5Mbps）host only
  - port0 support OTG
  - soft connect/disconnect
  - 16 Endpoints
  - Supports control, interrupt, ISO and bulk transfer
  - Support wakeup, remote-wakeup

1.2.10 Bootrom

- 24KB Boot ROM

2 PAD Information

2.1 Pin Map

X2600 Ball Assignment Ver1.1

BGA209, 11mm X 11mm X 1.2mm, 0.65mm pitch, top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	SFC0_CE__MSC1_D3_PD11	SFC0_DQ2_WP__MSC1_D2_PD10	SFC0_CLK_MSC1_CLK_PD06		TCK_I2C1_SCK_UART1_TXD_PCM_CLK_PC02	DMIC_CLK_UART7_TXD_UART1_RTS_PC04		EFUSE_AVDD	SSI0_CE0__UART1_TXD_RISCV_TMS_I2C1_SCK_PB00		LCD_D22_UART5_RXD_TCU3_IN0_DST2AD14_PB26	LCD_D20_UART4_RXD_TCU2_IN0_DST0AD12_PB24	LCD_D18_UART3_RXD_TCU1_IN0_SFT_D7AD10_PB22		LCD_D13_SLCD_D13_PWM5_SFT_D2_AD5PB17	LCD_D11_SLCD_D11_PWM3_SFT_D0_AD3_PB15	LCD_D9_SLCD_D9_PWM1_DST7_AD1_PB13	A
B	UART2_TXD_PD13	UART2_RXD_PWM_TCU_ADC_TRIG_PD12	SFC0_DQ0_MSC1_CMD_PD07	TDO_I2C0_SCK_UART6_TXD_PCM_DO_PC00	TMS_I2C1_SDA_UART1_RXD_PCM_SYNC_PC03	DMIC_IN0_UART7_RXD_UART1_CTSPC05	RZQ	DDR_PLLVCCA	SSI0_DR_UART1_RXD_RISCV_TDI_I2C1_SDA_PB01	SSI0_CLK_UART1_CTS__RISCV_TCK_I2C2_SCK_PB03	LCD_D21_UART4_TXD_TCU2_IN1_DST1AD13_PB25	LCD_D19_UART3_TXD_TCU1_IN1_LAT__AD11_PB23	LCD_D17_TCU0_IN1_SFT_D6_AD9_PB21	LCD_D15_SLCD_D15_PWM7_SFT_D4_AD7_PB19	LCD_D12_SLCD_D12_PWM4_SFT_D1_AD4PB16	LCD_D8_SLCD_D8_PWM0_AD0_PB12	LCD_D7_SLCD_D7_SM7_PB11	B
C	MSC0_CLK_SFC0_CLK_SSI0_CLK_PD00	MSC0_D1_SFC0_DQ3_HOLD__I2C0_SDAPD03	SFC0_DQ1_MSC1_D0_PD08	SFC0_DQ3_HOLD__MSC1_D1_PD09	TDI_I2C0_SDA_UART6_RXD_PCM_DI_PC01	TRST_	DMIC_IN1_PC06		DDR_ZQ	SSI0_DT_UART1_RTS__RISCV_TDO_I2C2_SDA_PB02	LCD_D23_UART5_TXD_TCU3_IN1_DST3AD15_PB27		LCD_D16_TCU0_IN0_SFT_D5_AD8_PB20	LCD_D14_SLCD_D14_PWM6_SFT_D3_AD6_PB18	LCD_D10_SLCD_D10_PWM2_SFT_CLK_AD2_PB14	LCD_D6_SLCD_D6_SM6_PB10	LCD_D5_SLCD_D5_SM5_PB09	C
D		MSC0_D2_SFC0_DQ2_WP__I2C0_SCK_PD04	MSC0_CMD_SFC0_DQ0_SSI0_DT_PD01												LCD_D4_SLCD_D4_SM4_PB08	LCD_D3_SLCD_D3_SM3_PB07		D
E	MSC0_D4_DRV_VBUS_PE01	MSC0_D3_SFC0_CE__SSI0CE0__PD05	MSC0_D0_SFC0_DQ1_SSI0DR_PD02		VSS	VSS	DDR_VREF	VDDMEM	VDDMEM	VDDMEM	VDDMEM	VSS	VSS		LCD_D2_SLCD_D2_SM2_PB06	LCD_D1_SLCD_D1_SM1_PB05	LCD_D0_SLCD_D0_SM0_PB04	E
F	MSC0_D6_UART7_TXD_PE03	MSC0_D5_EXCLK_PWM10_PE02			VSS	VSS		VDDMEM	VDDMEM	VDDMEM	VDDMEM	VSS	VSS		LCD_HSYNC_SLCD_WR_SSI_SLV_DR_DST6_AVD__PB30	LCD_PCLK_SLCD_CE__SSI_SLV_CLK_DST4_RD__PB28	LCD_VSYNC_SLCD_DC_SSI_SLV_DT_DST5_WE__PB29	F
G	PE00	MSC0_D7_UART7_RXD_PE04	EXCLK_XIN		VSS	VSS	VDD	VSS	VSS	VSS	VSS	VDD			HPOUTPL	HPOUTNL	LCD_DE_SLCD_TE_SSI_SLV_CE__DST7_NEMC_CS1__PB31	G
H		EXCLK_XOUT	AUX7_UART0_CTS__PE12				VDD	VDD		VDD		VDD	VDD			VCM		H
J	AUX5_UART0_RXD_PE10	AUX4_UART0_TXD_PE09	AUX6_UART0_RTS__PE11		VDDIO_SD	VSS		VSS		VSS		VSS	VSS		MICBIAS	MICNL	MICPL	J
K		AUX3_PE08	AUX2_PE07		PLL_AVDD	PLL_AVSS		VDD	VDD	VDD		VSS	CODEC_AVDD		USB1PN	USB1PP		K
L	AUX0_I2C3_SCK_PE05	AUX1_I2C3_SDA_PE06	AUX8_PE13		VDDIO18	VSS						USB_AVD18	VDD		VBUS	USB0PN	USB0PP	L
M	AUX9_PE14	AUX12_PE17			SARADC_AVDD	VSS	VDD	VSS	VSS	VSS	VDDIO33	VSS	USB_AVD33			CIM_HSYNC_PA08	USB0ID	M
N	AUX13_PE18	AUX11_PE16	AUX10_PE15		SARADC_VREFP	VDD	TX_VCCA18	TEST_TE	VSS	VSS	VDDIO33	VSS	VDDIO_CIM		CIM_VSYNC_PA09	CIM_MCLK_PA11	CIM_PCLK_PA10	N
P		AUX15_PE20	AUX14_PE19												CIM_D6_PA06	CIM_D7_PA07		P
R	PPRST_	POR_RST_	BOOT_SEL2_PD16	TX_CLKN	TX_DATAN1		MAC_MDC_UART0_RXD_PC23	MAC_RXD1_PWM_TCU_ADC_TRIG_I2C2_SDA_PC20	MAC_TXD1_I2S0_DO_SSI1_CE0__UART4_TXDPC18	MAC_REF_CLK_I2S0_MCLK_SSI1_DT_UART3_TXD_PC16	PWM9_TCU4_IN1_CAN0_RX_UART5_RXDPC08		MSC1_CLK_SSI1_CLK_PC25	MSC1_D0_SSI1_DR_PC27	CIM_D2_PA02	CIM_D4_PA04	CIM_D5_PA05	R
T	BOOT_SEL1_PD15	TX_DATAN3	TX_DATAN2	TX_CLKP	TX_DATAP1	TX_DATAP0	MAC_RXD0_UART0_CTS__I2C3_SCK_PC21	MAC_TXD0_I2S0_DI_I2C2_SCK_PC19	MAC_PHY_CLK_I2S0_BCLK_SSI1_CLK_UART3_RXD_PC15	PWM8_TCU4_IN0_CAN0_TX_UART5_TXD_PC07	PWM11_TCU5_IN1_CAN1_RX_PC10	PWM13_TCU6_IN1_PC12	PWM15_TCU7_IN1_PC14	MSC1_D1_PC28	MSC1_CMD_SSI1_DT_PC26	CIM_D0_PA00	CIM_D3_PA03	T
U	BOOT_SEL0_PD14	TX_DATAP3	TX_DATAP2		TX_DATAN0	MAC_MDIO_UART0_TXD_PC24	MAC_CRS_DV_UART0_RTS__I2C3_SDA_PC22		MAC_TX_EN_I2S0_LRCK_SSI1_DR_UART4_RXD_PC17		PWM10_TCU5_IN0_CAN1_TX_PC09	PWM12_TCU6_IN0_PC11	PWM14_TCU7_IN0_PC13		MSC1_D3_SSI1_CE0__PC30	MSC1_D2_PC29	CIM_D1_PA01	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

2.2 Pin Description

2.2.1 GPIO Group A

Ball No.	Ball Name	DS	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
T16	CIM_D0_PA00	8mA	Hiz	fast	No	GPA [0]	CIM_D0				VDDIO_CIM
U17	CIM_D1_PA01	8mA	Hiz	fast	No	GPA [1]	CIM_D1				VDDIO_CIM
R15	CIM_D2_PA02	8mA	Hiz	fast	No	GPA [2]	CIM_D2				VDDIO_CIM
T17	CIM_D3_PA03	8mA	Hiz	fast	No	GPA [3]	CIM_D3				VDDIO_CIM
R16	CIM_D4_PA04	8mA	Hiz	fast	No	GPA [4]	CIM_D4				VDDIO_CIM
R17	CIM_D5_PA05	8mA	Hiz	fast	No	GPA [5]	CIM_D5				VDDIO_CIM
P15	CIM_D6_PA06	8mA	Hiz	fast	No	GPA [6]	CIM_D6				VDDIO_CIM
P16	CIM_D7_PA07	8mA	Hiz	fast	No	GPA [7]	CIM_D7				VDDIO_CIM
M16	CIM_HSYNC_PA08	8mA	Hiz	fast	No	GPA [8]	CIM_HSYNC				VDDIO_CIM
N15	CIM_VSYNC_PA09	8mA	Hiz	fast	No	GPA [9]	CIM_VSYNC				VDDIO_CIM
N17	CIM_PCLK_PA10	8mA	Hiz	fast	No	GPA [10]	CIM_PCLK				VDDIO_CIM
N16	CIM_MCLK_PA11	8mA	Hiz	fast	No	GPA [11]	CIM_MCLK				VDDIO_CIM

2.2.2 GPIO Group B

Ball No.	Ball Name	DS	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
A9	SSI0_CE0__UART1_TXD_RISCV_TMS_I2C1_SCK_PB00	8mA	Hiz	fast	No	GPB [0]	SSI0_CE0_	UART1_TXD	RISCV_TMS	I2C1_SCK	VDDIO33
B9	SSI0_DR_UART1_RXD_RISCV_TDI_I2C1_SDA_PB01	8mA	Hiz	fast	No	GPB [1]	SSI0_DR	UART1_RXD	RISCV_TDI	I2C1_SDA	VDDIO33

C10	SSI0_DT_UART1_RTS__RISCV_TDO _I2C2_SDA_PB02	8mA	Hiz	fast	No	GPB [2]	SSI0_DT	UART1_RTS_	RISCV_TDO	I2C2_SDA	VDDIO33
B10	SSI0_CLK_UART1_CTS__RISCV_TCK _I2C2_SCK_PB03	8mA	Hiz	fast	No	GPB [3]	SSI0_CLK	UART1_CTS_	RISCV_TCK	I2C2_SCK	VDDIO33
E17	LCD_D0_SLCD_D0_SM0_PB04	8mA	Hiz	fast	No	GPB [4]	LCD_D0	SLCD_D0		SM0	VDDIO33
E16	LCD_D1_SLCD_D1_SM1_PB05	8mA	Hiz	fast	No	GPB [5]	LCD_D1	SLCD_D1		SM1	VDDIO33
E15	LCD_D2_SLCD_D2_SM2_PB06	8mA	Hiz	fast	No	GPB [6]	LCD_D2	SLCD_D2		SM2	VDDIO33
D16	LCD_D3_SLCD_D3_SM3_PB07	8mA	Hiz	fast	No	GPB [7]	LCD_D3	SLCD_D3		SM3	VDDIO33
D15	LCD_D4_SLCD_D4_SM4_PB08	8mA	Hiz	fast	No	GPB [8]	LCD_D4	SLCD_D4		SM4	VDDIO33
C17	LCD_D5_SLCD_D5_SM5_PB09	8mA	Hiz	fast	No	GPB [9]	LCD_D5	SLCD_D5		SM5	VDDIO33
C16	LCD_D6_SLCD_D6_SM6_PB10	8mA	Hiz	fast	No	GPB [10]	LCD_D6	SLCD_D6		SM6	VDDIO33
B17	LCD_D7_SLCD_D7_SM7_PB11	8mA	Hiz	fast	No	GPB [11]	LCD_D7	SLCD_D7		SM7	VDDIO33
B16	LCD_D8_SLCD_D8_PWM0_AD0_PB 12	8mA	Hiz	fast	No	GPB [12]	LCD_D8	SLCD_D8	PWM0	AD0	VDDIO33
A17	LCD_D9_SLCD_D9_PWM1_DST7_A D1_PB13	8mA	Hiz	fast	No	GPB [13]	LCD_D9	SLCD_D9	PWM1	DST7/AD1	VDDIO33
C15	LCD_D10_SLCD_D10_PWM2_SFT_ CLK_AD2_PB14	8mA	Hiz	fast	No	GPB [14]	LCD_D10	SLCD_D10	PWM2	SFT_CLK/AD2	VDDIO33
A16	LCD_D11_SLCD_D11_PWM3_SFT_ D0_AD3_PB15	8mA	Hiz	fast	No	GPB [15]	LCD_D11	SLCD_D11	PWM3	SFT_D0/AD3	VDDIO33
B15	LCD_D12_SLCD_D12_PWM4_SFT_ D1_AD4_PB16	8mA	Hiz	fast	No	GPB [16]	LCD_D12	SLCD_D12	PWM4	SFT_D1/AD4	VDDIO33
A15	LCD_D13_SLCD_D13_PWM5_SFT_ D2_AD5_PB17	8mA	Hiz	fast	No	GPB [17]	LCD_D13	SLCD_D13	PWM5	SFT_D2/AD5	VDDIO33
C14	LCD_D14_SLCD_D14_PWM6_SFT_ D3_AD6_PB18	8mA	Hiz	fast	No	GPB [18]	LCD_D14	SLCD_D14	PWM6	SFT_D3/AD6	VDDIO33
B14	LCD_D15_SLCD_D15_PWM7_SFT_ D4_AD7_PB19	8mA	Hiz	fast	No	GPB [19]	LCD_D15	SLCD_D15	PWM7	SFT_D4/AD7	VDDIO33
C13	LCD_D16_TCU0_IN0_SFT_D5_AD8_ PB20	8mA	Hiz	fast	No	GPB [20]	LCD_D16	SLCD_RD	TCU0_IN0	SFT_D5/AD8	VDDIO33

B13	LCD_D17_TCU0_IN1_SFT_D6_AD9_PB21	8mA	Hiz	fast	No	GPB [21]	LCD_D17		TCU0_IN1	SFT_D6/AD9	VDDIO33
A13	LCD_D18_UART3_RXD_TCU1_IN0_SFT_D7_AD10_PB22	8mA	Hiz	fast	No	GPB [22]	LCD_D18	UART3_RXD	TCU1_IN0	SFT_D7/AD10	VDDIO33
B12	LCD_D19_UART3_TXD_TCU1_IN1_LAT__AD11_PB23	8mA	Hiz	fast	No	GPB [23]	LCD_D19	UART3_TXD	TCU1_IN1	LAT_/AD11	VDDIO33
A12	LCD_D20_UART4_RXD_TCU2_IN0_DST0_AD12_PB24	8mA	Hiz	fast	No	GPB [24]	LCD_D20	UART4_RXD	TCU2_IN0	DST0/AD12	VDDIO33
B11	LCD_D21_UART4_TXD_TCU2_IN1_DST1_AD13_PB25	8mA	Hiz	fast	No	GPB [25]	LCD_D21	UART4_TXD	TCU2_IN1	DST1/AD13	VDDIO33
A11	LCD_D22_UART5_RXD_TCU3_IN0_DST2_AD14_PB26	8mA	Hiz	fast	No	GPB [26]	LCD_D22	UART5_RXD	TCU3_IN0	DST2/AD14	VDDIO33
C11	LCD_D23_UART5_TXD_TCU3_IN1_DST3_AD15_PB27	8mA	Hiz	fast	No	GPB [27]	LCD_D23	UART5_TXD	TCU3_IN1	DST3/AD15	VDDIO33
F16	LCD_PCLK_SLCD_CE__SSI_SLV_CLK_DST4_RD__PB28	8mA	Hiz	fast	No	GPB [28]	LCD_PCLK	SLCD_CE_	SSI_SLV_CLK	DST4/RD_	VDDIO33
F17	LCD_VSYNC_SLCD_DC_SSI_SLV_DT_DST5_WE__PB29	8mA	Hiz	fast	No	GPB [29]	LCD_VSYNC	SLCD_DC	SSI_SLV_DT	DST5/WE_	VDDIO33
F15	LCD_HSYNC_SLCD_WR_SSI_SLV_DR_DST6_AVD__PB30	8mA	Hiz	fast	No	GPB [30]	LCD_HSYNC	SLCD_WR	SSI_SLV_DR	DST6/AVD_	VDDIO33
G17	LCD_DE_SLCD_TE_SSI_SLV_CE__DST7_NEMC_CS1__PB31	8mA	Hiz	fast	No	GPB [31]	LCD_DE	SLCD_TE	SSI_SLV_CE_	DST7/NEMC_CS1_	VDDIO33

2.2.3 GPIO Group C

Ball No.	Ball Name	DS	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
B4	TDO_I2C0_SCK_UART6_TXD_PCM_DO_PC00	8mA	Hiz	fast	No	GPC [0]	TDO	I2C0_SCK	UART6_TXD	PCM_DO	VDDIO33
C5	TDI_I2C0_SDA_UART6_RXD_PCM_DI_PC01	8mA	PU	fast	No	GPC [1]	TDI	I2C0_SDA	UART6_RXD	PCM_DI	VDDIO33

A5	TCK_I2C1_SCK_UART1_TXD_PCM_CLK_PC02	8mA	PU	fast	No	GPC [2]	TCK	I2C1_SCK	UART1_TXD	PCM_CLK	VDDIO33
B5	TMS_I2C1_SDA_UART1_RXD_PCM_SYNC_PC03	8mA	PU	fast	No	GPC [3]	TMS	I2C1_SDA	UART1_RXD	PCM_SYNC	VDDIO33
A6	DMIC_CLK_UART7_TXD_UART1_RTS__PC04	8mA	Hiz	fast	No	GPC [4]	DMIC_CLK	UART7_TXD	UART1_RTS_		VDDIO33
B6	DMIC_IN0_UART7_RXD_UART1_CTS__PC05	8mA	Hiz	fast	No	GPC [5]	DMIC_IN0	UART7_RXD	UART1_CTS_		VDDIO33
C7	DMIC_IN1_PC06	8mA	Hiz	fast	No	GPC [6]	DMIC_IN1				VDDIO33
T10	PWM8_TCU4_IN0_CAN0_TX_UART5_TXD_PC07	8mA	Hiz	fast	No	GPC [7]	PWM8	TCU4_IN0	CAN0_TX	UART5_TXD	VDDIO33
R11	PWM9_TCU4_IN1_CAN0_RX_UART5_RXD_PC08	8mA	Hiz	fast	No	GPC [8]	PWM9	TCU4_IN1	CAN0_RX	UART5_RXD	VDDIO33
U11	PWM10_TCU5_IN0_CAN1_TX_PC09	8mA	Hiz	fast	No	GPC [9]	PWM10	TCU5_IN0	CAN1_TX		VDDIO33
T11	PWM11_TCU5_IN1_CAN1_RX_PC10	8mA	Hiz	fast	No	GPC [10]	PWM11	TCU5_IN1	CAN1_RX		VDDIO33
U12	PWM12_TCU6_IN0_PC11	8mA	Hiz	fast	No	GPC [11]	PWM12	TCU6_IN0			VDDIO33
T12	PWM13_TCU6_IN1_PC12	8mA	Hiz	fast	No	GPC [12]	PWM13	TCU6_IN1			VDDIO33
U13	PWM14_TCU7_IN0_PC13	8mA	Hiz	fast	No	GPC [13]	PWM14	TCU7_IN0			VDDIO33
T13	PWM15_TCU7_IN1_PC14	8mA	PD	fast	No	GPC [14]	PWM15	TCU7_IN1			VDDIO33
T9	MAC_PHY_CLK_I2S0_BCLK_SSI1_CLK_UART3_RXD_PC15	8mA	Hiz	fast	No	GPC [15]	MAC_PHY_CLK	I2S0_BCLK	SSI1_CLK	UART3_RXD	VDDIO33
R10	MAC_REF_CLK_I2S0_MCLK_SSI1_DT_UART3_TXD_PC16	8mA	Hiz	fast	No	GPC [16]	MAC_REF_CLK	I2S0_MCLK	SSI1_DT	UART3_TXD	VDDIO33
U9	MAC_TX_EN_I2S0_LRCK_SSI1_DR_UART4_RXD_PC17	8mA	Hiz	fast	No	GPC [17]	MAC_TXEN	I2S0_LRCK	SSI1_DR	UART4_RXD	VDDIO33
R9	MAC_TXD1_I2S0_DO_SSI1_CE0__UART4_TXD_PC18	8mA	Hiz	fast	No	GPC [18]	MAC_TXD1	I2S0_DO	SSI1_CE0_	UART4_TXD	VDDIO33
T8	MAC_TXD0_I2S0_DI_I2C2_SCK_PC19	8mA	Hiz	fast	No	GPC [19]	MAC_TXD0	I2S0_DI	I2C2_SCK		VDDIO33

R8	MAC_RXD1_PWM_TCU_ADC_TRIG_I2C2_SDA_PC20	8mA	Hiz	fast	No	GPC [20]	MAC_RXD1	PWM_TCU_ADC_TRIG	I2C2_SDA		VDDIO33
T7	MAC_RXD0_UART0_CTS__I2C3_SCK_PC21	8mA	Hiz	fast	No	GPC [21]	MAC_RXD0	UART0_CTS_	I2C3_SCK		VDDIO33
U7	MAC_CRS_DV_UART0_RTS__I2C3_SDA_PC22	8mA	Hiz	fast	No	GPC [22]	MAC_CRS_DV	UART0_RTS_	I2C3_SDA		VDDIO33
R7	MAC_MDC_UART0_RXD_PC23	8mA	Hiz	fast	No	GPC [23]	MAC_MDC	UART0_RXD			VDDIO33
U6	MAC_MDIO_UART0_TXD_PC24	8mA	Hiz	fast	No	GPC [24]	MAC_MDIO	UART0_TXD			VDDIO33
R13	MSC1_CLK_SSI1_CLK_PC25	8mA	PU	fast	No	GPC [25]	MSC1_CLK	SSI1_CLK			VDDIO33
T15	MSC1_CMD_SSI1_DT_PC26	8mA	PU	fast	No	GPC [26]	MSC1_CMD	SSI1_DT			VDDIO33
R14	MSC1_D0_SSI1_DR_PC27	8mA	PU	fast	No	GPC [27]	MSC1_D0	SSI1_DR			VDDIO33
T14	MSC1_D1_PC28	8mA	PU	fast	No	GPC [28]	MSC1_D1				VDDIO33
U16	MSC1_D2_PC29	8mA	PU	fast	No	GPC [29]	MSC1_D2				VDDIO33
U15	MSC1_D3_SSI1_CE0__PC30	8mA	PU	fast	No	GPC [30]	MSC1_D3	SSI1_CE0_			VDDIO33

2.2.4 GPIO Group D

Ball No.	Ball Name	DS	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
C1	MSC0_CLK_SFC0_CLK_SSI0_CLK_PD00	26pF	PU	fast	No	GPD [0]	MSC0_CLK	SFC0_CLK	SSI0_CLK		VDDIO_SD
D3	MSC0_CMD_SFC0_DQ0_SSI0_DT_PD01	26pF	PU	fast	No	GPD [1]	MSC0_CMD	SFC0_DQ0	SSI0_DT		VDDIO_SD
E3	MSC0_D0_SFC0_DQ1_SSI0_DR_PD02	26pF	PU	fast	No	GPD [2]	MSC0_D0	SFC0_DQ1	SSI0_DR		VDDIO_SD
C2	MSC0_D1_SFC0_DQ3_HOLD__I2C0_SDA_PD03	26pF	PU	fast	No	GPD [3]	MSC0_D1	SFC0_DQ3/HOLD_	I2C0_SDA		VDDIO_SD
D2	MSC0_D2_SFC0_DQ2_WP__I2C0_SCK_PD04	26pF	PU	fast	No	GPD [4]	MSC0_D2	SFC0_DQ2/WP_	I2C0_SCK		VDDIO_SD

E2	MSC0_D3_SFC0_CE__SSI0_CE0__PD05	26pF	PU	fast	No	GPD [5]	MSC0_D3	SFC0_CE_	SSI0_CE0_		VDDIO_SD
A3	SFC0_CLK_MSC1_CLK_PD06	8mA	PU	fast	No	GPD [6]	SFC0_CLK	MSC1_CLK			VDDIO33
B3	SFC0_DQ0_MSC1_CMD_PD07	8mA	PU	fast	No	GPD [7]	SFC0_DQ0	MSC1_CMD			VDDIO33
C3	SFC0_DQ1_MSC1_D0_PD08	8mA	PU	fast	No	GPD [8]	SFC0_DQ1	MSC1_D0			VDDIO33
C4	SFC0_DQ3_HOLD__MSC1_D1_PD09	8mA	PU	fast	No	GPD [9]	SFC0_DQ3/HOLD_	MSC1_D1			VDDIO33
A2	SFC0_DQ2_WP__MSC1_D2_PD10	8mA	PU	fast	No	GPD [10]	SFC0_DQ2/WP_	MSC1_D2			VDDIO33
A1	SFC0_CE__MSC1_D3_WAIT__PD11	8mA	PU	fast	No	GPD [11]	SFC0_CE_	MSC1_D3		WAIT_	VDDIO33
B2	UART2_RXD_PWM_TCU_ADC_TRIG_PD12	8mA	PU	fast	No	GPD [12]	UART2_RXD	PWM_TCU_ADC_TRIG			VDDIO33
B1	UART2_TXD_PD13	8mA	Hiz	fast	No	GPD [13]	UART2_TXD				VDDIO33
U1	BOOT_SEL0_PD14	8mA	Hiz	fast	Yes	GPD [14]	BOOT_SEL0				VDDIO33
T1	BOOT_SEL1_PD15	8mA	Hiz	fast	Yes	GPD [15]	BOOT_SEL1				VDDIO33
R3	BOOT_SEL2_PD16	8mA	PD	fast	Yes	GPD [16]	BOOT_SEL2				VDDIO33

2.2.5 GPIO Group E

Ball No.	Ball Name	DS	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
G1	PE00	12mA	PD	dis	No	GPE [0]					VDDIO18
E1	MSC0_D4_DRV_VBUS_PE01	12mA	Hiz	dis	No	GPE [1]	MSC0_D4	DRV_VBUS			VDDIO18
F2	MSC0_D5_EXCLK_PWM10_PE02	12mA	Hiz	dis	No	GPE [2]	MSC0_D5	EXCLK	PWM10		VDDIO18
F1	MSC0_D6_UART7_TXD_PE03	12mA	Hiz	dis	No	GPE [3]	MSC0_D6	UART7_TXD			VDDIO18
G2	MSC0_D7_UART7_RXD_PE04	12mA	Hiz	dis	No	GPE [4]	MSC0_D7	UART7_RXD			VDDIO18
L1	AUX0_I2C3_SCK_PE05	12mA	Hiz	dis	No	GPE [5]	AUX0	I2C3_SCK			SARADC_AVDD
L2	AUX1_I2C3_SDA_PE06	12mA	Hiz	dis	No	GPE [6]	AUX1	I2C3_SDA			SARADC_AVDD
K3	AUX2_PE07	12mA	Hiz	dis	No	GPE [7]	AUX2				SARADC_AVDD

K2	AUX3_PE08	12mA	Hiz	dis	No	GPE [8]	AUX3				SARADC_AVDD
J2	AUX4_UART0_TXD_PE09	12mA	Hiz	dis	No	GPE [9]	AUX4	UART0_TXD			SARADC_AVDD
J1	AUX5_UART0_RXD_PE10	12mA	Hiz	dis	No	GPE [10]	AUX5	UART0_RXD			SARADC_AVDD
J3	AUX6_UART0_RTS__PE11	12mA	Hiz	dis	No	GPE [11]	AUX6	UART0_RTS			SARADC_AVDD
H3	AUX7_UART0_CTS__PE12	12mA	Hiz	dis	No	GPE [12]	AUX7	UART0_CTS			SARADC_AVDD
L3	AUX8_PE13	12mA	Hiz	dis	No	GPE [13]	AUX8				SARADC_AVDD
M1	AUX9_PE14	12mA	Hiz	dis	No	GPE [14]	AUX9				SARADC_AVDD
N3	AUX10_PE15	12mA	Hiz	dis	No	GPE [15]	AUX10				SARADC_AVDD
N2	AUX11_PE16	12mA	Hiz	dis	No	GPE [16]	AUX11				SARADC_AVDD
M2	AUX12_PE17	12mA	Hiz	dis	No	GPE [17]	AUX12				SARADC_AVDD
N1	AUX13_PE18	12mA	Hiz	dis	No	GPE [18]	AUX13				SARADC_AVDD
P3	AUX14_PE19	12mA	Hiz	dis	No	GPE [19]	AUX14				SARADC_AVDD
P2	AUX15_PE20	12mA	Hiz	dis	No	GPE [20]	AUX15				SARADC_AVDD

2.3 Analog PAD Description

Ball No.	Pin Names	IO	Power	Pin Description
Memory				
B8	DDR_PLLVCCA	P	-	DDR PHY PLL Supply 1.8V
B7	RZQ	I	VDDMEM	For DDR, external reference resistor for output calibrating
C9	DDR_ZQ	I	VDDMEM	For DDR, external reference resistor for output calibrating
E7	DDR_VREF	P	-	Reference voltage supply of DDR , typical 0.5*VDDMEM
Power and Ground				
E8	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
E9	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
E10	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2

E11	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
F8	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
F9	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
F10	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
F11	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
M11	VDDIO33	P	-	IO digital power for GPIO Port B&C&D, 3.3V
N11	VDDIO33	P	-	IO digital power for GPIO Port B&C&D, 3.3V
L5	VDDIO18	P	-	IO digital power for GPIO Port E, 1.8V
N13	VDDIO_CIM	P	-	CIM GPIO Supply 1.8/3.3V
J5	VDDIO_SD	P	-	SD GPIO Supply 1.8/3.3V
E5	VSS	P	-	Ground
E6	VSS	P	-	Ground
E12	VSS	P	-	Ground
E13	VSS	P	-	Ground
F5	VSS	P	-	Ground
F6	VSS	P	-	Ground
F12	VSS	P	-	Ground
F13	VSS	P	-	Ground
G5	VSS	P	-	Ground
G6	VSS	P	-	Ground
G8	VSS	P	-	Ground
G9	VSS	P	-	Ground
G10	VSS	P	-	Ground
G11	VSS	P	-	Ground
J6	VSS	P	-	Ground
J8	VSS	P	-	Ground
J10	VSS	P	-	Ground
J12	VSS	P	-	Ground
J13	VSS	P	-	Ground
K12	VSS	P	-	Ground
L6	VSS	P	-	Ground

M6	VSS	P	-	Ground
M8	VSS	P	-	Ground
M9	VSS	P	-	Ground
M10	VSS	P	-	Ground
M12	VSS	P	-	Ground
N9	VSS	P	-	Ground
N10	VSS	P	-	Ground
N12	VSS	P	-	Ground
G7	VDD	P	-	Power supply 0.9V
G12	VDD	P	-	Power supply 0.9V
H7	VDD	P	-	Power supply 0.9V
H8	VDD	P	-	Power supply 0.9V
H10	VDD	P	-	Power supply 0.9V
H12	VDD	P	-	Power supply 0.9V
H13	VDD	P	-	Power supply 0.9V
K8	VDD	P	-	Power supply 0.9V
K9	VDD	P	-	Power supply 0.9V
K10	VDD	P	-	Power supply 0.9V
L13	VDD	P	-	Power Supply 0.9V
M7	VDD	P	-	Power Supply 0.9V
N6	VDD	P	-	Power Supply 0.9V
DSI-TX				
N7	TX_VCCA18	P	-	MIPI DSI Analog IO Supply 1.8V
U5	TX_DATAN0	AIO	TX_VCCA18	Lane0 negative end
T6	TX_DATAP0	AIO	TX_VCCA18	Lane0 positive end
R5	TX_DATAN1	AO	TX_VCCA18	Lane1 negative end
T5	TX_DATAP1	AO	TX_VCCA18	Lane1 positive end
T3	TX_DATAN2	AO	TX_VCCA18	Lane2 negative end
U3	TX_DATAP2	AO	TX_VCCA18	Lane2 positive end
T2	TX_DATAN3	AO	TX_VCCA18	Lane3 negative end
U2	TX_DATAP3	AO	TX_VCCA18	Lane3 positive end

R4	TX_CLKN	AO	TX_VCCA18	CLK lane negative end
T4	TX_CLKP	AO	TX_VCCA18	CLK lane positive end
Audio Codec				
K13	CODEC_AVDD	P	-	Codec Analog Supply 1.8V
H16	VCM	AO	CODEC_AVDD	Reference voltage output
J17	MICPL	AI	CODEC_AVDD	ADC channel input
J16	MICNL	AI	CODEC_AVDD	ADC channel input
J15	MICBIAS	AO	CODEC_AVDD	Microphone bias output
G16	HPOUTNL	AO	CODEC_AVDD	DAC channel output
G15	HPOUTPL	AO	CODEC_AVDD	DAC channel output
USB OTG				
M13	USB_AVD33	P	-	USB Analog Supply.3.3V
L12	USB_AVD18	P	-	USB Analog Supply.1.8V
L16	USB0PN	AIO	USB_AVD33	USB0 OTG data negative
L17	USB0PP	AIO	USB_AVD33	USB0 OTG data positive
L15	USB0VBUS	AI	USB_AVD33	The USB0VBUS is used for signaling to detect which device is connected. No charge pumps inside PHY, so no supplying capability by default. The PHY supports the VBUS divided to 3/5(default) off chip or not.
M17	USB0ID	AI	USB_AVD18	Used to identify the device attached to the PHY. The state of the pin is one of: high impedance (>1M Ω), or low impedance (<10Ω to ground).
K15	USB1PN	AIO	USB_AVD33	USB1 data negative
K16	USB1PP	AIO	USB_AVD33	USB1 data positive
SARADC				
M5	SARADC_AVDD	P	-	SARADC Analog Supply 1.8V
N5	SARADC_VREFP	AI	SARADC_AVDD	Positive reference voltage input
L1	AUX0	AI	SARADC_AVDD	SARADC input channel 0
L2	AUX1	AI	SARADC_AVDD	SARADC input channel 1
K3	AUX2	AI	SARADC_AVDD	SARADC input channel 2
K2	AUX3	AI	SARADC_AVDD	SARADC input channel 3
J2	AUX4	AI	SARADC_AVDD	SARADC input channel 4

J1	AUX5	AI	SARADC_AVDD	SARADC input channel 5
J3	AUX6	AI	SARADC_AVDD	SARADC input channel 6
H3	AUX7	AI	SARADC_AVDD	SARADC input channel 7
L3	AUX8	AI	SARADC_AVDD	SARADC input channel 8
M1	AUX9	AI	SARADC_AVDD	SARADC input channel 9
N3	AUX10	AI	SARADC_AVDD	SARADC input channel 10
N2	AUX11	AI	SARADC_AVDD	SARADC input channel 11
M2	AUX12	AI	SARADC_AVDD	SARADC input channel 12
N1	AUX13	AI	SARADC_AVDD	SARADC input channel 13
P3	AUX14	AI	SARADC_AVDD	SARADC input channel 14
P2	AUX15	AI	SARADC_AVDD	SARADC input channel 15
EFUSE				
A8	EFUSE_AVDD	P	-	EFUSE programming power, 1.8V
CPM				
G3	EXCLK_XIN	AI	VDDIO18	EXCLK OSC Input
H2	EXCLK_XOUT	AO	VDDIO18	EXCLK OSC Output
K5	PLL_AVDD	P	-	PLL Analog Supply 1.8V
K6	PLL_AVSS	P	-	PLL Analog Ground

2.4 Digital PAD Description

Ball No.	Pin Names	IO	Power	Pin Description
System Control				
R1	PPRST_	I	VDDIO33	power on reset and RESET-KEY reset input
C6	TRST_	I	VDDIO33	JTAG reset
N8	TEST_TE	I	VDDIO33	Manufacture test enable, program readable
R2	POR_RST_	O	VDDIO33	POR Reset Output(open drain)

Pin Names	IO	Pin Description
LCD		
LCD_PCLK	O	LCD pixel clock
LCD_VSYNC	O	LCD frame sync
LCD_HSYNC	O	LCD line sync
LCD_DE	O	LCD data enable
LCD_D<n>	O	LCD data output bit n (0-23)
SLCD(60/80-Type MCU)		
SLCD_WR	O	Smart LCD write signal
SLCD_CE_	O	Smart LCD chip select signal
SLCD_TE	I	Smart LCD tearing effect signal
SLCD_DC	O	Smart LCD data/command select signal
SLCD_D<n>	O	Smart LCD data output bit n (0-15)
CIM(Camera Interface)		
CIM_PCLK	I	CIM pixel clock input
CIM_HSYNC	I	CIM line horizontal sync input
CIM_VSYNC	I	CIM vertical sync input
CIM_MCLK	O	CIM master clock output
CIM_D<n>	I	CIM data input bit n (0-7)
I2S		
I2S0_MCLK	O	I2S master clock output
I2S0_BCLK	IO	I2S bit clock
I2S0_LRCK	IO	I2S LR clock
I2S0_DO	O	I2S data output
I2S0_DI	I	I2S data input
DMIC		
DMIC_CLK	O	Digital MIC clock output
DMIC_IN0	I	DMIC data in for DMIC 0/1
DMIC_IN1	I	DMIC data in for DMIC 2/3

PCM		
PCM_CLK	IO	PCM clock
PCM_SYNC	IO	PCM sync
PCM_DO	O	PCM data out
PCM_DI	I	PCM data in
SFC		
SFC0_CLK	O	Serial Flash clock output
SFC0_CE_	O	Serial Flash chip enable
SFC0_DQ0	IO	Serial Flash data
SFC0_DQ1	IO	Serial Flash data
SFC0_DQ2/WP_	IO	Serial Flash write protect signal
SFC0_DQ3/HOLD_	IO	Serial Flash hold signal
MSC		
MSC<n>_CLK	O	MSC(MMC/SD) n clock output
MSC<n>_CMD	IO	MSC(MMC/SD) n command
MSC<n>_D<m>	IO	MSC(MMC/SD) n data bit m (0-7)
PWM		
PWM<n>	O	PWM n data output
PWM_TCU_TRIG	I	Use to save PWM counter
TCU		
TCU<n>_IN0	I	TCU n data input
TCU<n>_IN1	I	TCU n data input
PWM_TCU_ADC_TRIG	I	Use to save TCU counter
UART		
UART<n>_RXD	I	UART n receiving data
UART<n>_TXD	O	UART n transmitting data
UART<n>_CTS_	I	UART n Clear to send control
UART<n>_RTS_	O	UART n Request to send control
I2C		
I2C<n>_SCK	IO	I2C n serial clock

I2C<n>_SDA	IO	I2C n serial data
SSI		
SSI0_CLK	O	SSI clock output
SSI0_CE0_	O	SSI chip enable 0
SSI0_DT	O	SSI data output
SSI0_DR	I	SSI data input
SSI_Slave		
SSI_SLV_CLK	I	SSI Slave clock
SSI_SLV_CE0_	I	SSI Slave chip enable
SSI_SLV_DT	O	SSI Slave data output
SSI_SLV_DR	I	SSI Slave data input
NEMC(LocalBus)		
NEMC_CS1_	O	NEMC chip select1
AVD_	O	Address Valid ouput
RD_	O	NEMC read enable, low active
WE_	O	NEMC write enable, low active
ADn	IO	Address[15:0], Data[15:0] in muxed mode
WAIT_	I	External wait state request signal
CAN		
CAN<n>_TX	O	CAN n TX output to CAN transceiver
CAN<n>_RX	I	CAN n RX input from CAN transceiver
TPC		
SFT_CLK	O	Thermal Print Head data clock
SFT_D<n>	O	Thermal Print Head data channel n(0-7)
LAT_	O	Thermal Print Head latch pin
DST<n>	O	Thermal Print Head heating channel n(0-7)
SM<n>	O	Stepper Motor unit channel n(0-7)
DEBUG		
TDO	O	JTAG serial data output
TDI	I	JTAG serial data input

TCK	I	JTAG clock
TMS	I	JTAG mode select
RISCV_TDO	O	JTAG serial data output for RISC-V
RISCV_TDI	I	JTAG serial data input for RISC-V
RISCV_TCK	I	JTAG clock for RISC-V
RISCV_TMS	I	JTAG mode select for RISC-V

NOTES:

1 The meaning of phases in IO cell characteristics are:
   a DS: default output drive strength
   b Pull: default driver state, PD(pull-up), PU(pull-down) , HIZ
   c SlewRate: slew-rate function select fast mode by default
   d Schmitt: The IO cell is Schmitt trigger input by default
   e I: Digtal Input
   f O: Digtal Output
   g IO: Digtal Input and Output
   h AI: Analog Input
   i AO: Analog Output
   j AIO: Analog Input and Output
2 All GPIO shared pins are reset to GPIO input except PC00-03 is function 0

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3 1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Rating

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	85	°C
VDD core power supplies voltage	-0.5	1.05	V
VDDMEM power supplies voltage(1.5V for DDR3)	-0.4	1.8	V
VDDMEM power supplies voltage(1.35V for DDR3L)	-0.4	1.8	V
VDDMEM power supplies voltage(1.8V for DDR2)	-0.5	2.3	V
DDR_PLLVCCA power supplies voltage	-0.5	1.98	V
PLL_AVDD power supplies voltage	-0.5	1.98	V
VDDIO18 power supplies voltage	-0.5	1.98	V
VDDIO33 power supplies voltage	-0.5	3.63	V
VDDIO_CIM power supplies voltage	-0.5	3.63	V
VDDIO_SD power supplies voltage	-0.5	3.63	V
TX_VCCA18	-0.1	1.98	V
CODEC_AVDD	-0.1	1.98	V
USB_AVD33 power supplies voltage	-0.1	3.63	V
USB_AVD18 power supplies voltage	-0.1	1.98	V
SARADC_AVDD	-0.1	1.98	V
EFUSE_AVDD power supplies voltage	-0.1	1.98	V
IO voltage to VDDMEM(1.5V for DDR3) supplied non-supply pins	-0.4	1.8	V
IO voltage to VDDMEM(1.35V for DDR3L) supplied non-supply pins	-0.4	1.8	V
IO voltage to VDDMEM(1.8V for DDR2) supplied non-supply pins	-0.5	2.3	V
IO voltage to VDDIO18 supplied non-supply pins	-0.3	2.28	V
IO voltage to VDDIO33 supplied non-supply pins	-0.5	3.93	V
IO voltage to VDDIO_CIM supplied non-supply pins	-0.5	3.93	V
IO voltage to VDDIO_SD supplied non-supply pins	-0.5	3.93	V
IO voltage to CODEC_AVDD supplied non-supply pins	-0.1	1.98	V
IO voltage to USB_AVD33 supplied non-supply pins	-0.1	3.63	V
input voltage to SARADC_AVDD supplied non-supply pins	-0.1	1.98	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.	-	2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VCORE	VDD core voltage	0.9	0.9	0.99	V
VMEM(1.5V)	VDDMEM voltage for DDR3	1.425	1.5	1.575	V
VMEM(1.35V)	VDDMEM voltage for DDR3L	1.283	1.35	1.45	V
VMEM(1.8V)	VDDMEM voltage for DDR2	1.71	1.8	1.89	V
VDDRPLL	DDR_PLLVCCA voltage	1.62	1.8	1.98	V
VPLLAVDD	PLL_AVDD voltage	1.62	1.8	1.98	V
VIO18	VDDIO18 voltage	1.62	1.8	1.98	V
VIO33	VDDIO33 voltage	2.97	3.3	3.63	V
VCIM(1.8V)	VDDIO_CIM voltage, use as 1.8V	1.62	1.8	1.98	V
VCIM(3.3V)	VDDIO_CIM voltage, use as 3.3V	2.97	3.3	3.63	V
VSD(1.8V)	VDDIO_SD voltage, use as 1.8V	1.7	1.8	1.95	V
VSD (3.3V)	VDDIO_SD voltage, use as 3.3V	2.7	3.3	3.63	V
VDSI18	TX_VCCA18 voltage	1.62	1.8	1.98	V
VCDC	CODEC_AVDD voltage	1.62	1.8	1.98	V
VUSB33	USB_AVD33 voltage	3.0	3.3	3.6	V
VUSB18	USB_AVD18 voltage	1.62	1.8	1.98	V
VADC	SARADC_AVDD voltage	1.62	1.8	1.98	V
VEFUSE	EFUSE_AVDD voltage	1.71	1.8	1.98	V

Table 3-3 Recommended operating conditions for SARADC pins

Symbol	Description	Min	Typical	Max	Unit
SARADC_VREFP	SARADC_VREFP and SARADC_AGND are used as reference for SARADC	-	1.8	VADC	V
V_{IADC}	AUX0-15 input voltage range	0		VADC	V

Table 3-4 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
TA	Ambient temperature	–40		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device

Table 3-5 DC characteristics for VREF

Symbol	Parameter	Min	Typical	Max	Unit
DDR_VREF(DC)	Reference voltage supply of DDR	0.49* VMEM	0.5* VMEM	0.51* VMEM	V

NOTE: The ac peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/-1% VMEM.

Table 3-6 DC characteristics for VDDIO33/VDDIO_CIM supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V_{DVDD}	I/O supply voltage		2.97	3.3	3.63	V
V_{PAD}	Voltage at IO		-0.3		V_{DVDD}+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2		V_{DVDD}+0.3	V
V_{T+}	Schmitt trig low to high threshold point		0.9		2.1	V
V_{T-}	Schmitt trig high to low threshold point		0.7		1.9	V
R_{PU}	Pull-up Resistor		36	57	100	kΩ
R_{PD}	Pull-down Resistor		35	57	103	kΩ
V_{OL}	Output low voltage				0.23	V
V_{OH}	Output high voltage		2.69			V
I_{OL}	Low level output current	2mA	3.5	6.0	8.8	mA
		4mA	8.1	13.0	20.5	mA
		8mA	13.8	23.8	35.2	mA
		12mA	18.4	31.7	46.9	mA
I_{OH}	High level output current	2mA	3.4	5.3	7.5	mA
		4mA	6.9	10.7	14.9	mA
		8mA	12.7	19.7	27.5	mA
		12mA	16.1	25.0	35.0	mA

Table 3-7 DC characteristics for VDDIO_CIM supplied pins for 1.8V application

Symbol	Parameter		Min	Typical	Max	Unit
V_{DVDD}	I/O supply voltage		1.62	1.8	1.98	V
V_{PAD}	Voltage at IO		-0.3		V_{DVDD}+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.35*V_{DVDD}	V
V_{IH}	Input High Voltage		0.65*V_{DVDD}		V_{DVDD}+0.3	V
V_{T+}	Schmitt trig low to high threshold point		0.4*V_{DVDD}		0.7*V_{DVDD}	V
V_{T-}	Schmitt trig high to low threshold point		0.3*V_{DVDD}		0.6*V_{DVDD}	V
R_{PU}	Pull-up Resistor		35	54	88	kΩ
R_{PD}	Pull-down Resistor		35	59	114	kΩ
V_{OL}	Output low voltage				0.24	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current	2mA	3.4	6.2	9.2	mA
		4mA	7.9	14.4	21.4	mA
		8mA	13.6	24.7	36.8	mA
		12mA	18.1	32.9	49.0	mA
I_{OH}	High level output current	2mA	3.6	5.5	7.6	mA
		4mA	7.3	11.1	15.1	mA

		8mA	13.4	20.4	27.9	mA
		12mA	17.0	26.0	35.5	mA

Table 3-8 DC characteristics for VDDIO_SD supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V_{DVDD}	I/O supply voltage		2.7	3.3	3.63	V
V_{PAD}	Voltage at IO		-0.3		V_{DVDD}+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.25*V_{DVDD}	V
V_{IH}	Input High Voltage		0.625*V_{DVDD}		V_{DVDD}+0.3	V
V_{T+}	Schmitt trig low to high threshold point		0.9		2.1	V
V_{T-}	Schmitt trig high to low threshold point		0.7		1.9	V
R_{PU}	Pull-up Resistor		23	29	35	kΩ
R_{PD}	Pull-down Resistor		21	26	31	kΩ
V_{OL}	Output low voltage					V
V_{OH}	Output high voltage					V
I_{OL}	Low level output current	40pF	12.9	18.2	23.6	mA
		25pF	10.1	14.2	18.4	mA
		12pF	8.4	11.9	15.4	mA
		5pF	5.6	7.9	10.2	mA
I_{OH}	High level output current	40pF	12.2	16.3	20.8	mA
		25pF	9.5	12.7	16.2	mA
		12pF	8.1	10.9	13.9	mA
		5pF	5.4	7.2	9.3	mA

Table 3-9 DC characteristics for VDDIO_SD supplied pins for 1.8V application

Symbol	Parameter		Min	Typical	Max	Unit
V_{DVDD}	I/O supply voltage		1.7	1.8	1.95	V
V_{PAD}	Voltage at IO		-0.3		V_{DVDD}+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.58	V
V_{IH}	Input High Voltage		1.27		2.00	V
V_{T+}	Schmitt trig low to high threshold point		0.4*V_{DVDD}		0.7*V_{DVDD}	V
V_{T-}	Schmitt trig high to low threshold point		0.3*V_{DVDD}		0.6*V_{DVDD}	V
R_{PU}	Pull-up Resistor		23	29	35	kΩ
R_{PD}	Pull-down Resistor		22	26	32	kΩ
V_{OL}	Output low voltage					V
V_{OH}	Output high voltage					V
I_{OL}	Low level output current	TypeA	17.3	24.5	31.8	mA
		TypeB	14.5	20.6	26.6	mA
		TypeC	12.8	18.2	23.6	mA
		TypeD	10.0	14.2	18.4	mA
I_{OH}	High level output current	TypeA	16.2	21.7	27.7	mA
		TypeB	13.5	18.1	23.1	mA

		TypeC	12.2	16.3	20.8	mA
		TypeD	9.5	12.7	16.2	mA

Table 3-10 DC characteristics for VDDIO18 supplied pins for 1.8V application

Symbol	Parameter		Min	Typical	Max	Unit
VDDIO	I/O supply voltage		1.62	1.8	1.98	V
V_{IL}	Input Low Voltage		-0.3		0.35* VDDIO	V
V_{IH}	Input High Voltage		0.65* VDDIO		VDDIO+ 0.3	V
V_T	Threshold point		0.83	0.91	1	V
V_{T+}	Schmitt trig low to high threshold point		0.95	1.03	1.12	V
V_{T-}	Schmitt trig high to low threshold point		0.73	0.8	0.9	V
V_{TPU}	Threshold point with pull-up resistor enabled		0.82	0.9	1	V
V_{TPD}	Threshold point with pull-down resistor enabled		0.84	0.92	1	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.94	1.02	1.11	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.72	0.79	0.89	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.96	1.05	1.12	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.74	0.81	0.91	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	µA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	µA
R_{PU}	Pull-up Resistor		55	79	122	kΩ
R_{PD}	Pull-down Resistor		51	87	169	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		VDDIO-0.45			V
I_{OL}	Low level output current	(DS1,DS0) = 00	7.7	12.8	17.8	mA
		(DS1,DS0) = 01	15.3	25.4	35.2	mA
		(DS1,DS0) = 10	22.8	37.6	51.7	mA
		(DS1,DS0) = 11	30.2	49.2	67.1	mA
I_{OH}	High level output current	(DS1,DS0) = 00	4.8	10.9	18.9	mA
		(DS1,DS0) = 01	9.6	21.5	37.4	mA
		(DS1,DS0) = 10	14.4	32.3	56.0	mA
		(DS1,DS0) = 11	19.1	42.8	74.2	mA

3.4 Audio Codec Electrical Characteristics

Table 3-11 Audio CodecElectrical Specification

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Microphone Bias						
Bias Voltage	V_{MICB}		0.8*AVDD		0.975*AVDD	V
Bias Current	I_{MICB}				3	mA
Microphone Gain Boost PGA						
Programmable Gain	G_{BST}		0		20	dB
Input Resistance	R_{IN}		8		44	KΩ
Input Capacitance	C_{IN}			10		pF
ALC PGA						
Programmable Gain	G_{ALC}		-18		28.5	dB
Gain Step Size				1.5		dB
ADC						
Signal to Noise Ratio	SNR	A-weighted		90		dB
Total Harmonic Distortion	THD	-3dBFS input		-80		dB
Channel Separation				90		dB
Headphone Output Driver						
Programmable Gain	G_{DRV}		-39		6	dB
Gain Step Size				1.5		dB
Output Resistance	R_{OUT}				1	Ω
Output Capacitance	C_{OUT}			20		pF

3.5 SARADC Electrical Characteristics

Table 3-12 SARADC Electrical Specification

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Condition						
Analog Supply	AVDD	-	1.62	1.8	1.98	V
SARADC Performance						
Resolution	-	-	-	12	-	bit
Effective Number of Bit	ENOB	-	10-	11	-	bit
Differential Nonlinearity	DNL	-	-1.5	-	+1.5	LSB
Integral Nonlinearity	INL	-	-3	-	+3	LSB
Reference voltage	VREFP		-	1.8	-	V
Input Capacitance	C_{IN}	-	-	16	-	pF
Sampling Rate	f_S	-	-	-	2	MS/s
Spurious Free Dynamic Range	SFDR	f_S=2MS/s f_{OUT}=1.17KHz	-	70	-	dB
Signal to Noise and Harmonic Ratio	SNDR	-	-	68	-	dB
Power Consumption						
Analog Supply Current	IAVDD	f_S=2MS/s	-	1.9	-	mA
		Power Down	-	1	-	uA
Digital Supply Current	IVDD	f_S=2MS/s	-	0.1	-	mA
		Power Down	-	1	-	uA

3.6 Power On, Reset and BOOT

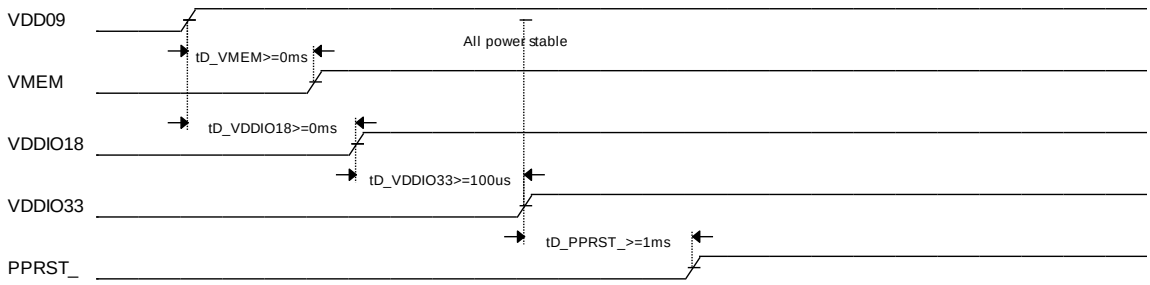
3.6.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the X2600 processor with a specific sequence of power and resets to ensure proper operation. Following are the name of the power：

- VDD09: all 0.9V power supplies
- VMEM: VDDMEM
- VDDIO18: all 1.8V power supplies, VDDIO18, PLL_AVDD, SARADC_AVDD, DDR_PLLVCCA, CODEC_AVDD, TX_VCCA18, USB_AVD18, EFUSE_AVDD, VDDIO_CIM[Note1], VDDIO_SD[Note2]
- VDDIO33: all 3.3V power supplies, VDDIO33, USB_AVD33, VDDIO_CIM[Note1], VDDIO_SD[Note2]

Table 3-13 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{D_VMEM}	Delay between VDD09 arriving 90% to VMEM arriving 50%	0	–	ms
$t_{D_VDDIO18}$	Delay between VDD09 arriving 90% to VDD18 arriving 50%	0	–	ms
$t_{D_AVDIO33}$	Delay between VDDIO18 arriving 90% to VDDIO33 to be turned on	100	–	us
$t_{D_PPRST_}$	Delay between all power rails get stable and power-on reset PPRST_ de-asserted	1	–	ms[2]



Note1: VDDIO_CIM supports two level standards, 3.3V and 1.8V.
Note2: VDDIO_SD supports two level standards, 3.3V and 1.8V.

Figure 3-1 Power-On Timing Diagram

3.6.2 Power On Reset

X2600 has an internal POR circuit, and compares PLL_AVDD,VDD with the reference voltage to generate a signal which is open-drain output.

Table 3-14 POR

Symbol	Parameter	Min	Typical	Max	Unit
V_{tha+}	Power up threshold on PLL_AVDD supply[1]	1.3	1.35	1.4	V
V_{tha-}	Power down threshold on PLL_AVDD supply[1]	1.2	1.25	1.3	V
V_{thd+}	Power up threshold on VDD supply[1]	0.55	0.6	0.65	V
V_{thd-}	Power down threshold on VDD supply[1]	0.45	0.5	0.55	V
V_{hysa}	POR hysteresis on PLL_AVDD supply[1]	-	0.1	-	V
V_{hysd}	POR hysteresis on VDD supply[1]	-	0.1	-	V
T_{dr}	Debounce delay time for POR rising edge	-	120	-	us
T_{df}	Debounce delay time for POR falling edge	-	4	-	us
T_{D_POR}	Extend delay time for POR rising edge[2]		15		ms

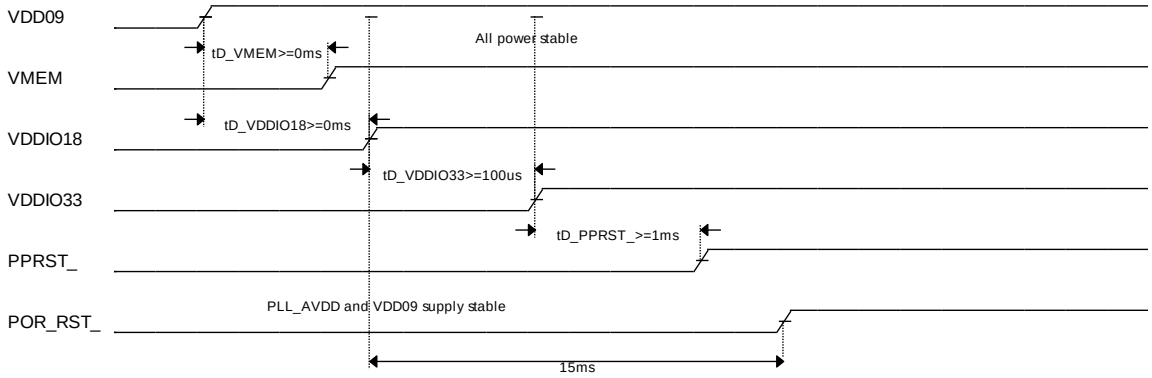


Figure 3-2 POR_RST_ Timing Diagram

Note:

1 In order to use the POR circuit to reset X2600, follow the circuit design below to connect the POR_RST_ to PPRST_.

2 After PLL_AVDD and VDD supply stable, the POR_RST_ output will be extended 15ms then release..

Following figure shows the sequence where PLL_AVDD rises first and VDD drops first.

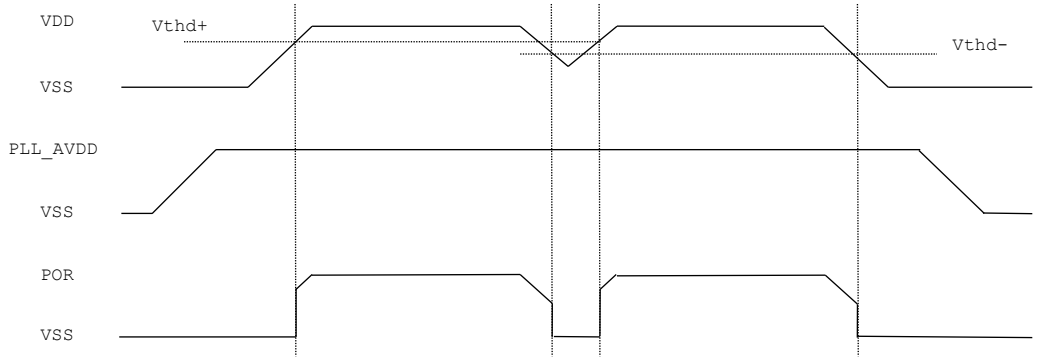


Figure 3-3 POR TIMING 1

Following figure shows the sequence where VDD rises first and PLL_AVDD drops first.

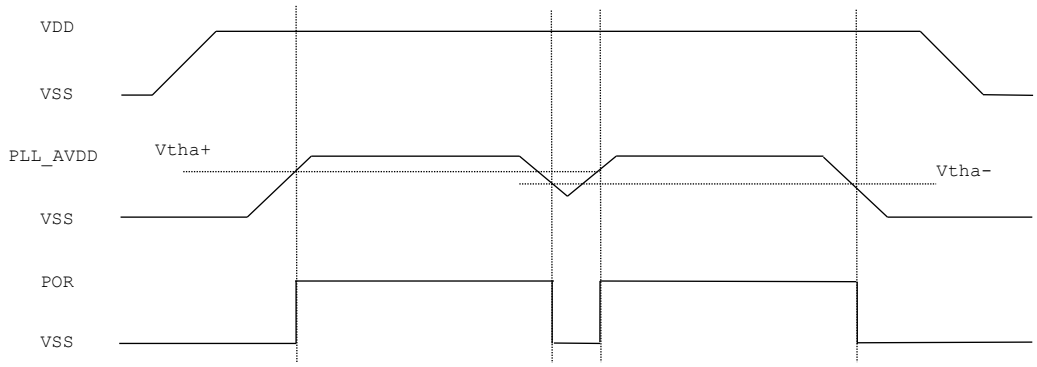


Figure 3-4 POR TIMING 2

3.6.3 Reset procedure

In addition, X2600 also supports 2 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset. After reset, program start from boot.

1. PPRST_ pin reset

This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on all power stable and RESET-KEY pressed to reset the chip from unknown dead state.

2. WDT timeout reset

This reset happens in case of WDT timeout. The reset keeps for about a few EXCLK/512 cycles.

After reset, all GPIO shared pins are put to GPIO input function, except JTAG relate TCK/ TMS/ TDI/TDO which reset to function mode. The oscillators are on

3.6.4 BOOT

The boot sequence of the X2600 is controlled by boot_sel [2:0].

Table 3-15 Boot configuration of X2600

boot_sel[2]	boot_sel[1]	boot_sel[0]	Boot configuration	Error jump
0	0	0	MSC0(PD0)_3.3V	SFC(PD0)_3.3V
0	0	1	SFC(PD6)_3.3V	MSC1(PD6)_3.3V
0	1	0	SFC(PD0)_3.3V	MSC1(PC25)_3.3V
0	1	1	USB	
1	0	1	MSC0(PD0)_1.8V	SFC(PD0)_1.8V
1	1	0	SFC(PD0)_1.8V	USB
1	1	1	USB	

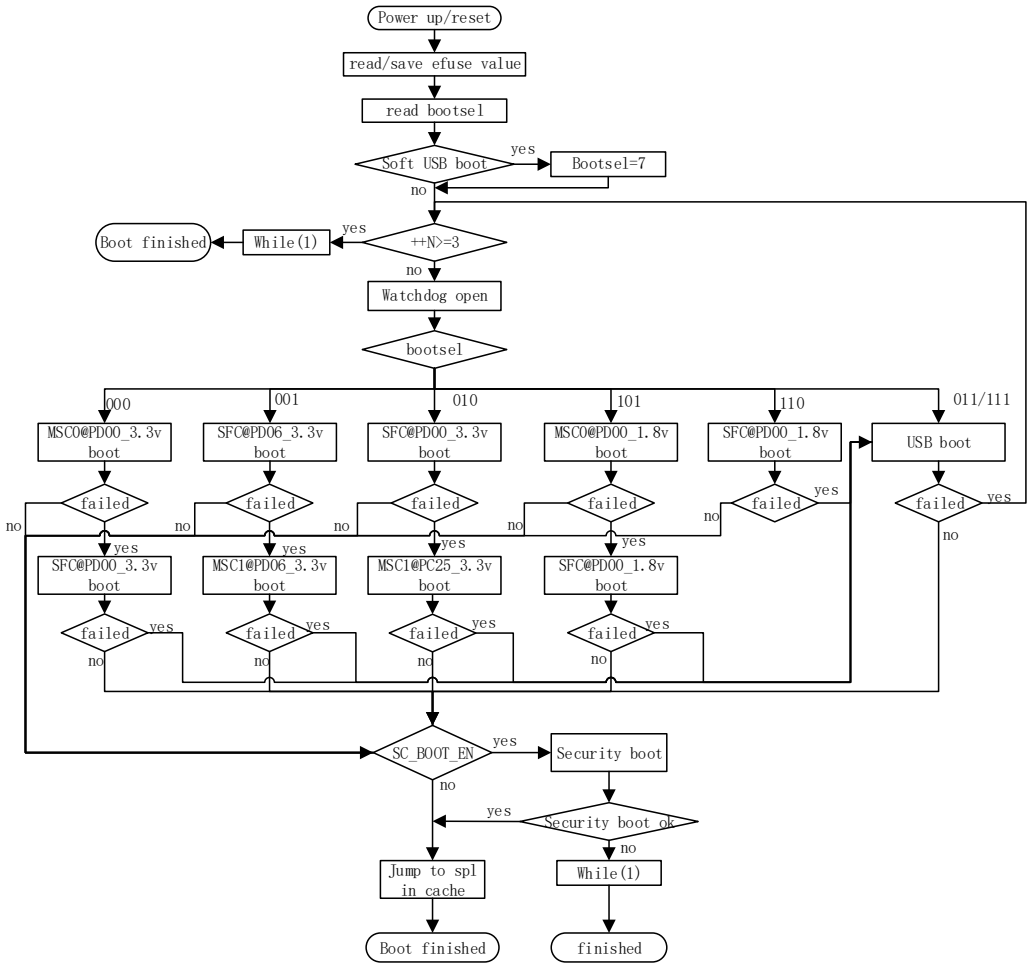


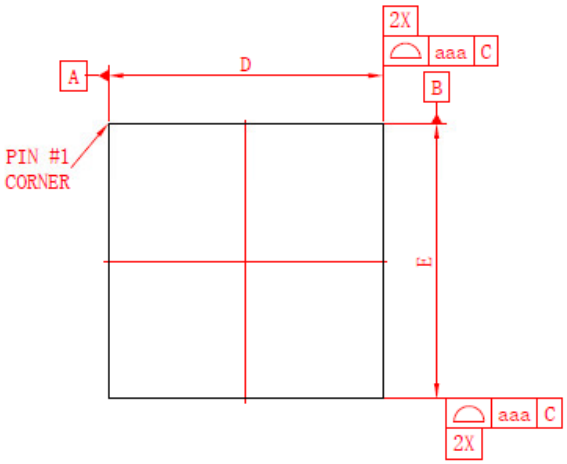
Figure 3-5 Boot sequence diagram of X2600

4 Packaging Information

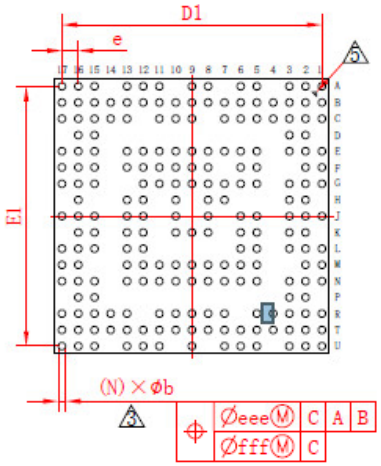
4.1 Overview

*X2600 processor is offered in 209-pin BGA package, which is 11mm * 11mm * 1.18mm outline, 17 * 17 matrix ball grid array and 0.65mm ball pitch, show in Figure 4-1.*

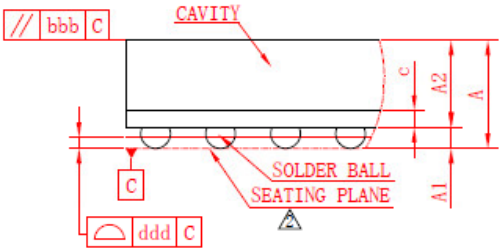
4.2 Device Dimensions



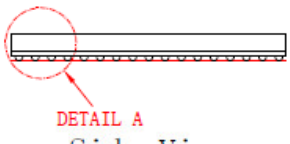
Top View



Bottom View



DETAIL A



Side View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.180	---	---	0.046
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.820	0.870	0.920	0.032	0.034	0.036
c	0.140	0.170	0.200	0.006	0.007	0.008
D	10.900	11.000	11.100	0.429	0.433	0.437
E	10.900	11.000	11.100	0.429	0.433	0.437
D1	---	10.400	---	---	0.409	---
E1	---	10.400	---	---	0.409	---
e	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	209			209		
MD/ME	17/17			17/17		

Figure 4-1 X2600 package outline drawing

Notes:

1. BALL PAD OPENING: 0.270mm;
2. PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER,PARALLEL
4. TO PRIMARY DATUM C;
5. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd;
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
7. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;

4.3 Solder Ball Materials

Both the top (joint) and bottom solder ball materials of X2600 are SAC125.

4.4 Moisture Sensitivity Level

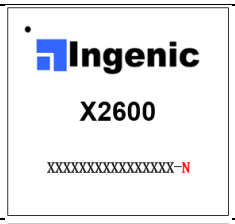
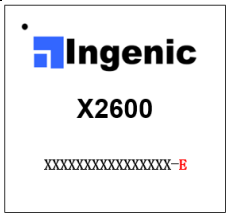
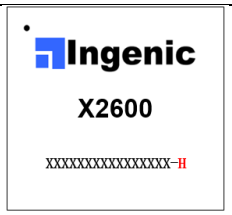
X2600 package moisture sensitivity is level 3.

5 Device Name & Part Numbers

5.1 Device Name

The device name is X2600. This is a family including Part Numbers of X2600N, X2600E, and X2600H.

5.2 Part Numbers

Part Number	DRAM SIP (Bytes)	VDDMEM Power Rail (Volt)	Marking On Chip	IC Package	EVB Board
X2600N	DDR3 128M	1.5		11mm*11mm*1.18mm BGA 209 Pin to pin compatible.	Halley 7
	DDR3(L) 128M	1.35			
X2600E	DDR3 256M	1.5			
	DDR3(L) 256M	1.35			
X2600H	DDR3 512M	1.5			
	DDR3(L) 512M	1.35			

5.3 When used in PO or invoice

Part Numbers should be specified in POs and invoices. If the device name X2600 is used, Part Numbers should be attached in some way.

5.4 DDR3 & DDR3(L)

For the X2600N, there are options for DDR3 and DDR3(L), but the packaged KGD (Known Good Die) is the same. The voltage of VDDMEM determines whether the KGD is working as DDR3 or DDR3(L). The KGD can automatically adapt to the appropriate mode. The same applies to the X2600E and X2600H.