XR81102

Universal Clock - High Frequency LVPECL Clock Synthesizer

General Description

The XR81101-CA02 is a clock synthesizer operating at a 3.3V/2.5V supply with Integer divider, using a 25MHz parallel resonant crystal reference input provides a 125MHz LVPECL outputs. The device is optimized for use with a 25MHz crystal (or system clock) and generates a 125MHz output clock for GE applications. The LVPECL outputs have very low phase noise jitter of sub 150fs, while consuming extremely low power.

The application diagram below shows a typical synthesizer configuration with any standard crystal oscillating in fundamental mode. Internal load capacitors are optionally available to minimize/eliminate external crystal loads. A system clock can also be used to overdrive the oscillator for a synchronous timing system.

The typical phase noise plot below shows the jitter integrated over the 1.875MHz to 20MHz range that is widely used in WAN systems. These clock devices show a very good high frequency noise floor below -150dB.

The XR81102 is a family of Universal Clock synthesizer devices in TSSOP-8 packages. The devices generate ANY frequency in the range of 100MHz to 1.5GHz by utilizing a highly flexible delta sigma modulator and a wide ranging VCO. These devices can be used with standard crystals or external system clock to support a wide variety of applications. This family of products has an extremely low power PLL block with core power consumption 40% less than the equivalent devices from competition. By second sourcing several of the existing sockets, these devices provides a very compelling power efficiency value benefit across all market segments.

Other clock multiplier and/or driver configurations are possible in this clock family and can be requested from the factory

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FEATURES

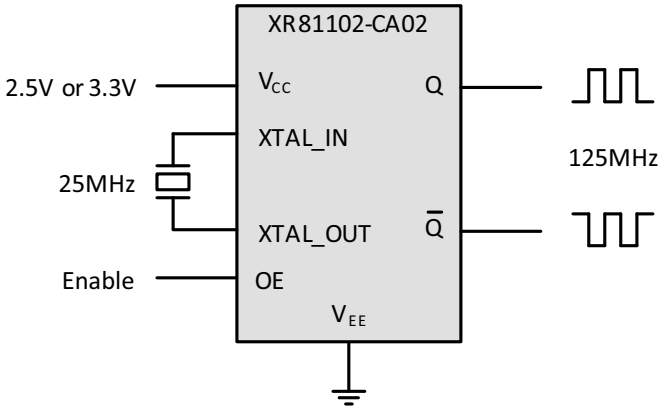
- XR81102-CA02: Factory configured
- One differential LVPECL output pair
- Crystal oscillator interface which can also be overdriven using a single-ended reference clock
- Output frequency: 125MHz
- Crystal/input frequency: 25MHz, parallel resonant crystal
- RMS phase jitter @ 125MHz, 1.875MHz - 20MHz: < 150fs
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) package

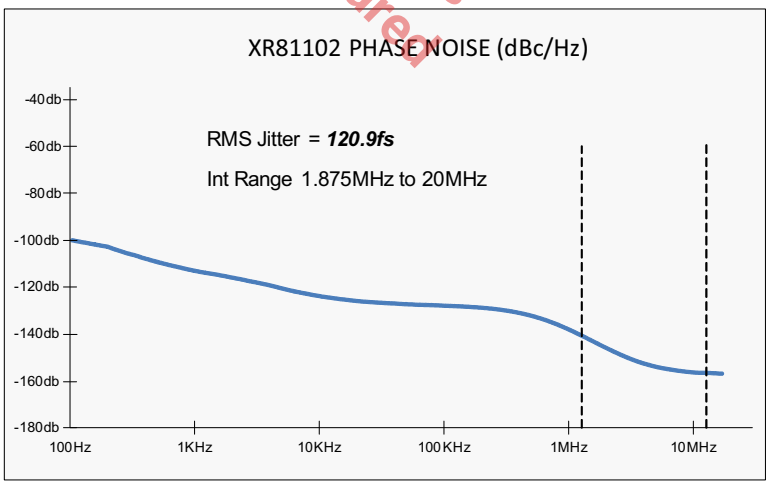
APPLICATIONS

- Gigabit Ethernet
- Low-jitter Clock Generation
- Synchronized clock systems

Ordering Information – page 8

Typical Application





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Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Maximum Rating condition for extended periods may affect device reliability and lifetime.

Supply Voltage.....+4.2V

Input Voltage.....-0.5V to VCC + 0.5V

Output Voltage.....-0.5V to VCC + 0.5V

Reference Frequency/Input Crystal.....10MHz to 60MHz

Storage Temperature.....-55°C to +125°C

Lead Temperature (Soldering, 10 sec).....300°C

ESD Rating (HBM - Human Body Model).....2kV

Operating Conditions

Operating Temperature Range.....-40°C to +85°C

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Electrical Characteristics

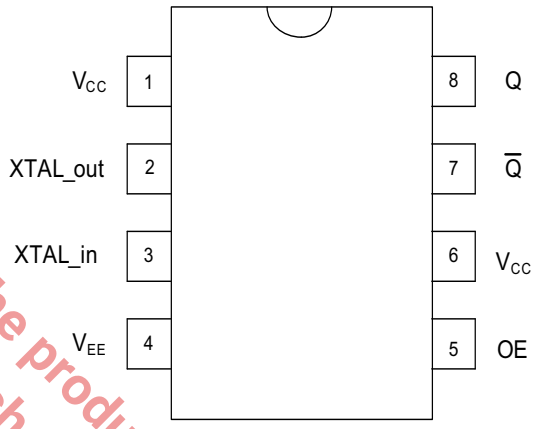
Unless otherwise noted: T_A = -40°C to +85°C, V_{CC} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V

Symbol	Parameter	Conditions	*	Min	Typ	Max	Units
3.3V Power Supply DC Characteristics							
V_{CC}	Power Supply Voltage		•	3.135	3.3	3.465	V
I_{EE}	Power Supply Current	Measured at 156.25MHz and includes the output load current			68		mA
2.5V Power Supply DC Characteristics							
V_{CC}	Power Supply Voltage		•	2.375	2.5	2.625	V
I_{EE}	Power Supply Current	Measured at 156.25MHz and includes the output load current			58		mA
LVCMOS/LVTTL DC Characteristics							
V_{IH}	Input High Voltage	V_{CC} = 3.465V	•	2.42		V_{CC} + 0.3	V
		V_{CC} = 2.625V	•	1.83		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	V_{CC} = 3.465V	•	-0.3		1.03	V
		V_{CC} = 2.625V	•	-0.3		0.785	V
I_{IH}	Input High Current (OE, FSEL[1:0])	V_{IN} = V_{CC} = 3.465V or 2.625V	•			15	µA
I_{IL}	Input Low Current (OE, FSEL[1:0])	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	•	-10			µA
LVPECL DC Characteristics							
V_{OH}	Output High Voltage		•	V_{CC} - 1.3		V_{CC} - 0.4	V
V_{OL}	Output Low Voltage		•	V_{CC} - 2.0		V_{CC} - 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		•	0.6		1.2	V
Crystal Characteristics							
X_{Mode}	Mode of Oscillations			Fundamental			
X_f	Frequency				25		MHz
ESR	Equivalent Series Resistance					50	Ω
C_S	Shunt Capacitance					7	pF
AC Characteristics							
f_{OUT}	Output Frequency				125		MHz
$t_{jit}(\phi)$	RMS Phase Jitter	125MHz Integration Range 1.875MHz-20MHz			0.15		pS
$t_{jit}(cc)$	Cycle-to-Cycle Jitter	Using 25MHz, 18pF resonant crystal	•			10	pS
t_R/t_F	Output Rise/Fall Time	20% to 80%	•	100		500	pS
Odc	Output Duty Cycle		•	48		52	%

* Limits applying over the full operating temperature range are denoted by a "•".

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Pin Configuration



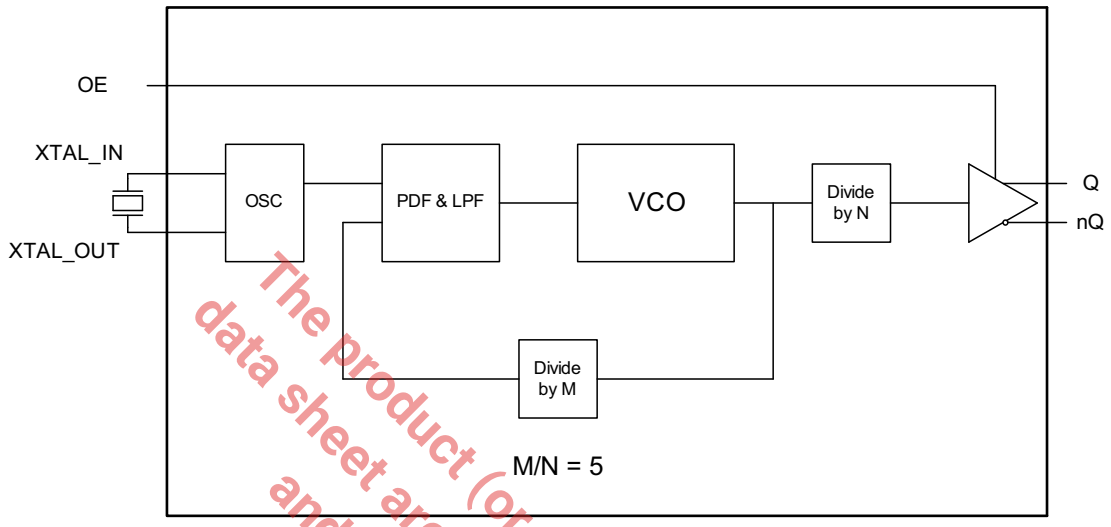
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Pin Assignments

Pin No.	Pin Name	Type	Description
1	V_{CC}	Supply	Power supply pin.
2	XTAL_OUT	Output	Crystal oscillator output.
3	XTAL_IN	Input	Crystal oscillator input.
4	V_{EE}	Supply	Negative supply pin.
5	OE	Input (900KΩ pull-up)	Output enable pin - LVCMOS/LVTTL active high input. Outputs are enabled when OE = high. Outputs are disabled when OE = low.
6	V_{CC}	Supply	Power supply pin.
7	$\overline{Q}$	Output	Inverted LVPECL output.
8	Q	Output	Positive LVPECL output.

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Functional Block Diagram



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Typical Performance Characteristics

Figure 1 shows a typical phase noise performance plot for a 125MHz clock output. The data was taken using the industry standard Agilent E5052B phase noise instrument. The integration range is 1.875MHz to 20MHz.

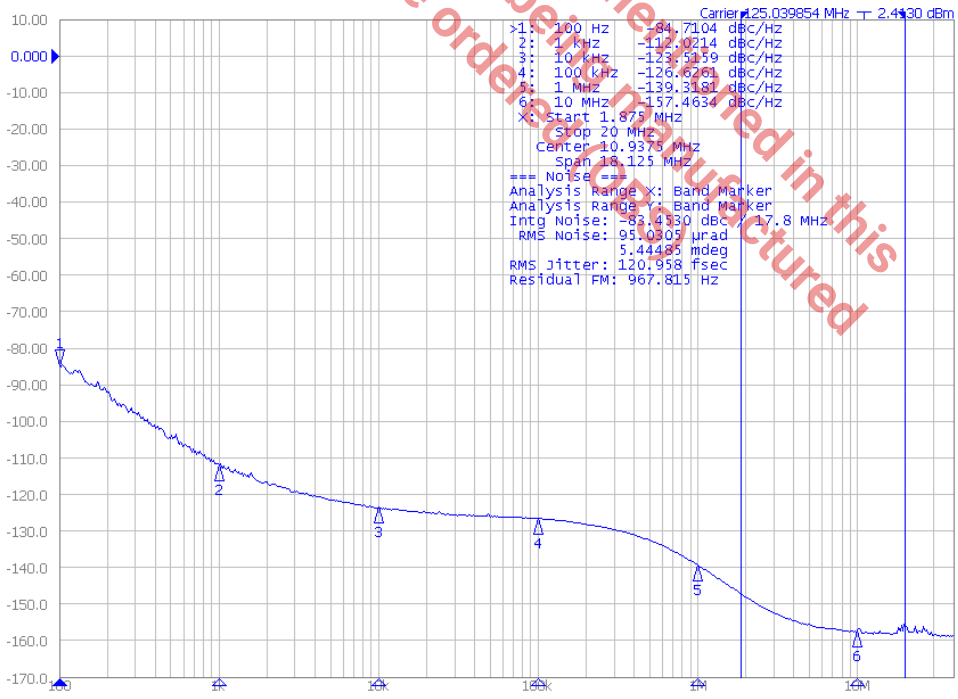


Figure 1: 125MHz Operation, Typical Phase Noise at 3.3V

Application Information

Termination for LVPECL Outputs

The termination schemes shown in Figure 2 and Figure 3 are typical for LVPECL outputs. Matched impedance layout techniques should be used for the LVPECL output pairs to minimize any distortion that could impact your maximum operating frequency. Figure 4 is an alternate termination scheme that uses a Y-termination approach.

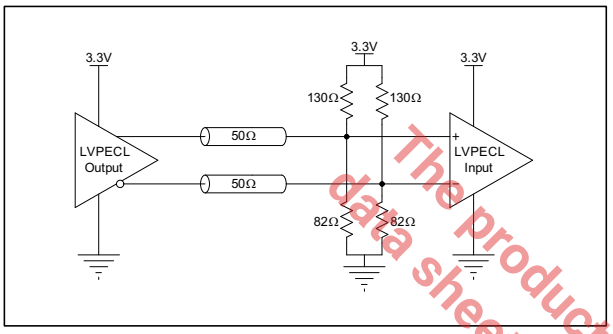


Figure 2: XR81102 3.3V LVPECL Output Termination

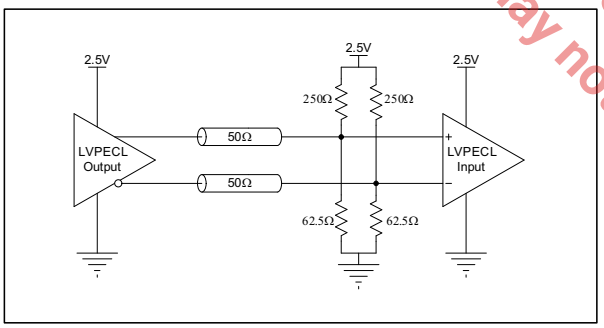


Figure 3: XR81102 2.5V LVPECL Output Termination

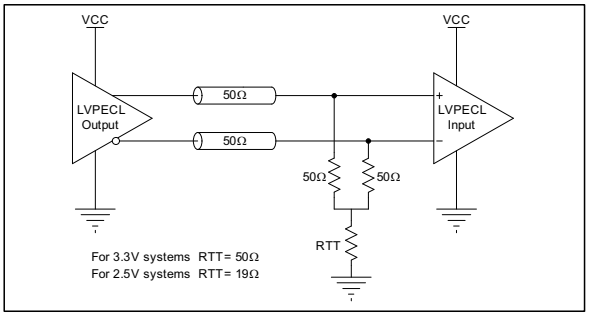


Figure 4: XR81102 Alternate LVPECL Output Termination Using Y-termination

Output Signal Timing Definitions

The following diagrams clarify the common definitions of the AC timing measurements.

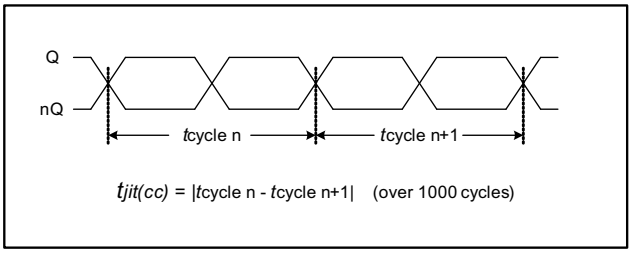


Figure 5: Cycle-to-Cycle Jitter

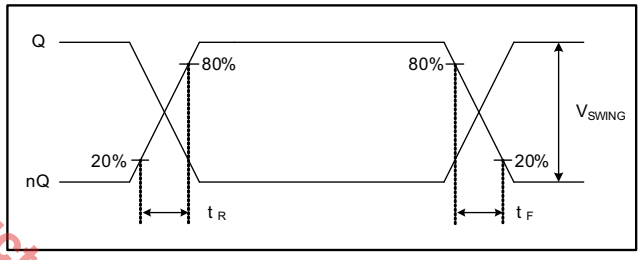


Figure 6: Output Rise/Fall Time and Swing

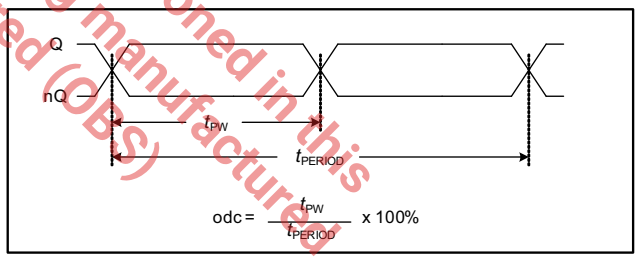
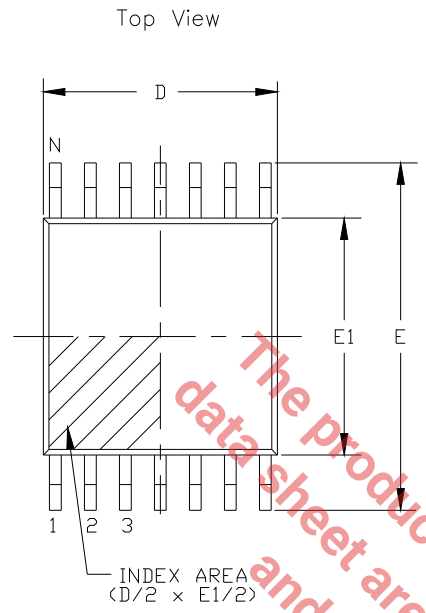


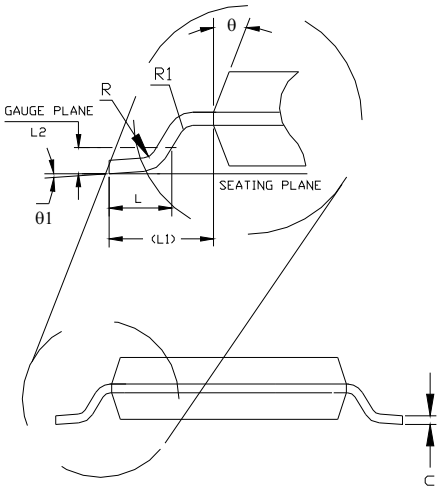
Figure 7: Output Period and Duty Cycle

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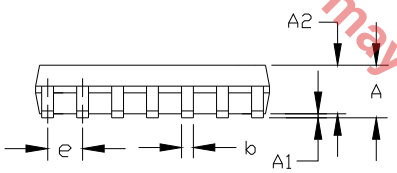
Mechanical Dimensions

8-Pin TSSOP





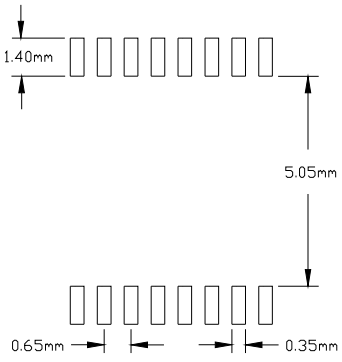
Front View



Side View

8-Pin TSSOP JEDEC MO-153 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.05	—	0.15	0.002	—	0.006
A2	0.85	0.90	0.95	0.033	0.035	0.037
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R	0.09	—	—	0.035	—	—
R1	0.09	—	—	0.035	—	—
θ	12° REF			12° REF		
θ1	0°	—	8°	0°	—	8°
D	2.90	3.00	3.10	0.114	0.118	0.122
N	8			8		

RECOMMENDED PCB LAND PATTERN



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Note : The side, top and landing pattern drawings are general to TSSOP packaging but the table is specific to the 8pin TSSOP

Ordering Information

Part Number	Package	Green	Operating Temperature Range	Shipping Packaging	Marking
XR81102-CA02-F	8-pin TSSOP	Yes	-40°C to +85°C	Tube	T02
XR81102-CA02TR-F	8-pin TSSOP	Yes	-40°C to +85°C	Tape & Reel	T02
XR81102EVB	Eval Board	N/A	N/A	N/A	N/A

Revision History

Revision	Date	Description
1A	April 2014	Initial release.
1B	April 28, 2014	Update to general description. [ECN1421-16 I 05/25/2014]

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