PRELIMINARY DATA SHEET

# Si53212, Si53208, Si53204: 12/8/4-Output PCI-Express Low Jitter, Low Power Gen 1 to Gen 7 Clock Buffer

## Applications

- Data centers
- Servers
- Storage
- PCIe add-on cards
- Communications
- Industrial

## Key Features

- 4, 8, and 12 Output 100 MHz PCIe Gen1 through Gen 7, compliant clock fanout buffer
- Low additive jitter: 0.02 ps rms max, Gen 6
- Low-power, push-pull, HCSL compatible differential outputs
- 10 MHz to 200 MHz clock input
- Individual hardware control pins and I2C controls for Output Enable
- Spread spectrum tolerant to pass through a spread input clock for EMI reduction
- Supports Intel QPI/UPI standards
- Single 1.5 to 1.8 V power supply
- Internal 100 Ω or 85 Ω output impedance matching
- Adjustable output slew rate
- Temperature range: –40 °C to 85 °C
- Small QFN package options:
  - 64-pin QFN (9 x 9 mm): 12 Output
  - 48-pin QFN (6 x 6 mm): 8 Output
  - 32-pin QFN (5 x 5 mm): 4 Output
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

## Description

The Si53212, Si53208, and Si53204 are the industry's highest performance, low additive jitter, low power PCIe clock fanout buffer family that can source 4, 8, or 12 clock outputs. All differential clock outputs are compliant to PCIe Gen 1 through Gen 7 common clock and separate reference clock specifications.

This family of buffers is spread spectrum tolerant to pass through a spread input clock. Each device has an individual hardware output enable control pin for enabling and disabling each differential output. The device can also support input frequencies from 10 MHz to 200 MHz. All the devices are packaged in small QFN packages. The small footprint and low-power consumption make this family of PCIe clock fanout buffers ideal for industrial and consumer applications.

To confirm PCI-Express compliance, the Skyworks PCIe Clock Jitter Tool makes measuring PCIe clock jitter quick and easy. Download it free: https://www.skyworksinc.com/en/Application-Pages/pcie-clock-jitter-tool.

## 1. Feature List

- 12/8/4-output 100 MHz PCIe Gen 1 through Gen 7 CC and separate reference clock compliant clock fanout buffer
- Low-power, push-pull, HCSL compatible differential outputs from 10 MHz to 200 MHz clock input
- Low additive jitter of 0.02 ps rms max to meet PCIe Gen 7 specifications
- Individual hardware control pins and I2C for Output Enable to easily disable unused outputs for power savings
- Spread spectrum tolerant to pass through a spread input clock for EMI reduction
- Supports Intel QPI/UPI jitter requirements with margin
- Internal 100 Ω or 85 Ω output impedance matching
- Eliminates external termination resistors to reduce board space
- Adjustable slew rate to improve signal quality for different applications and board designs
- Single 1.5 to 1.8 V power supply
- Temperature range: –40°C to 85°C
- Package options:
  - 64-pin QFN (9 x 9 mm), 12-output
  - 48-pin QFN (6 x 6 mm), 8-output
  - 32-pin QFN (5 x 5 mm), 4-output
- Pb-free, RoHS-6 compliant

## 2. Functional Block Diagrams

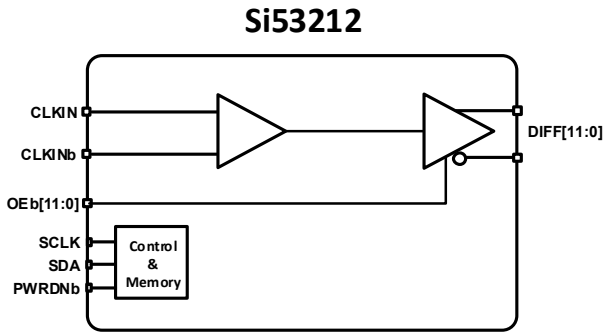


Figure 1. Si53212 Block Diagram

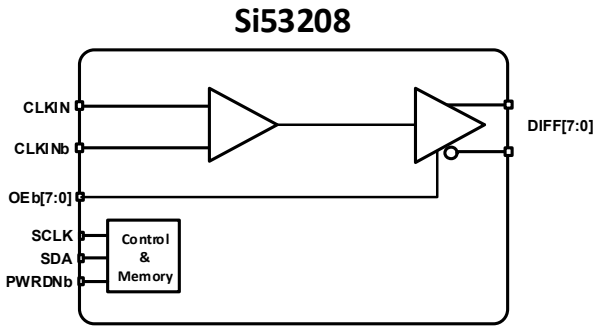


Figure 2. Si53208 Block Diagram

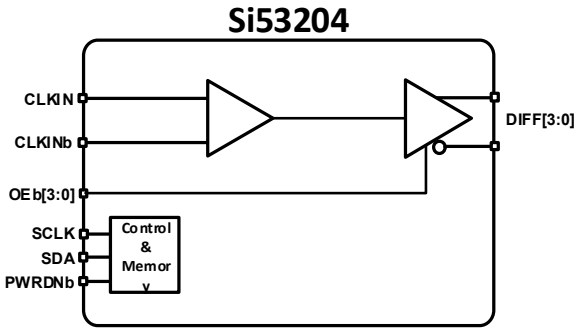


Figure 3. Si53204 Block Diagram

# 3. Pin Descriptions

## 3.1. Si523212 Pin Descriptions

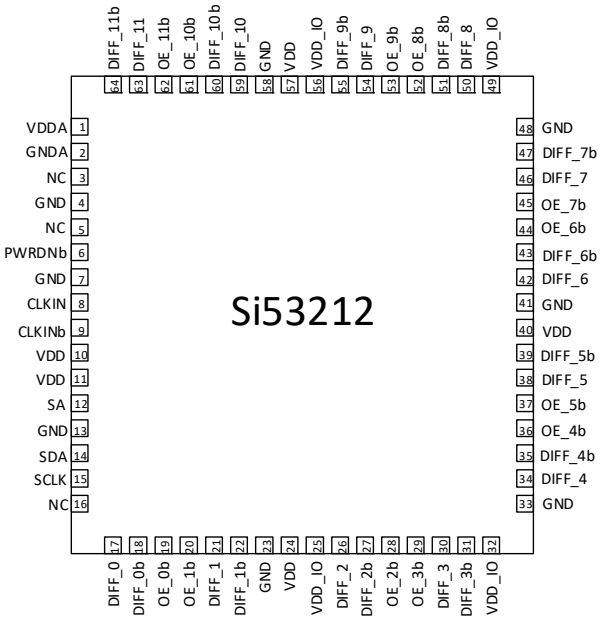


**Figure 4. Si53212 64-Pin QFN Pinout**

**Table 1. Si53212 Signal Descriptions**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1 | VDDA | PWR | Analog power supply |
| 2 | GNDA | GND | Analog ground |
| 3 | NC | NC | No connection |
| 4 | GND | GND | Ground |
| 5 | NC | NC | No connection |
| 6 | PWRDNb | I | Active low input pin asserts power down (PWRDNb) and disables all outputs (This pin has an internal 100 kΩ pull-up). |
| 7 | GND | GND | Ground |
| 8 | CLKIN | I | Clock input |
| 9 | CLKINb | I | Complementary clock input |
| 10 | VDD | PWR | Power supply |
| 11 | VDD | PWR | Power supply |
| 12 | SA | I | Address select for $I^2C$ (this pin has an internal 60 kΩ pull-up) |
| 13 | GND | GND | Ground |
| 14 | SDA | I/O | $I^2C$ compatible SDATA |

**Table 1. Si53212 Signal Descriptions (Continued)**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 15 | SCLK | I | $I^2C$ compatible SCLOCK |
| 16 | NC | NC | No connect |
| 17 | DIFF_0 | O, DIF | HCSL DIFF_0, true |
| 18 | DIFF_0b | O, DIF | HCSL DIFF_0, complement |
| 19 | OE_0b | I, PD | Output enable for DIFF_0 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs |
| 20 | OE_1b | I, PD | Output enable for DIFF_1 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs |
| 21 | DIFF_1 | O, DIF | HCSL DIFF_1, true |
| 22 | DIFF_1b | O, DIF | HCSL DIFF_1, complement |
| 23 | GND | GND | Ground |
| 24 | VDD | PWR | Power supply |
| 25 | VDD_IO | PWR | Output power supply |
| 26 | DIFF_2 | O, DIF | HCSL DIFF_2, true |
| 27 | DIFF_2b | O, DIF | HCSL DIFF_2, complement |
| 28 | OE_2b | I, PD | Output enable for DIFF_2 pair (This pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 29 | OE_3b | I, PD | Output enable for DIFF_3 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 30 | DIFF_3 | O, DIF | HCSL DIFF_3, true |
| 31 | DIFF_3b | O, DIF | HCSL DIFF_3, complement |
| 32 | VDD_IO | PWR | Output power supply |
| 33 | GND | GND | Ground |
| 34 | DIFF_4 | O, DIF | HCSL DIFF_4, true |
| 35 | DIFF_4b | O, DIF | HCSL DIFF_4, complement |
| 36 | OE_4b | I, PD | Output enable for DIFF_4 pair (This pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 37 | OE_5b | I, PD | Output enable for DIFF_5 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 38 | DIFF_5 | O, DIF | HCSL DIFF_5, true |
| 39 | DIFF_5b | O, DIF | HCSL DIFF_5, complement |
| 40 | VDD | PWR | Power supply |
| 41 | GND | GND | Ground |
| 42 | DIFF_6 | O, DIF | HCSL DIFF_6, true |
| 43 | DIFF_6b | O, DIF | HCSL DIFF_6, complement |
| 44 | OE_6b | I, PD | Output enable for DIFF_6 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 45 | OE_7b | I, PD | Output enable for DIFF_7 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 46 | DIFF_7 | O, DIF | HCSL DIFF_7, true |
| 47 | DIFF_7b | O, DIF | HCSL DIFF_7, complement |
| 48 | GND | GND | Ground |
| 49 | VDD_IO | PWR | Output power supply |
| 50 | DIFF_8 | O, DIF | HCSL DIFF_8, true |

**Table 1. Si53212 Signal Descriptions (Continued)**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 51 | DIFF_8b | O, DIF | HCSL DIFF_8, complement |
| 52 | OE_8b | I, PD | Output enable for DIFF_8 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 53 | OE_9b | I, PD | Output enable for DIFF_9 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 54 | DIFF_9 | O, DIF | HCSL DIFF_9, true |
| 55 | DIFF_9b | O, DIF | HCSL DIFF_9, complement |
| 56 | VDD_IO | PWR | Output power supply |
| 57 | VDD | PWR | Power supply |
| 58 | GND | GND | Ground |
| 59 | DIFF_10 | O, DIF | HCSL DIFF_10, true |
| 60 | DIFF_10b | O, DIF | HCSL DIFF_10, complement |
| 61 | OE_10b | I, PD | Output enable for DIFF_10 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 62 | OE_11b | I, PD | Output enable for DIFF_11 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 63 | DIFF_11 | O, DIF | HCSL DIFF_11, true |
| 64 | DIFF_11b | O, DIF | HCSL DIFF_11, complement |
| | GND PAD | GND | The ground pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible. |

## 3.2. Si53208 Pin Descriptions

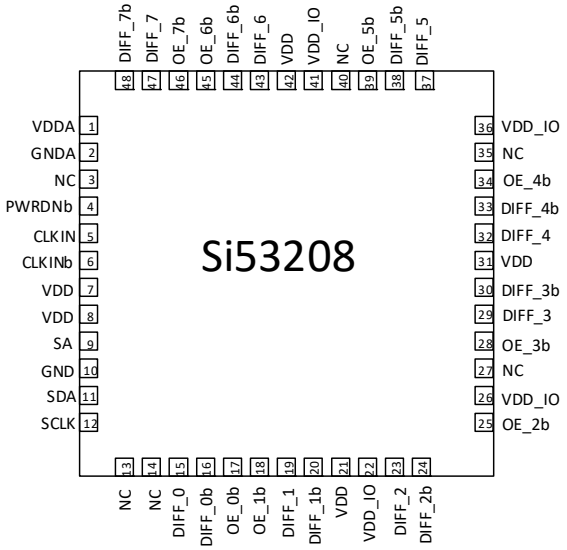


**Figure 5. Si53208 48-pin QFN Pinout**

**Table 2. Si53208 Signal Descriptions**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | VDDA | PWR | Analog power supply |
| 2 | GNDA | PWR | Analog ground |
| 3 | NC | NC | No connection |
| 4 | PWRDNb | I | Active low input pin asserts power down (PWRDNb) and disables all outputs (this pin has an internal 100 kΩ pull-up) |
| 5 | CLKIN | I | Clock input |
| 6 | CLKINb | I | Complementary clock input |
| 7 | VDD | PWR | Power supply |
| 8 | VDD | PWR | Power supply |
| 9 | SA | I | Address select for $I^2C$ (this pin has an internal 60 kΩ pull-up) |
| 10 | GND | GND | Ground |
| 11 | SDA | I/O | $I^2C$ compatible SDATA |
| 12 | SCLK | I | $I^2C$ compatible SCLOCK |
| 13 | NC | NC | No connection |
| 14 | NC | NC | No connection |
| 15 | DIFF_0 | O, DIF | HCSL DIFF_0, true |
| 16 | DIFF_0b | O, DIF | HCSL DIFF_0, complement |
| 17 | OE_0b | I, PD | Output enable for DIFF_0 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 18 | OE_1b | I, PD | Output enable for DIFF_1 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 19 | DIFF_1 | O, DIF | HCSL DIFF_1, true |
| 20 | DIFF_1b | O, DIF | HCSL DIFF_1, complement |
| 21 | VDD | PWR | Power supply |
| 22 | VDD_IO | PWR | Output power supply |
| 23 | DIFF_2 | O, DIF | HCSL DIFF_2, true |
| 24 | DIFF_2b | O, DIF | HCSL DIFF_2, complement |
| 25 | OE_2b | I, PD | Output enable for DIFF_2 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 26 | VDD_IO | PWR | Output power supply |
| 27 | NC | NC | No connection |
| 28 | OE_3b | I, PD | Output enable for DIFF_3 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 29 | DIFF_3 | O, DIF | HCSL DIFF_3, true |
| 30 | DIFF_3b | O, DIF | HCSL DIFF_3, complement |
| 31 | VDD | PWR | Power supply |
| 32 | DIFF_4 | O, DIF | HCSL DIFF_4, true |
| 33 | DIFF_4b | O, DIF | HCSL DIFF_4, complement |
| 34 | OE_4b | I, PD | Output enable for DIFF_4 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 35 | NC | NC | No connection |

**Table 2. Si53208 Signal Descriptions (Continued)**

| Pin | Name | Type | Description |
|---|---|---|---|
| 36 | VDD_IO | PWR | Output power supply |
| 37 | DIFF_5 | O, DIF | HCSL DIFF_5, true |
| 38 | DIFF_5b | O, DIF | HCSL DIFF_5, complement |
| 39 | OE_5b | I, PD | Output enable for DIFF_5 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 40 | NC | NC | No connection |
| 41 | VDD_IO | PWR | Output power supply |
| 42 | VDD | PWR | Power supply |
| 43 | DIFF_6 | O, DIF | HCSL DIFF_6, true |
| 44 | DIFF_6b | O, DIF | HCSL DIFF_6, complement |
| 45 | OE_6b | I, PD | Output enable for DIFF_6 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 46 | OE_7b | I, PD | Output enable for DIFF_7 pair (This pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 47 | DIFF_7 | O, DIF | HCSL DIFF_7, true |
| 48 | DIFF_7b | O, DIF | HCSL DIFF_7, complement |
|  | GND PAD | GND | The ground pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible. |

## 3.3. Si53204 Pin Descriptions

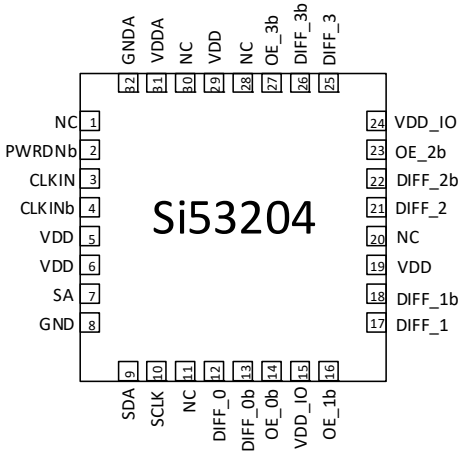


**Figure 6. Si53204 32-pin QFN Pinout**

**Table 3. Si53204 Signal Descriptions**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1 | NC | NC | No connection |
| 2 | PWRDNb | I | Active low input pin asserts power down (PWRDNb) and disables all outputs (this pin has an internal 100 kΩ pull-up) |
| 3 | CLKIN | I | Clock input |
| 4 | CLKINb | I | Complementary clock input |
| 5 | VDD | PWR | Power supplyl |
| 6 | VDD | PWR | Power supply |
| 7 | SA | I | Address select for $I^2C$ (this pin has an internal 60 kΩ pull-up) |
| 8 | GND | GND | Ground |
| 9 | SDA | I/O | $I^2C$ compatible SDATA |
| 10 | SCLK | I | $I^2C$ compatible SCLOCK |
| 11 | NC | NC | No connection |
| 12 | DIFF_0 | O, DIF | HCSL DIFF_0, true |
| 13 | DIFF_0b | O, DIF | HCSL DIFF_0, complement |
| 14 | OE_0b | I, PD | Output enable for DIFF_0 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 15 | VDD_IO | PWR | Output power supply |
| 16 | OE_1b | I, PD | Output enable for DIFF_1 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 17 | DIFF_1 | O, DIF | HCSL DIFF_1, true |
| 18 | DIFF_1b | O, DIF | HCSL DIFF_1, complement |
| 19 | VDD | PWR | Power supply |

**Table 3. Si53204 Signal Descriptions (Continued)**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 20 | NC | NC | No connection |
| 21 | DIFF_2 | O, DIF | HCSL DIFF_2, true |
| 22 | DIFF_2b | O, DIF | HCSL DIFF_2, complement |
| 23 | OE_2b | I, PD | Output enable for DIFF_2 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 24 | VDD_IO | PWR | Output power supply |
| 25 | DIFF_3 | O, DIF | HCSL DIFF_3, true |
| 26 | DIFF_3b | O, DIF | HCSL DIFF_3, complement |
| 27 | OE_3b | I, PD | Output enable for DIFF_3 pair (this pin has an internal 100 kΩ pull-down), 0 = Enable outputs; 1 = Disable outputs |
| 28 | NC | NC | No connection |
| 29 | VDD | PWR | Power supply |
| 30 | NC | NC | No connection |
| 31 | VDDA | PWR | Analog power supply |
| 32 | GNDA | PWR | Analog ground |
|  | GND PAD | GND | The ground pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible. |

# 4. Electrical Specifications

**Table 4. DC Electrical Specifications**
**(VDD = VDDA = 1.5 V ±5%)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1.5 V Operating voltage | VDD | 1.5 V ±5% | 1.425 | 1.5 | 1.575 | V |
| Output supply voltage | VDD_IO | Supply voltage for differential low power outputs | 0.9975 | 1.05 to 1.5 | 1.575 | V |
| 1.5 V Input high voltage | $V_{IH}$ | Control input pins | 0.75 VDD | — | VDD +0.3 | V |
| 1.5 V Input low voltage | $V_{IL}$ | Control input pins | –0.3 | — | 0.25 VDD | V |
| Input current | $I_{IN}$ | Single-ended inputs, VIN = GND, VIN = VDD | –5 | — | 5 | µA |
| | $I_{INP}$ | Single-ended inputs, VIN = 0 V, inputs with internal pull-up resistors VIN = VDD, inputs with internal pull-down resistors | –200 | — | 200 | µA |
| Input pin capacitance | $C_{IN}$ | | 1.5 | — | 5 | pF |
| Output pin capacitance | $C_{OUT}$ | | — | — | 6 | pF |
| Pin inductance | $L_{IN}$ | | — | — | 7 | nH |
| **Si53212 Current Consumption (VDD = VDDA = 1.5 V ±5%)** | | | | | | |
| Power down current | $I_{DD_PD_total}$ | | — | 1.3 | 1.7 | mA |
| | $I_{DD_PD}$ | VDD, except VDDA and VDD_IO, all outputs off | — | 0.4 | 0.75 | mA |
| | $I_{DD_APD}$ | VDDA, all outputs off | — | 0.6 | 0.75 | mA |
| | $I_{DD_IOPD}$ | VDD_IO, all outputs off | — | 0.3 | 0.5 | mA |
| Dynamic supply current | $I_{DD_1.5V_Total}$ | All outputs enabled. Differential clocks with 5” traces and 2 pF load. | — | 60 | 71.5 | mA |
| | $I_{DD_OP}$ | VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz | — | 12 | 13 | mA |
| | $I_{DD_AOP}$ | VDDA, all differential outputs active at 100 MHz | — | 2.2 | 2.6 | mA |
| | $I_{DD_IOOP}$ | VDD_IO, all differential outputs active at 100 MHz | — | 46 | 55.5 | mA |
| **Si53208 Current Consumption (VDD = VDDA = 1.5 V ±5%)** | | | | | | |
| Power down current | $I_{DD_PD_total}$ | | — | 1.3 | 1.7 | mA |
| | $I_{DD_PD}$ | VDD, except VDDA and VDD_IO, all outputs off | — | 0.4 | 0.75 | mA |
| | $I_{DD_APD}$ | VDDA, all outputs off | — | 0.6 | 0.75 | mA |
| | $I_{DD_IOPD}$ | VDD_IO, all outputs off | — | 0.3 | 0.5 | mA |
| Dynamic supply current | $I_{DD_1.5V_Total}$ | All outputs enabled. Differential clocks with 5” traces and 2 pF load. | — | 42 | 51.5 | mA |
| | $I_{DD_OP}$ | VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz | — | 10 | 11 | mA |
| | $I_{DD_AOP}$ | VDDA, all differential outputs active at 100 MHz | — | 2.2 | 2.6 | mA |
| | $I_{DD_IOOP}$ | VDD_IO, all differential outputs active at 100 MHz | — | 30 | 37.5 | mA |

**Table 4. DC Electrical Specifications (Continued)**
**(VDD = VDDA = 1.5 V ±5%)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Si53204 Current Consumption (VDD = VDDA = 1.5 V ±5%)** | | | | | | |
| Power down current | $I_{DD_PD_total}$ | | — | 1.3 | 1.7 | mA |
| | $I_{DD_PD}$ | VDD, except VDDA and VDD_IO, all outputs off | — | 0.4 | 0.75 | mA |
| | $I_{DD_APD}$ | VDDA, all outputs off | — | 0.6 | 0.75 | mA |
| | $I_{DD_IOPD}$ | VDD_IO, all outputs off | — | 0.3 | 0.5 | mA |
| Dynamic supply current | $I_{DD_1.8V_Total}$ | All outputs enabled. Differential clocks with 5” traces and 2 pF load. | — | 26 | 31.5 | mA |
| | $I_{DD_OP}$ | VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz | — | 8.5 | 9.5 | mA |
| | $I_{DD_AOP}$ | VDDA, all differential outputs active at 100 MHz | — | 2.2 | 2.6 | mA |
| | $I_{DD_IOOP}$ | VDD_IO, all differential outputs active at 100 MHz | — | 15.5 | 19 | mA |

**Table 5. DC Electrical Specifications**
**(VDD = VDDA = 1.8 V ±5%)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1.8 V Operating voltage | VDD | 1.8 V ±5% | 1.71 | 1.8 | 1.89 | V |
| Output supply voltage | VDD_IO | Supply voltage for differential low power outputs | 0.9975 | 1.05 to 1.8 | 1.9 | V |
| 1.8 V Input high voltage | $V_{IH}$ | Control input pins | 0.75 VDD | — | VDD +0.3 | V |
| 1.8 V Input low voltage | $V_{IL}$ | Control input pins | –0.3 | — | 0.25 VDD | V |
| Input current | $I_{IN}$ | Single-ended inputs, VIN = GND, VIN = VDD | –5 | — | 5 | µA |
| | $I_{INP}$ | Single-ended inputs, VIN = 0 V, inputs with internal pull-up resistors VIN = VDD, inputs with internal pull-down resistors | –200 | — | 200 | µA |
| Input pin capacitance | $C_{IN}$ | | 1.5 | — | 5 | pF |
| Output pin capacitance | $C_{OUT}$ | | — | — | 6 | pF |
| Pin inductance | $L_{IN}$ | | — | — | 7 | nH |
| **Si53212 Current Consumption (VDD = VDDA = 1.8 V ±5%)** | | | | | | |
| Power down current | $I_{DD_PD_total}$ | | — | 1.4 | 2.7 | mA |
| | $I_{DD_PD}$ | VDD, except VDDA and VDD_IO, all outputs off | — | 0.5 | 1.7 | mA |
| | $I_{DD_APD}$ | VDDA, all outputs off | — | 0.6 | 0.75 | mA |
| | $I_{DD_IOPD}$ | VDD_IO, all outputs off | — | 0.3 | 0.65 | mA |

**Table 5. DC Electrical Specifications (Continued)**
**(VDD = VDDA = 1.8 V ±5%)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Dynamic supply current | $I_{DD_1.8V_Total}$ | All outputs enabled. Differential clocks with 5” traces and 2 pF load | — | 61 | 74 | mA |
| | $I_{DD_OP}$ | VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz | — | 12 | 14.5 | mA |
| | $I_{DD_AOP}$ | VDDA, all differential outputs active at 100 MHz | — | 2.2 | 2.6 | mA |
| | $I_{DD_IOOP}$ | VDD_IO, all differential outputs active at 100 MHz | — | 47 | 56.5 | mA |
| **Si53208 Current Consumption (VDD = VDDA = 1.8 V ±5%)** | | | | | | |
| Power down current | $I_{DD_PD_total}$ | | — | 1.4 | 2.7 | mA |
| | $I_{DD_PD}$ | VDD, except VDDA and VDD_IO, all outputs off | — | 0.5 | 1.7 | mA |
| | $I_{DD_APD}$ | VDDA, all outputs off | — | 0.6 | 0.75 | mA |
| | $I_{DD_IOPD}$ | VDD_IO, all outputs off | — | 0.3 | 0.65 | mA |
| Dynamic supply current | $I_{DD_1.8V_Total}$ | All outputs enabled. Differential clocks with 5” traces and 2 pF load | — | 44 | 53.5 | mA |
| | $I_{DD_OP}$ | VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz | — | 10.5 | 12.5 | mA |
| | $I_{DD_AOP}$ | VDDA, all differential outputs active at 100 MHz | — | 2.2 | 2.6 | mA |
| | $I_{DD_IOOP}$ | VDD_IO, all differential outputs active at 100 MHz | — | 31 | 38 | mA |
| **Si53204 Current Consumption (VDD = VDDA = 1.8 V ±5%)** | | | | | | |
| Power down current | $I_{DD_PD_total}$ | | — | 1.4 | 2.7 | mA |
| | $I_{DD_PD}$ | VDD, except VDDA and VDD_IO, all outputs off | — | 0.5 | 1.7 | mA |
| | $I_{DD_APD}$ | VDDA, all outputs off | — | 0.6 | 0.75 | mA |
| | $I_{DD_IOPD}$ | VDD_IO, all outputs off | — | 0.3 | 0.65 | mA |
| Dynamic supply current | $I_{DD_1.8V_Total}$ | All outputs enabled. Differential clocks with 5” traces and 2 pF load | — | 27 | 33 | mA |
| | $I_{DD_OP}$ | VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz | — | 9 | 10.5 | mA |
| | $I_{DD_AOP}$ | VDDA, all differential outputs active at 100 MHz | — | 2.2 | 2.6 | mA |
| | $I_{DD_IOOP}$ | VDD_IO, all differential outputs active at 100 MHz | — | 16 | 19.5 | mA |

**Table 6. AC Electrical Specifications[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CLKIN frequency range | | | 10 | — | 200 | MHz |
| CLKIN rising and falling slew rate | CLKIN_$T_R$_$T_F$ | Single-ended measurement: VOL = 0.175 to VOH = 0.525 V (Averaged) | 0.6 | — | 4 | V/ns |
| Differential input high voltage | $V_{IH}$ | | 150 | — | — | mV |
| Differential input low voltage | $V_{IL}$ | | — | — | –150 | mV |
| Crossing point voltage | $V_{OX}$ | Single-ended measurement | 250 | — | 550 | mV |
| Crossing point voltage (var) | $V_{OX_DELTA}$ | Single-ended measurement | — | — | 140 | mV |
| Differential ringback voltage | $V_{RB}$ | | –100 | — | 100 | mV |
| Time before ringback voltage | $T_{STABLE_RB}$ | | 500 | — | — | ps |
| Absolute maximum input voltage | $V_{MAX}$ | | — | — | 1150 | mV |
| Absolute minimum input voltage | $V_{MIN}$ | | –300 | — | — | mV |
| Duty cycle for each clock output signal in a given differential pair | $T_{DC}$ | Measured at crossing point $V_{OX}$ | 45 | — | 55 | % |
| Rise/fall matching | $T_{FRM}$ | Determined as a fraction of 2 x ($T_R$ - $T_F$)($T_R$ + $T_F$) | — | — | 20 | % |
| **Control Input Pins** | | | | | | |
| Trise | $T_R$ | Rise time of single-ended control inputs | — | — | 5 | ns |
| Tfall | $T_F$ | Fall time of single-ended control inputs | — | — | 5 | ns |
| **DIFF HCSL** | | | | | | |
| Output-to-output skew | TSKEW | Measured at 0 V differential | — | — | 50 | ps |
| Additive cycle-to-cycle jitter | JADD_CCJ | Measured at 0 V differential | — | 14 | 20 | ps |
| Additive phase jitter | JADD | 12 kHz to 20 MHz | | — | 0.21 | ps (RMS) |
| 100 MHz PCIe common-clock additive jitter performance[2] | JADD_PK-PK | PCIe Gen 1 (2.5 GT/s) | | 10 | 17 | ps (pk-pk) |
| | JADD_GEN2 | PCIe Gen 2 (5.0GT/s), 10 kHz < F < 1.5 MHz | | 0.125 | 0.2 | ps (RMS) |
| | | PCIe Gen 2 (5.0GT/s), 1.5 MHz < F < Nyquist | | 0.003 | 0.005 | ps (RMS) |
| | JADD_GEN3 | PCIe Gen 3 (8GT/s) | | 0.04 | 0.06 | ps (RMS) |
| | JADD_GEN4 | PCIe Gen 4 (16GT/s) | | 0.04 | 0.06 | ps (RMS) |
| | JADD_GEN5 | PCIe Gen 5 (32GT/s) | | 0.015 | 0.021 | ps (RMS) |
| | JADD_GEN6 | PCIe Gen 6 (64GT/s) | | 0.015 | 0.02 | ps (RMS) |
| | JADD_GEN7 | PCIe Gen 7 (128GT/s) | | 0.0105 | 0.014 | ps (RMS) |
| 100 MHz PCIe separate reference clock additive jitter performance[2] | JADD_GEN3_SR | PCIe Gen 3 (8GT/s) | | 0.035 | 0.043 | ps (RMS) |
| | JADD_GEN4_SR | PCIe Gen 4 (16GT/s) | | 0.035 | 0.043 | ps (RMS) |
| | JADD_GEN5_SR | PCIe Gen 5 (32GT/s) | | 0.02 | 0.03 | ps (RMS) |
| | JADD_GEN6_SR | PCIe Gen 6 (64GT/s) | | 0.015 | 0.02 | ps (RMS) |
| | JADD_GEN7_SR | PCIe Gen 7 (128GT/s) | | 0.0105 | 0.014 | ps (RMS) |

**Table 6. AC Electrical Specifications[1] (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Slew rate[2] | $T_R/T_F$ | Measured differentially from ±150 mV (fast setting) | — | 2.4 | 3.7 | V/ns |
| | | Measured differentially from ±150 mV (slow setting) | — | 1.9 | 2.9 | V/ns |
| Slew rate matching | $\Delta T_R/T_F$ | | — | — | 10 | % |
| Voltage high | $V_{HIGH}$ | | 600 | — | 850 | mV |
| Voltage low | $V_{LOW}$ | | –150 | — | 150 | mV |
| Max voltage | $V_{MAX}$ | | — | — | 1150 | mV |
| Min voltage | $V_{MIN}$ | | –300 | — | — | mV |
| **Enable/Disable and Setup** | | | | | | |
| Clock stabilization from power-up | $T_{STABLE}$ | Minimum ramp rate 200 V/s | — | 1 | 5 | ms |
| OE_b latency | $T_{OEb_LAT}$ | Differential outputs start after OE_b assertion, differential outputs stop after OE_b deassertion | — | 2 | 3.5 | clocks |
| PWRDNb latency to differential outputs enable | $T_{PWRDNb}$ | Differential outputs enable after PD_b deassertion | — | 490 | 520 | µs |
| **Intel QPI Specifications for 100 MHz and 133 MHz** | | | | | | |
| Intel QPI and SMI REFCLK additive jitter[3] | $J_{ADD_QPI_SMI}$ | 4.8 Gb/s, 133 MHz, 12UI, 7.8 M | — | 0.16 | — | ps (RMS) |
| | | 6.4 Gb/s, 133 MHz, 12UI, 7.8 M | — | 0.12 | — | ps (RMS) |
| Intel QPI and SMI REFCLK additive jitter[5] | $J_{ADD_SQPI_SMI}$ | 8 Gb/s, 100 MHz, 12 UI | — | 0.09 | — | ps (RMS) |
| Intel QPI and SMI REFCLK additive jitter[5] | $J_{ADD_QPI_SMI}$ | 9.6 Gb/s, 100 MHz, 12UI | — | 0.07 | — | ps (RMS) |
| **Intel UPI Specifications for 100 MHz** | | | | | | |
| UPI Additive Phase Jitter | $J_{ADD_UPI}$ | Intel UPI 1–10 MHz | — | 0.67 | 1 | ps |

1. Skyworks PCIe Clock Jitter Tool is used to obtain measurements for additive phase jitter. Additive Phase Jitter = sqrt (output jitter^2 - input jitter^2). Input used is 100 MHz from Si5340.
2. Input clock slew rate of 3.0 V/ns used for jitter measurements.
3. Post processed evaluation through Intel supplied Matlab scripts, using Intel PCIe Clock Jitter Tool. Measuring on 100 MHz output using the template file in the Intel PCIe Clock Jitter Tool. Measuring on 100 MHz, 133 MHz outputs using the template file in the Intel PCIe Jitter Tool.

**Table 7. Thermal Conditions**

| Parameter | Symbol | Test Condition | Value | Units |
|---|---|---|---|---|
| **Si53204 – 32-QFN[1]** | | | | |
| Thermal resistance, junction to ambient | $\theta_{JA}$ | Still Air | 50.3 | °C/W |
| | | Air Flow 1 m/s | 47 | |
| | | Air Flow 2 m/s | 45.6 | |
| Thermal resistance, junction to case | $\theta_{JC}$ | | 10.3 | °C/W |
| Thermal resistance, junction to board | $\theta_{JB}$ | | 30.9 | °C/W |
| Calculation parameter, junction to top center | $\Psi_{JT}$ | | 2.3 | °C/W |
| Calculation parameter, junction to board | $\Psi_{JB}$ | | 30.9 | °C/W |
| **Si53208 – 48-QFN[2]** | | | | |
| Thermal resistance, junction to ambient | $\theta_{JA}$ | Still Air | 27.9 | °C/W |
| | | Air Flow 1 m/s | 24.5 | |
| | | Air Flow 2 m/s | 23.5 | |
| Thermal resistance, junction to case | $\theta_{JC}$ | | 17 | °C/W |
| Thermal resistance, junction to board | $\theta_{JB}$ | | 13.4 | °C/W |
| Calculation parameter, junction to top center | $\Psi_{JT}$ | | 0.5 | °C/W |
| Calculation parameter, junction to board | $\Psi_{JB}$ | | 13.1 | °C/W |
| **Si53212 – 64-QFN[3]** | | | | |
| Thermal resistance, junction to ambient | $\theta_{JA}$ | Still Air | 27.2 | °C/W |
| | | Air Flow 1 m/s | 23.9 | |
| | | Air Flow 2 m/s | 22.5 | |
| Thermal resistance, junction to case | $\theta_{JC}$ | | 13.7 | °C/W |
| Thermal resistance, junction to board | $\theta_{JB}$ | | 14.4 | °C/W |
| Calculation parameter, junction to top center | $\Psi_{JT}$ | | 0.5 | °C/W |
| Calculation parameter, junction to board | $\Psi_{JB}$ | | 14.2 | °C/W |

1. Based on a PCB with a dimension of 3" x 4.5", PCB thickness of 1.6 mm, and PCB center land with 4 via to top plane.
2. Based on 4 layer PCB with a dimension of 3" x 4.5", PCB thickness of 1.6 mm, and PCB center land with 9 via to top plane.
3. Based on 4 Layer PCB with a dimension of 3" x 4.5", PCB thickness of 1.6 mm, and PCB center land with 25 via to top plane.

**Table 8. Absolute Maximum Conditions[1] [2]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Main supply voltage | $V_{DD_1.8V}$ | Functional | — | — | 2.5 | V |
| Input voltage | $V_{IN}$ | Relative to VSS | –0.5 | — | VDD + 0.5 | V |
| Input high voltage $i^2c$ | $V_{IH_I2C}$ | SDATA and SCLK | — | | 3.6 | V |
| Temperature, storage | $T_S$ | Non-functional | –65 | — | 150 | Celsius |
| Temperature, operating ambient | $T_A$ | Functional | –40 | — | 85 | Celsius |
| Temperature, junction | $T_J$ | Functional | — | — | 125 | Celsius |
| ESD protection (human body model) | ESDHBM | JEDEC (JESD 22-A114) | –2000 | — | 2000 | V |
| Flammability rating | UL-94 | UL (Class) | V–0 | | | |

1. While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
2. Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***ESD Handling:*** *Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

# 5. Functional Description

## 5.1. OEb Pin

The OEb pin is an active low input used for synchronous stopping and starting the respective output clock while the rest of the device continues to function. By default, the OEb pin is set to logic low, and $I^2C$ OE bit is set to logic high. There are two methods to disable the output clock: the OEb pin is pulled to a logic high, or the $I^2C$ OE bit is set to a logic low. This pin has a 100 kΩ internal pull-down.

## 5.2. OEb Assertion

The assertion of the OEb function is achieved by pulling the OEb pin low while the $I^2C$ OE bit is high, which causes the respective stopped output to resume normal operation. No short or stretched clock pulses are produced when the clocks resume.

## 5.3. OEb Deassertion

The OEb function is deasserted by pulling the pin high or writing the $I^2C$ OE bit to a logic low. The corresponding output is stopped cleanly and the final output state is driven low.

## 5.4. SA Pin

The SA functionality sets the Slave Address of the part. This address is latched to the value of the pin when the part initially powers up. See Table 8.1 SA State on First Application of PWRDNb on page 24 for the available addresses. By default, the internal 60 kΩ pull-up resistor will set SA to a value of 1. Never directly connect the SA pin to VDD or GND. To drive the pin low or high, use a 10 kΩ resistor.

## 5.5. PWRDNb (Power Down) Pin

When PWRDNb is pulled low, the device will be placed in power down mode. The assertion and deasertion of PWRDNb is asynchronous. This pin has a 100 kΩ internal pull-up.

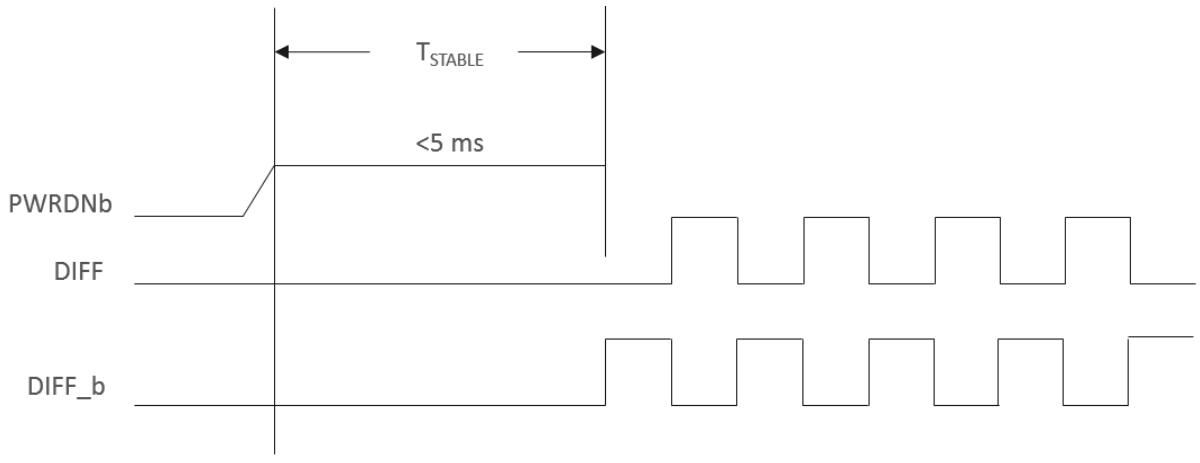


**Figure 7. Initial Sample High of PWRDNb After Power Up**

## 5.6. PWRDNb (Power Down) Assertion

The PWRDNb pin is an asynchronous active low input used to disable all output clocks in a glitch-free manner. In power down mode, all outputs and the $I^2C$ logic are disabled. All disabled outputs will be driven low.

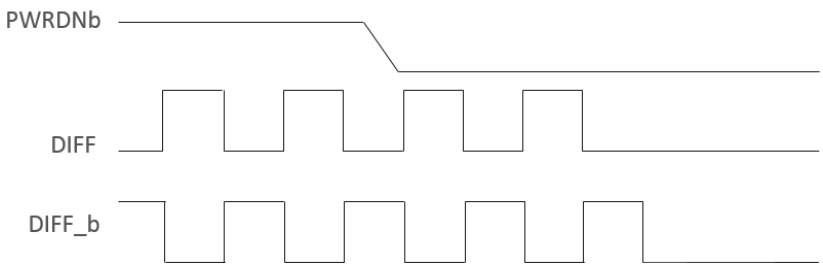


**Figure 8. PWRDNb Assertion**

## 5.7. PWRDNb (Power Down) Deassertion

When a valid rising edge on PWRGD/PWRDNb pin is applied, all outputs are enabled in a glitch-free manner within 520 µs.

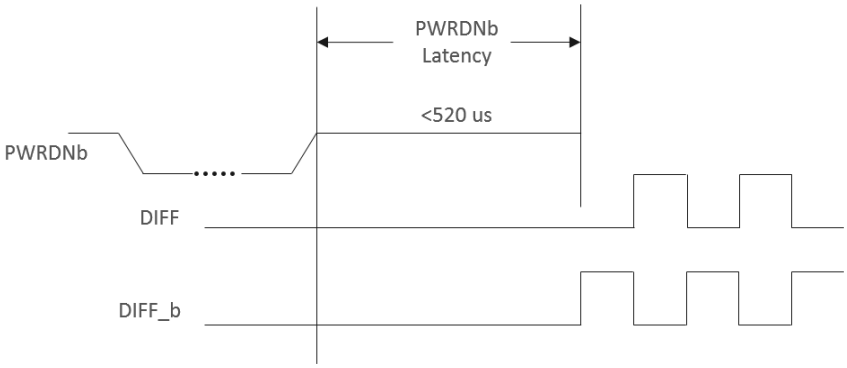


**Figure 9. Subsequent Deassertion of PWRDNb**

## 5.8. Power Supply Filtering Recommendations

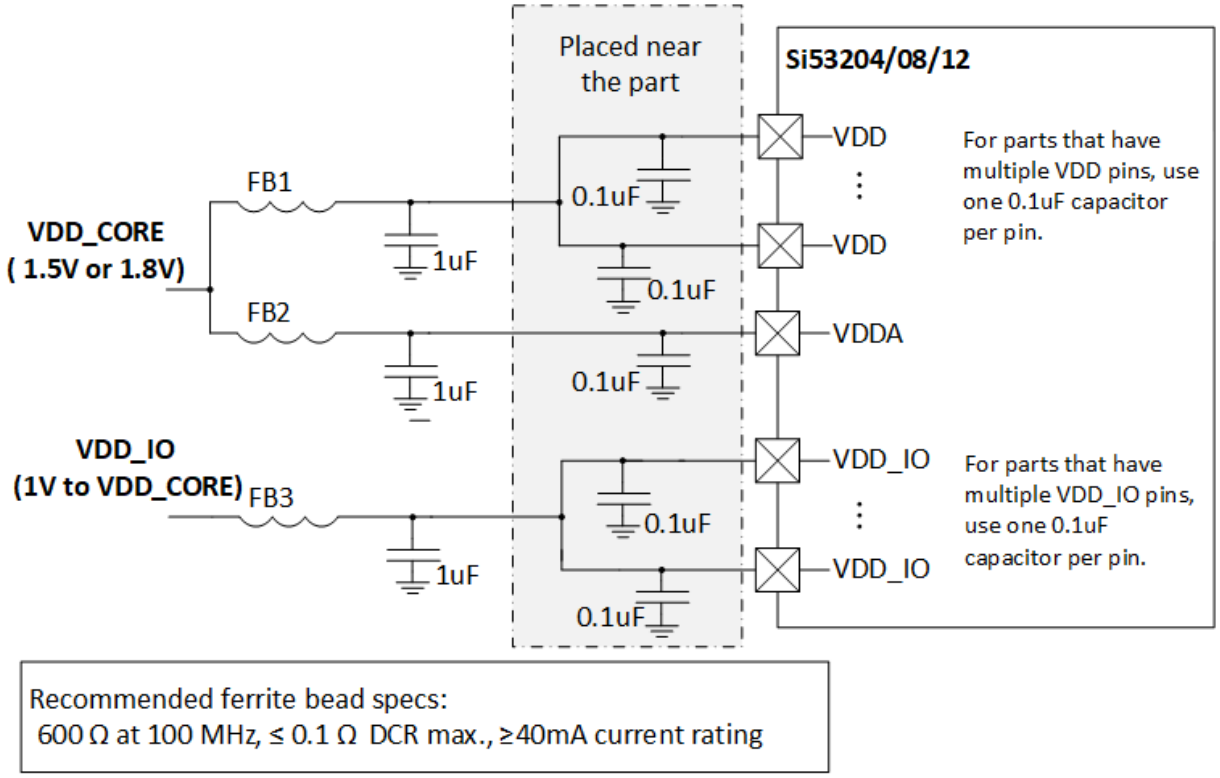


**Figure 10. Power Supply Filtering**

Separate out each type of VDD (VDD, VDDA, and VDD_IO) using ferrite beads. Then, for each VDD type, use one 1 uF bulk capacitor along with an additional 0.1 uF capacitor for each individual VDD pin. All VDD Core (VDD and VDDA) pins should be tied to the same voltage, either 1.8 V or 1.5 V. The VDD_IO pins can be tied to a voltage between 1 V and the selected VDD Core voltage.

**NOTE**: The VDD_IO pins must all be tied to the same voltage.

## 6. Test and Measurement Setup

The following diagrams show the test load configuration for the differential clock signals.

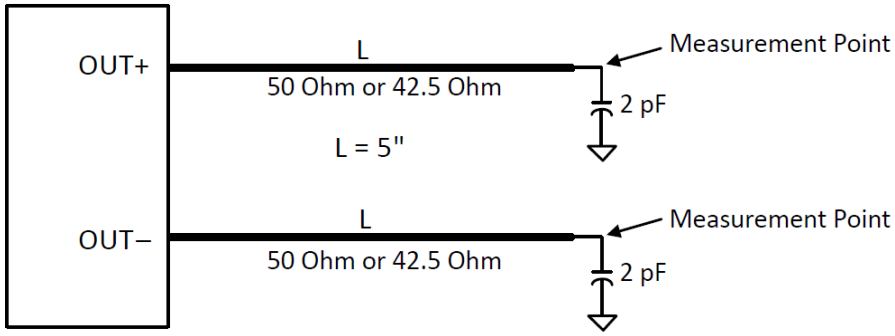


**Figure 11. 0.7 V Differential Load Configuration**

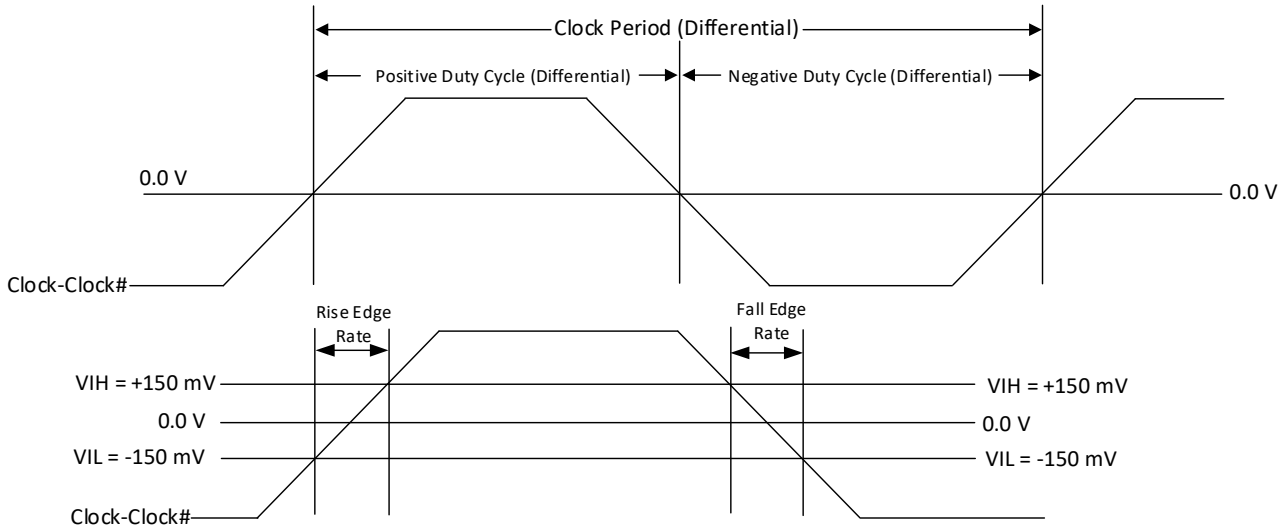


**Figure 12. Differential Measurement for Output Signals (for AC Parameters Measurement)**

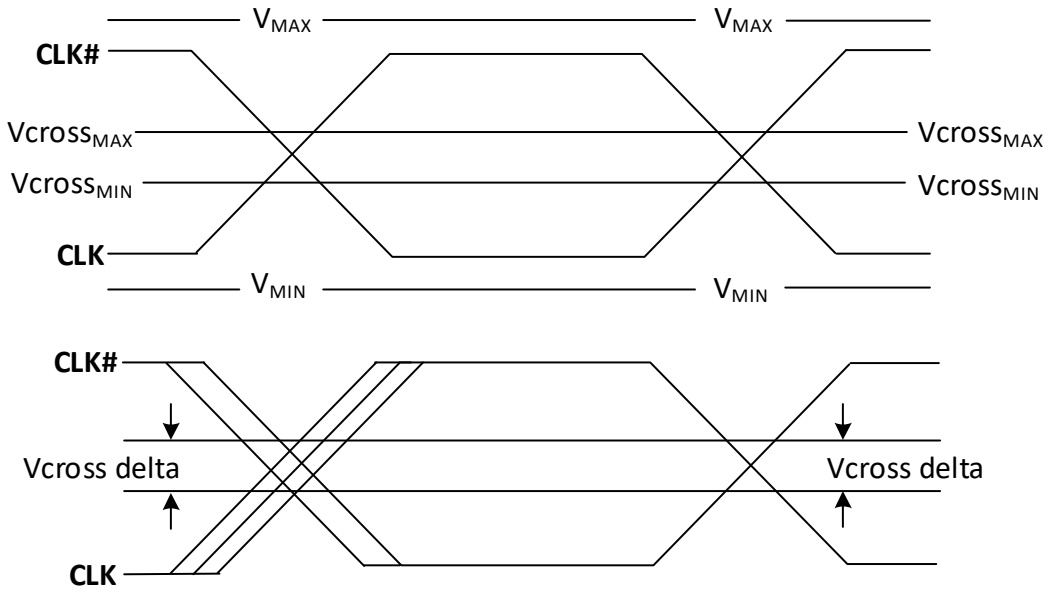


**Figure 13. Single-Ended Measurement for Differential Output Signals (for AC Parameters Measurement)**

## 7. PCIe Clock Jitter Tool

The PCIe Clock Jitter Tool is designed to enable users to quickly and easily take jitter measurements for PCIe Gen 1 through Gen 7 and common clock and separate reference clock. This software removes all the guesswork for PCIe Gen 1 through Gen 7 and SRNS/SRIS jitter measurements and margins in board designs. This software tool will provide accurate results in just a few clicks, and is provided in an executable format to support various common input waveform files, such as .csv, .wfm, and .bin. The easy-to-use GUI and helpful tips guide users through each step. Release notes and other documentation are also included in the software package.

Download it for free at Timing - PCI Express Learning Center.

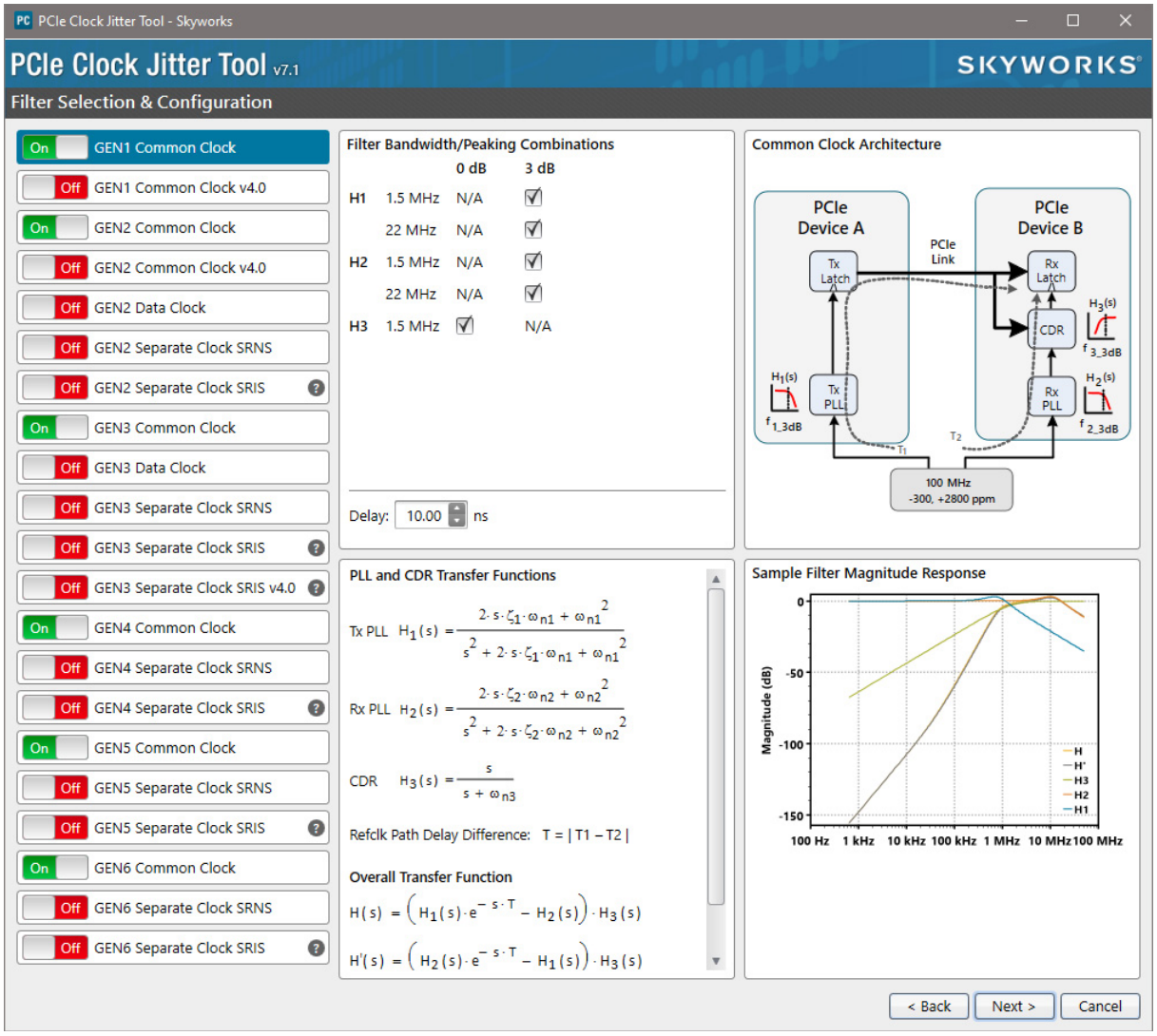


**Figure 14. PCIe Clock Jitter Tool**

# 8. Control Registers

## 8.1. I²C Interface

To enhance the flexibility and function of the clock synthesizer, an I²C interface is provided. Through the I2C interface, various device functions, such as individual clock output buffers, are individually enabled or disabled. The registers associated with the I²C interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

## 8.2. Block Read/Write

The clock driver I²C protocol accepts block write and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. The block write and block read protocol is outlined in Table 10.

## 8.3. Block Read

After the slave address is sent with the R/W condition bit set, the command byte is sent with the MSB = 0. The slave acknowledges the register index in the command byte. The master sends a repeat start function. After the slave acknowledges this, the slave sends the number of bytes it wants to transfer (>0 and <7). The master acknowledges each byte except the last and sends a stop condition.

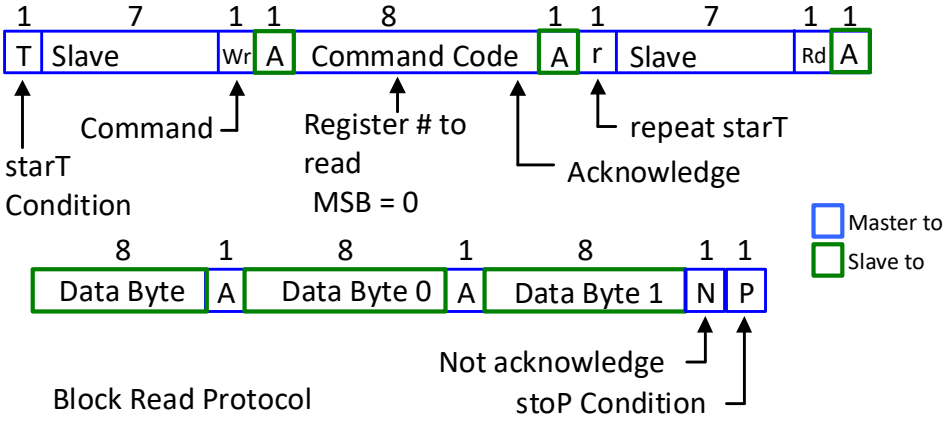


**Figure 15. Block Read Protocol**

## 8.4. Block Write

After the slave address is sent with the R/W condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate the register at which to start the transfer. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a block write must be the count of bytes that the master will transfer to the slave device. The byte count must be greater than zero and less than 7. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the Ack and the master sends a stop function.

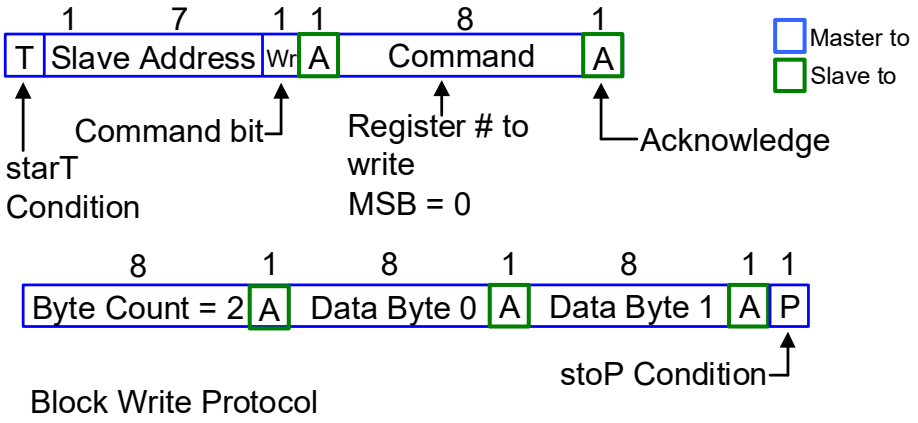


**Figure 16. Block Write Protocol**

## 8.5. Byte Read/Write

Reading or writing a register in an $I^2C$ slave device in byte mode always involves specifying the register number. Refer to Table XX Byte Read and Byte Write Protocol for byte read and byte write protocol.

## 8.6. Byte Read

The standard byte read is as shown in the figure below. It is an extension of the byte write. The write start condition is repeated; then, the slave device starts sending data, and the master acknowledges it until the last byte is sent. The master terminates the transfer with a Nack, then a stop condition. For byte operation, the MSB bit of the command byte must be set. For block operations, the MSB bit must be set low. If the bit is not set low, the next byte must be the byte transfer count.

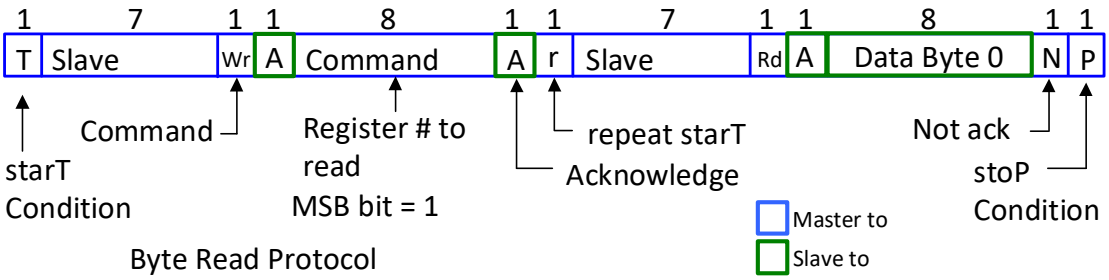


**Figure 17. Byte Read Protocol**

## 8.7. Byte Write

The figure below illustrates a simple, typical byte write. For byte operation, the MSB bit of the command byte must be set high. For block operations, the MSB bit must be set. If the bit is not set, the next byte must be the byte transfer count. The count can be between 1 and 32. It is not allowed to be zero or to exceed 32.

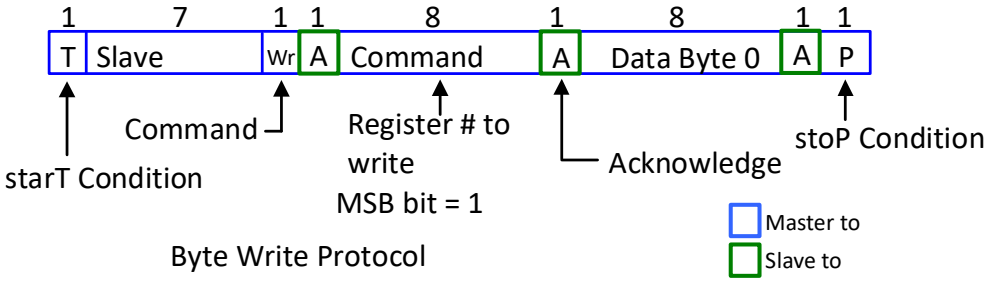


**Figure 18. Byte Write Protocol**

## 8.8. Data Protocol

The clock driver I2C protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operations, the system controller can access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The block write and block read protocol is outlined in Table 10. The byte write and byte read protocol is provided in Table 10. SA is the address select for $I^2C$. When the part is powered up, SA will be latched to select the $I^2C$ address.

**Table 9. SA State on First Application of PWRDNb**

| Description | SA | Address |
|---|---|---|
| State of SA on first deassertion of PWRDNb | 0 | 1101001 |
| | 1 | 1101010 |

**Table 10. Block Read and Block Write Protocol**

| Block Write Protocol | | Block Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 8:2 | Slave address—7 bits | 8:2 | Slave address–7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code—8 bits | 18:11 | Command Code–8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Byte Count—8 bits | 20 | Repeat start |

**Table 10. Block Read and Block Write Protocol (Continued)**

| Block Write Protocol | | Block Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 28 | Acknowledge from slave | 27:21 | Slave address–7 bits |
| 36:29 | Data byte 1–8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 45:38 | Data byte 2–8 bits | 37:30 | Byte Count from slave–8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| .... | Data Byte/Slave Acknowledges | 46:39 | Data byte 1 from slave–8 bits |
| .... | Data Byte N–8 bits | 47 | Acknowledge |
| .... | Acknowledge from slave | 55:48 | Data byte 2 from slave–8 bits |
| .... | Stop | 56 | Acknowledge |
| | | .... | Data bytes from slave/Acknowledge |
| | | .... | Data Byte N from slave–8 bits |
| | | .... | NOT Acknowledge |
| | | .... | Stop |

**Table 11. Byte Read and Byte Write Protocol**

| Byte Write Protocol | | Byte Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 8:2 | Slave address–7 bits | 8:2 | Slave address–7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code–8 bits | 18:11 | Command Code–8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Data byte–8 bits | 20 | Repeated start |
| 28 | Acknowledge from slave | 27:21 | Slave address–7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 37:30 | Data from slave–8 bits |
| | | 38 | NOT Acknowledge |
| | | 39 | Stop |

## 8.9. Register Tables

### 8.9.1. Si53212 Registers

**Table 12. Si53212 Control Register 0. Byte 0**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | DIFF7_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[7] |
| 6 | DIFF6_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[6] |
| 5 | DIFF5_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[5] |
| 4 | DIFF4_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[4] |
| 3 | DIFF3_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[3] |
| 2 | DIFF2_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[2] |
| 1 | DIFF1_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[1] |
| 0 | DIFF0_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[0] |

**Table 13. Si53212 Control Register 1. Byte 1**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | DIFF11_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[11] |
| 6 | DIFF10_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[10] |
| 5 | DIFF9_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[9] |
| 4 | DIFF8_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF[8] |
| 3 | Reserved | | | | 0 | Reserved |
| 2 | | | | | 0 | |
| 1 | | | | | 0 | |
| 0 | | | | | 0 | |

**Table 14. Si53212 Control Register 2. Byte 2**

| Reserved |
|---|

**Table 15. Si53212 Control Register 3. Byte 3**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | SR_SEL_DIFF7 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF7 |
| 6 | SR_SEL_DIFF6 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF6 |
| 5 | SR_SEL_DIFF5 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF5 |
| 4 | SR_SEL_DIFF4 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF4 |
| 3 | SR_SEL_DIFF3 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF3 |
| 2 | SR_SEL_DIFF2 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF2 |
| 1 | SR_SEL_DIFF1 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF1 |
| 0 | SR_SEL_DIFF0 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF0 |

**Table 16. Si53212 Control Register 4. Byte 4**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | SR_SEL_DIFF11 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF11 |
| 6 | SR_SEL_DIFF10 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF10 |
| 5 | SR_SEL_DIFF9 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF9 |
| 4 | SR_SEL_DIFF8 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF8 |
| 3 | AMP | | | RW | 1 | DIFF Differential Outputs Amplitude Adjustment.<br>0110 : 600 mV<br>0111 : 650 mV<br>1000 : 700 mV<br>1001 : 750 mV<br>1010 : 800 mV<br>1011 : 850 mV |
| 2 | AMP | | | RW | 0 | |
| 1 | AMP | | | RW | 0 | |
| 0 | AMP | | | RW | 0 | |

**Table 17. Si53212 Control Register 5. Byte 5**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Rev Code [7:4] | | | R | 0 | Revision Code |
| 6 | | | | R | 0 | |
| 5 | | | | R | 0 | |
| 4 | | | | R | 0 | |
| 3 | Vendor ID [3:0] | | | R | 1 | Vendor Identification Code |
| 2 | | | | R | 0 | |
| 1 | | | | R | 0 | |
| 0 | | | | R | 0 | |

**Table 18. Si53212 Control Register 6. Byte 6**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Programming ID [7:0] | | | R | 0 | Programming ID (Internal Only) |
| 6 | | | | R | 0 | |
| 5 | | | | R | 0 | |
| 4 | | | | R | 0 | |
| 3 | | | | R | 0 | |
| 2 | | | | R | 0 | |
| 1 | | | | R | 0 | |
| 0 | | | | R | 0 | |

## 8.9.2. Si53208 Registers

**Table 19. Si53208 Control Register 0. Byte 0**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | 0 | Reserved |
| 6 | DIFF4_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_4 |
| 5 | DIFF3_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_3 |
| 4 | Reserved | | | | 0 | Reserved |
| 3 | Reserved | | | | 0 | Reserved |
| 2 | DIFF2_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_2 |
| 1 | DIFF1_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_1 |
| 0 | DIFF0_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_0 |

**Table 20. Si53208 Control Register 1. Byte 1**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | DIFF7_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_7 |
| 6 | DIFF6_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_6 |
| 5 | Reserved | | | | 0 | Reserved |
| 4 | DIFF5_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_5 |
| 3 | Reserved | | | | 0 | Reserved |
| 2 | | | | | 0 | |
| 1 | | | | | 0 | |
| 0 | | | | | 0 | |

**Table 21. Si53208 Control Register 2. Byte 2**

| Reserved |
|---|

**Table 22. Si53208 Control Register 3. Byte 3**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | RW | 1 | Reserved |
| 6 | SR_SEL_DIFF_4 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_4 |
| 5 | SR_SEL_DIFF_3 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_3 |
| 4 | Reserved | | | RW | 1 | Reserved |
| 3 | Reserved | | | RW | 1 | Reserved |
| 2 | SR_SEL_DIFF_2 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_2 |
| 1 | SR_SEL_DIFF_1 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_1 |
| 0 | SR_SEL_DIFF_0 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_0 |

**Table 23. Si53208 Control Register 4. Byte 4**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | SR_SEL_DIFF_7 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_7 |
| 6 | SR_SEL_DIFF_6 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_6 |
| 5 | Reserved | | | RW | 1 | Reserved |
| 4 | SR_SEL_DIFF_5 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_5 |
| 3 | AMP | | | RW | 1 | DIFF Differential Outputs Amplitude Adjustment.<br>0110 : 600 mV<br>0111 : 650 mV<br>1000 : 700 mV<br>1001 : 750 mV<br>1010 : 800 mV<br>1011 : 850 mV |
| 2 | AMP | | | RW | 0 | |
| 1 | AMP | | | RW | 0 | |
| 0 | AMP | | | RW | 0 | |

**Table 24. Si53208 Control Register 5. Byte 5**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Rev Code [7:4] | | | R | 0 | Revision Code |
| 6 | | | | R | 0 | |
| 5 | | | | R | 0 | |
| 4 | | | | R | 0 | |
| 3 | Vendor ID [3:0] | | | R | 1 | Vendor Identification Code |
| 2 | | | | R | 0 | |
| 1 | | | | R | 0 | |
| 0 | | | | R | 0 | |

**Table 25. Si53208 Control Register 6. Byte 6**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Programming ID [7:0] | | | R | 0 | Programming ID (Internal Only) |
| 6 | | | | R | 0 | |
| 5 | | | | R | 0 | |
| 4 | | | | R | 0 | |
| 3 | | | | R | 0 | |
| 2 | | | | R | 0 | |
| 1 | | | | R | 0 | |
| 0 | | | | R | 0 | |

### 8.9.3. Si53204 Registers

**Table 26. Si53204 Control Register 0. Byte 0**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | 0 | Reserved |
| 6 | DIFF2_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_2 |
| 5 | DIFF1_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_1 |
| 4 | Reserved | | | | 0 | Reserved |
| 3 | Reserved | | | | 0 | Reserved |
| 2 | DIFF0_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_0 |
| 1 | Reserved | | | RW | 0 | Reserved |
| 0 | Reserved | | | RW | 0 | Reserved |

**Table 27. Si53204 Control Register 1. Byte 1**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | 0 | Reserved |
| 6 | Reserved | | | | 0 | Reserved |
| 5 | Reserved | | | | 0 | Reserved |
| 4 | DIFF3_OE | Disabled | Enabled | RW | 1 | Output enable for DIFF_3 |
| 3 | Reserved | | | | 0 | Reserved |
| 2 | | | | | 0 | |
| 1 | | | | | 0 | |
| 0 | | | | | 0 | |

**Table 28. Si53204 Control Register 2. Byte 2**

| Reserved |
|---|

**Table 29. Si53204 Control Register 3. Byte 3**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | RW | 1 | Reserved |
| 6 | SR_SEL_DIFF_2 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_2 |
| 5 | SR_SEL_DIFF_1 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_1 |
| 4 | Reserved | | | RW | 1 | Reserved |
| 3 | Reserved | | | RW | 1 | Reserved |
| 2 | SR_SEL_DIFF_0 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_0 |
| 1 | Reserved | | | RW | 1 | Reserved |
| 0 | Reserved | | | RW | 1 | Reserved |

**Table 30. Si53204 Control Register 4. Byte 4**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | RW | 1 | Reserved |
| 6 | Reserved | | | RW | 1 | Reserved |
| 5 | Reserved | | | RW | 1 | Reserved |
| 4 | SR_SEL_DIFF_3 | Slow setting | Fast setting | RW | 1 | Slew rate control for DIFF_3 |
| 3 | AMP | | | RW | 1 | DIFF Differential Outputs Amplitude Adjustment.<br>0110 : 600 mV<br>0111 : 650 mV<br>1000 : 700 mV<br>1001 : 750 mV<br>1010 : 800 mV<br>1011 : 850 mV |
| 2 | AMP | | | RW | 0 | |
| 1 | AMP | | | RW | 0 | |
| 0 | AMP | | | RW | 0 | |

**Table 31. Si53204 Control Register 5. Byte 5**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Rev Code [7:4] | | | R | 0 | Revision Code |
| 6 | | | | R | 0 | |
| 5 | | | | R | 0 | |
| 4 | | | | R | 0 | |
| 3 | Vendor ID [3:0] | | | R | 1 | Vendor Identification Code |
| 2 | | | | R | 0 | |
| 1 | | | | R | 0 | |
| 0 | | | | R | 0 | |

**Table 32. Si53204 Control Register 6. Byte 6**

| Bit | Name | If Bit = 0 | If Bit = 1 | Type | Default | Function |
|---|---|---|---|---|---|---|
| 7 | Programming ID [7:0] | | | R | 0 | Programming ID (Internal Only) |
| 6 | | | | R | 0 | |
| 5 | | | | R | 0 | |
| 4 | | | | R | 0 | |
| 3 | | | | R | 0 | |
| 2 | | | | R | 0 | |
| 1 | | | | R | 0 | |
| 0 | | | | R | 0 | |

# 9. Packaging

## 9.1. Si53212 Package

The figure below illustrates the package details for the Si53212 in a 64-Lead 9 x 9 mm QFN package. The table lists the values for the dimensions shown in the illustration.

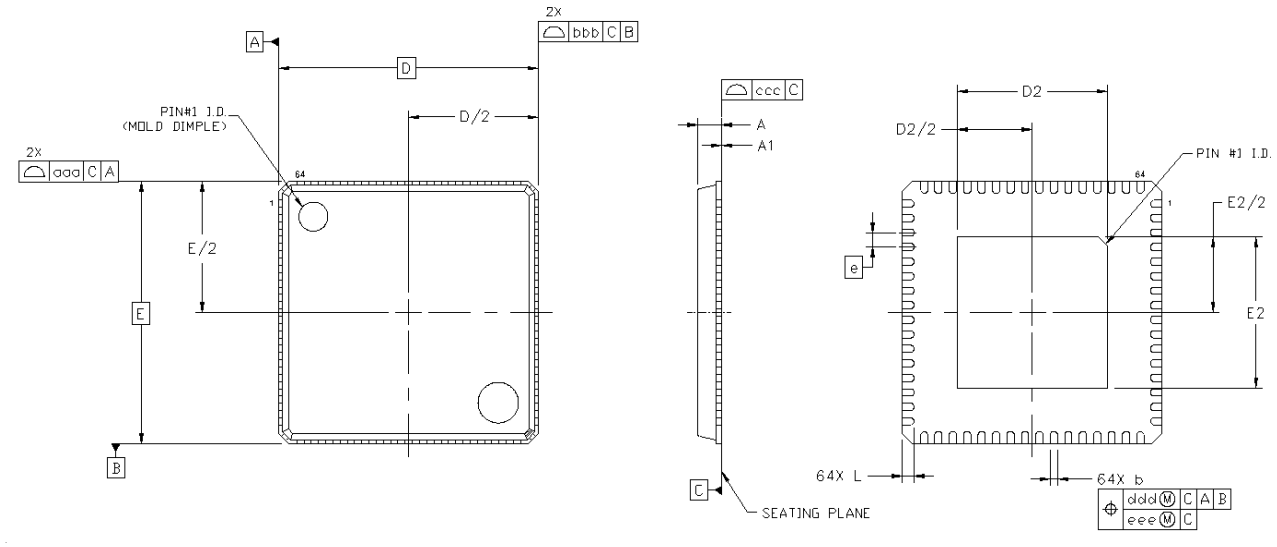


**Figure 19. Si53212 Package Diagram**

**Table 33. Si53212 Package Dimensions**

| Dimension | Min | Nom | Max | Notes |
|---|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 | All dimensions shown are in millimeters (mm) unless otherwise noted.<br>Dimensioning and Tolerancing per ANSI Y14.5M-1994.<br>This drawing conforms to JEDEC Outline MO-220.<br>Recommended card reflow profile is per JEDEC/IPC J-STD-020D specification for Small Body Components. |
| A1 | 0.00 | 0.02 | 0.05 | |
| b | 0.18 | 0.25 | 0.30 | |
| D | 9.00 BSC | | | |
| D2 | 5.10 | 5.20 | 5.30 | |
| e | 0.50 BSC | | | |
| E | 9.00 BSC | | | |
| E2 | 5.10 | 5.20 | 5.30 | |
| L | 0.30 | 0.40 | 0.50 | |
| aaa | 0.15 | | | |
| bbb | 0.10 | | | |
| ccc | 0.08 | | | |
| ddd | 0.10 | | | |
| eee | 0.05 | | | |

## 9.2. Si53212 Land Pattern

The following figure illustrates the land pattern details for the Si53212 in a 64-Lead 9 x 9 mm QFN package. The table lists the values for the dimensions shown in the illustration.

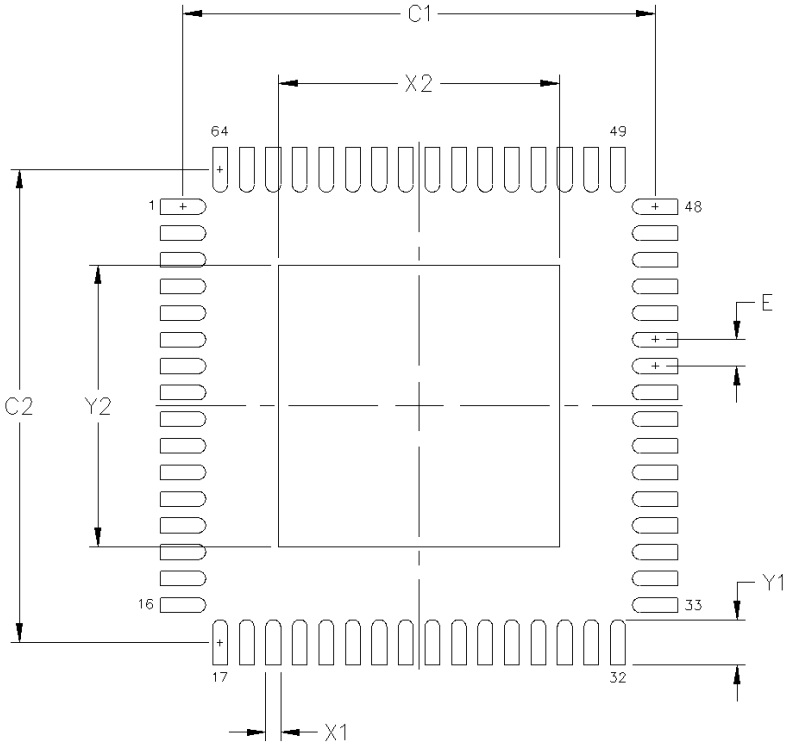


**Figure 20. Si53212 Land Pattern**

**Table 34. Si53212 PCB Land Pattern Dimensions**

| Dimension | mm | Notes |
|---|---|---|
| C1 | 8.90 | **General**<br>All dimensions shown are in millimeters (mm).<br>This Land Pattern Design is based on the IPC-7351 guidelines.<br>All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.<br><br>**Solder Mask Design**<br>All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.<br><br>**Stencil Design**<br>A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.<br>The stencil thickness should be 0.125 mm (5 mils).<br>The ratio of stencil aperture to land pad size should be 1:1 for all pads.<br>A 3x3 array of 1.25 mm square openings on a 1.80 mm pitch should be used for the center ground pad.<br><br>**Card Assembly**<br>A No-Clean, Type-3 solder paste is recommended.<br>The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. |
| C2 | 8.90 | |
| E | 0.50 | |
| X1 | 0.30 | |
| Y1 | 0.85 | |
| X2 | 5.30 | |
| Y2 | 5.30 | |

## 9.3. Si53212 Top Markings

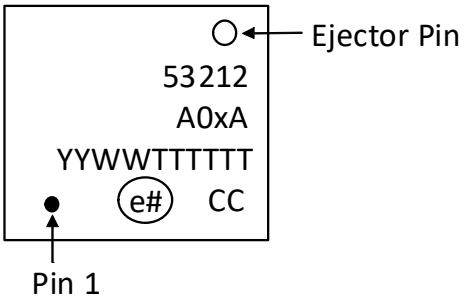


**Figure 21. Si53212 Top Marking**

**Table 35. Si53212 Top Marking Explanation**

| Line | Characters | Description |
|---|---|---|
| 1 | 53212 | Device part number |
| 2 | A0xA | Device part number<br>x = 1 = Internal 100 Ω impedance matching<br>x = 2 = Internal 85 Ω impedance matching |
| 3 | YYWWTTTTTT | YY = Assembly year<br>WW = Assembly work week<br>TTTTTT = Manufacturing trace code |
| 4 | e# CC | e# = Lead finish symbol. # is a number<br>CC = Country of origin (ISO abbreviation) |

## 9.4. Si53208 Package

The figure below illustrates the package details for the Si53208 in a 48-Lead 6 x 6 mm QFN package. The table lists the values for the dimensions shown in the illustration.

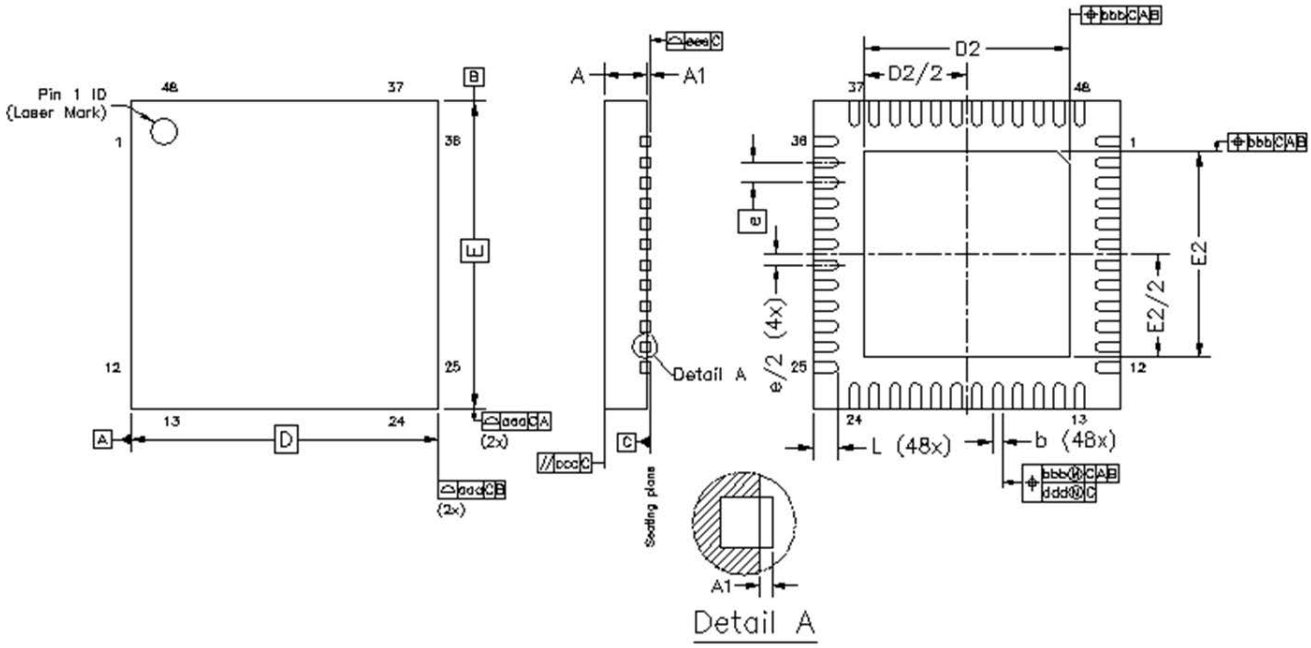


**Figure 22. Si53208 Package Diagram**

**Table 36. Si53208 Package Dimensions**

| Dimension | Min | Nom | Max | Notes |
|---|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| b | 0.15 | 0.20 | 0.25 | |
| D | | 6.00 BSC | | |
| D2 | 3.5 | 3.6 | 3.7 | All dimensions shown are in millimeters (mm) unless otherwise noted. |
| e | | 0.40 BSC | | |
| E | | 6.00 BSC | | Dimensioning and Tolerancing per ANSI Y14.5M-1994. |
| E2 | 3.5 | 3.6 | 3.7 | This drawing conforms to JEDEC Outline MO-220. |
| L | 0.30 | 0.40 | 0.50 | Recommended card reflow profile is per JEDEC/IPC J-STD-020 specification for Small Body Components. |
| aaa | | 0.10 | | |
| bbb | | 0.10 | | |
| ccc | | 0.10 | | |
| ddd | | 0.05 | | |
| eee | | 0.08 | | |

## 9.5. Si53208 Land Pattern

The figure below illustrates the land pattern details for the Si53208 in a 48-Lead, 6 x 6 mm QFN package. The table lists the values for the dimensions shown in the illustration.

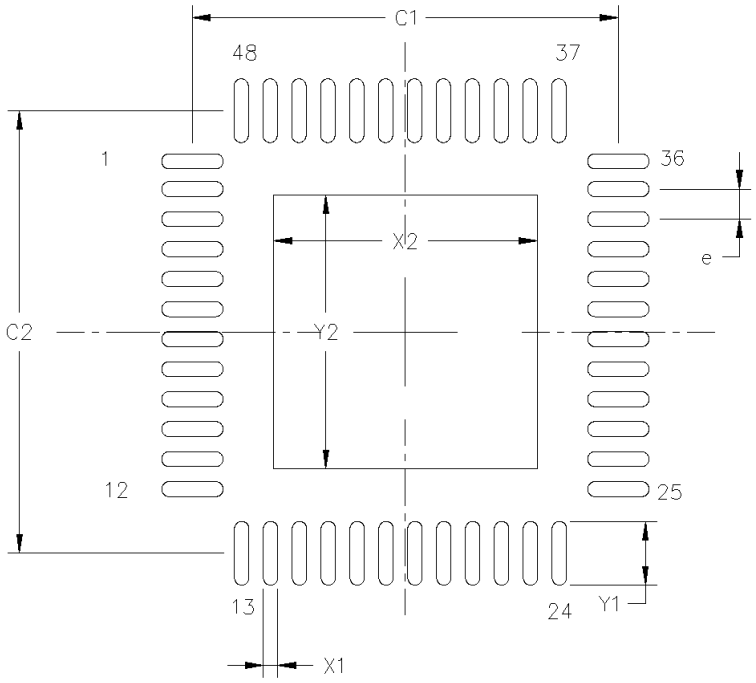


**Figure 23. Si53208 Land Pattern**

**Table 37. Si53208 PCB Land Pattern Dimensions**

| Dimension | mm | Notes |
|---|---|---|
| C1 | 5.90 | **General**<br>All dimensions shown are in millimeters (mm) unless otherwise noted.<br>Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.<br>This Land Pattern Design is based on IPC-7351 guidelines.<br>All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.<br><br>**Solder Mask Design**<br>All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.<br><br>**Stencil Design**<br>A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.<br>The stencil thickness should be 0.125 mm (5 mils).<br>The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.<br>A 3x3 array of 0.90 mm square openings on 1.15mm pitch should be used for the center ground pad.<br><br>**Card Assembly**<br>A No-Clean, Type-3 solder paste is recommended.<br>The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. |
| C2 | 5.90 | |
| X1 | 0.20 | |
| X2 | 3.60 | |
| Y1 | 0.85 | |
| Y2 | 3.60 | |
| e | 0.40 BSC | |

## 9.6. Si53208 Top Markings

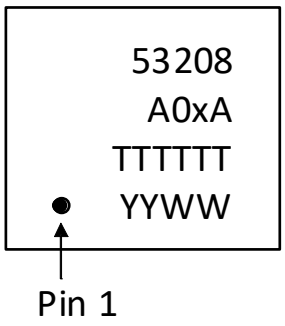


**Figure 24. Si53208 Top Marking**

**Table 38. Si53208 Top Marking Explanation**

| Line | Characters | Description |
|---|---|---|
| 1 | 52208 | Device part number |
| 2 | A0xA | Device part number<br>x = 1 = Internal 100 Ω impedance matching<br>x = 2 = Internal 85 Ω impedance matching |
| 3 | TTTTTT | TTTTTT = Manufacturing trace code |
| 4 | YYWW | YY = Assembly year<br>WW = Assembly work week |

## 9.7. Si53204 Package

The figure below illustrates the package details for the Si53204 in a 32-Lead, 5 x 5 mm QFN package. The table lists the values for the dimensions shown in the illustration.

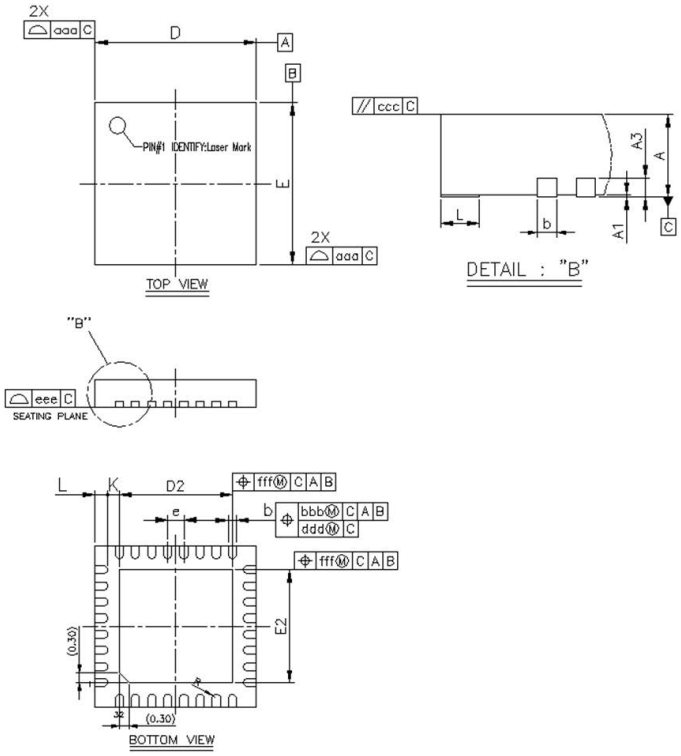


**Figure 25. Si53204 Package Diagram**

**Table 39. Si53204 Package Dimensions**

| Dimension | Min | Nom | Max | Notes |
|---|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 | All dimensions shown are in millimeters (mm) unless otherwise noted.<br><br>Dimensioning and Tolerancing per ANSI Y14.5M-1994.<br><br>This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.<br><br>Recommended card reflow profile is per JEDEC/IPC J-STD-020 specification for Small Body Components. |
| A1 | 0.00 | 0.02 | 0.05 | |
| A3 | | 0.20 REF | | |
| b | 0.18 | 0.25 | 0.30 | |
| D/E | 4.90 | 5.00 | 5.10 | |
| D2/E2 | 3.40 | 3.50 | 3.60 | |
| E | | 0.50 BSC | | |
| K | 0.20 | — | — | |
| L | 0.30 | 0.40 | 0.50 | |
| R | 0.09 | — | 0.14 | |
| aaa | | 0.15 | | |
| bbb | | 0.10 | | |
| ccc | | 0.10 | | |
| ddd | | 0.05 | | |
| eee | | 0.08 | | |
| fff | | 0.10 | | |

## 9.8. Si53204 Land Pattern

The figure below illustrates the land pattern details for the Si53204 in a 32-Lead, 5 x 5 mm QFN package. The table lists the values for the dimensions shown in the illustration.

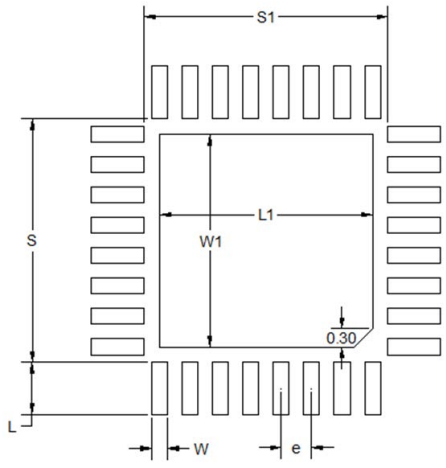


**Figure 26. Si53204 Land Pattern**

**Table 40. Si53204 PCB Land Pattern Dimensions**

| Dimension | mm | Notes |
|---|---|---|
| S1 | 4.01 | **General**<br>All dimensions shown are in millimeters (mm) unless otherwise noted.<br>This Land Pattern Design is based on IPC-7351 guidelines.<br><br>**Solder Mask Design**<br>All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.<br><br>**Stencil Design**<br>A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.<br>The stencil thickness should be 0.125mm (5 mils).<br>The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.<br>A 3x3 array of 0.85 mm square openings on 1.00 mm pitch can be used for the center ground pad.<br><br>**Card Assembly**<br>A No-Clean, Type-3 solder paste is recommended.<br>The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. |
| S | 4.01 | |
| L1 | 3.50 | |
| W1 | 3.50 | |
| e | 0.50 | |
| W | 0.26 | |
| L | 0.86 | |

## 9.9. Si53204 Top Markings

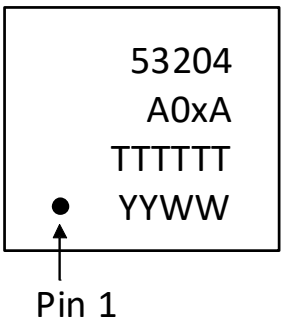


**Figure 27. Si53204 Top Marking**

**Table 41. Si53204 Top Marking Explanation**

| Line | Characters | Description |
|---|---|---|
| 1 | 52204 | Device part number |
| 2 | A0xB | Device part number<br>x = 1 = Internal 100 Ω impedance matching<br>x = 2 = Internal 85 Ω impedance matching |
| 3 | TTTTTT | TTTTTT = Manufacturing trace code |
| 4 | YYWW | YY = Assembly year<br>WW = Assembly work week |

# 10. Ordering Information

**Table 42. Si532x Ordering Guide**

| Number of Outputs | Internal Termination | Part Number | Package Type | Temperature |
|---|---|---|---|---|
| 12-output | 100 Ω | Si53212-A01AGM | 64-QFN | Extended, –40 to 85 °C |
| | | Si53212-A01AGMR | 64-QFN - Tape and Reel | Extended, –40 to 85 °C |
| | 85 Ω | Si53212-A02AGM | 64-QFN | Extended, –40 to 85 °C |
| | | Si53212-A02AGMR | 64-QFN - Tape and Reel | Extended, –40 to 85 °C |
| 8-output | 100 Ω | Si53208-A01AGM | 48-QFN | Extended, –40 to 85 °C |
| | | Si53208-A01AGMR | 48-QFN - Tape and Reel | Extended, –40 to 85 °C |
| | 85 Ω | Si53208-A02AGM | 48-QFN | Extended, –40 to 85 °C |
| | | Si53208-A02AGMR | 48-QFN - Tape and Reel | Extended, –40 to 85 °C |
| 4-output | 100 Ω | Si53204-A01AGM | 32-QFN | Extended, –40 to 85 °C |
| | | Si53204-A01AGMR | 32-QFN - Tape and Reel | Extended, –40 to 85 °C |
| | 85 Ω | Si53204-A02AGM | 32-QFN | Extended, –40 to 85 °C |
| | | Si53204-A02AGMR | 32-QFN - Tape and Reel | Extended, –40 to 85 °C |

## 10.1. Technical Support

**Table 43. Technical Support URLs**

| | |
|---|---|
| PCIe Clock Jitter Tool | https://www.skyworksinc.com/en/Products/Timing |
| PCIe Learning Center | https://www.skyworksinc.com/en/application-pages/pci-express-learning-center |
| Development Kit | https://www.skyworksinc.com/en/products/timing/evaluation-kits/clock/si52204-evaluation-kit |

# 11. Revision History

| Revision | Date | Description |
|---|---|---|
| B | August 2026 | • Added PCIe Gen7 performance specifications<br>• Replaced Skyworks Green icon, replaced with new wording for environmental compliance<br>• Revised copyright and trademark statement |
| A | July, 2023 | • Updated all references to PCIe Gen 1 through Gen 5 to Gen 1 to Gen 6 |
| 1.0 | March, 2019 | • Updated pin descriptions, electrical specifications, functional descriptions, and test and measurement Setup<br>• Added control registers |

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