8-Bit ADCs with Serial Interface and Configurable Input Multiplexer

Description

WM0834 and WM0838 are 8-bit analogue to digital converters (ADC) with configurable 4-input and 8-input multiplexers respectively and a serial I/O interface.

Assignment of the multiplexer inputs is configured before each conversion via the serial data input to give single-ended or differential operation for the selected inputs. A mixture of input configurations can be used in the same application. WM0838 also has a pseudo-differential configuration where all 8 inputs can be refered to a common input at an arbitrary voltage.

Serial communcation with WM0834/8 is via Data In (DI) and Data Out (DO) wires under the control of clock and chip select inputs. A high output at the SARS pin indicates when the conversion is in progress. To initiate a conversion chip enable is held low and data is input to DI on the rising edge of the clock, comprising, a start bit, and bits to set up the input configuration and polarity. After a half clock cycle delay conversion results appear at DO on the falling edge of the clock, MSB first, concurrently with A-D conversion. This is followed by the results LSB first, indicated by the falling edge of SARS. WM0838 has a shift enable (SE) input used to control the LSB first output on DO.

WM0834/8 operate on 5V and 3.3V supply voltages and are available in small outline and DIP packages for commercial (0 to 70^{O}C) and industrial (-40 to 85^{O}C) temperature ranges.

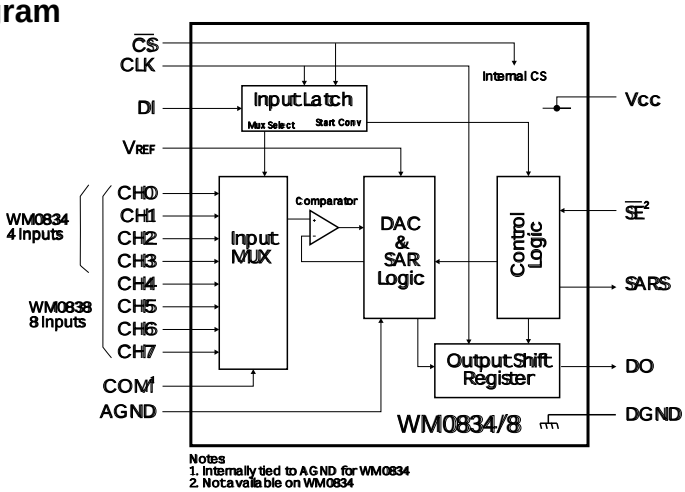
Features

- **Functionally Equivalent to National Semiconductor ADC0834 and ADC0838 without the Internal Zener Regulator Network**
- **4-input (WM0834) or 8-input (WM0838) MUX options**
- **Reference input operates ratiometrically or with a fixed reference**
- **Input range 0 to Vcc with Vcc Reference**
- **5V and 3.3V variants**
- **Total Unadjusted Error: ± 1 LSB**
- **8-bit resolution**
- **Low Power**
- **32 µs conversion time at fclock = 250 kHz**
- **Serial I/O interface**
- **WM0834 packages: 14 pin SO & DIP**
  WM0838 packages: 20 pin wide-body SO & DIP

Applications

- **Embedding with remote sensors**
- **Equipment health monitoring**
- **Automotive**
- **Industrial control**

Block Diagram

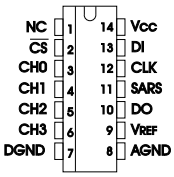


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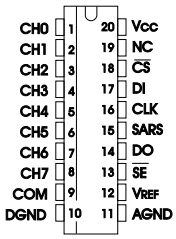
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Pin Configuration

Top View
WM0834 : N(DIP) and D (SO) packages
WM0838: N(DIP) and DW (SO) packages



WM0834



WM0838

Ordering Information

5V devices

DEVICE	TEMP. RANGE	PACKAGE
WM0834CN	0°C to 70°C	14 pin plastic DIP
WM0834CD	0°C to 70°C	14 pin plastic SO
WM0834IN	-40°C to 85°C	14 pin plastic DIP
WM0834ID	-40°C to 85°C	14 pin plastic SO
WM0838CN	0°C to 70°C	20 pin plastic DIP
WM0838CDW	0°C to 70°C	20 pin plastic SO
WM0838IN	-40°C to 85°C	20 pin plastic DIP
WM0838IDW	-40°C to 85°C	20 pin plastic SO

3.3V devices

DEVICE	TEMP. RANGE	PACKAGE
WM0834LCN	0°C to 70°C	14 pin plastic DIP
WM0834LCD	0°C to 70°C	14 pin plastic SO
WM0834LIN	-40°C to 85°C	14 pin plastic DIP
WM0834LID	-40°C to 85°C	14 pin plastic SO
WM0838LCN	0°C to 70°C	20 pin plastic DIP
WM0838LCDW	0°C to 70°C	20 pin plastic SO
WM0838LIN	-40°C to 85°C	20 pin plastic DIP
WM0838LIDW	-40°C to 85°C	20 pin plastic SO

Absolute Maximum Ratings (note 1)

Supply Voltage, Vcc (note 2) . . . . . 6.5 V
Input voltage range:
Digital Inputs . . . . GND - 0.3 V, VCC + 0.3 V
Analogue inputs . . . GND - 0.3 V, VCC + 0.3 V
Input current, any pin (note 3) . . . . . ± 5 mA
Total Input current for package . . . . . ± 20 mA

Operating temperature range, TA . . . . TMIN to TMAX
WM083_C_ (C suffix) . . . . . 0°C to +70°C
WM083_I_ (I suffix) . . . . . -40°C to +85°C
Storage Temperature . . . . . - 65°C to +150°C
Soldering Information:
Lead Temperature 1.6 mm (1/16) from case
for 10 seconds: D, DW or N package . . . . . 260°C

Recommended Operating Conditions (5V)

		SYMBOL	MIN	NOMINAL	MAX	UNIT
Supply voltage		V_{CC}	4.5	5	5.5	V
High level input voltage		V_{IH}	2			V
Low level input voltage		V_{IL}			0.8	V
Clock frequency		f_{clock}	10		600	KHz
Clock duty cycle (see Note 4)		D_{clk}	40		60	%
Pulse duration $\overline{CS}$ high		$t_{WH(CS)}$		220		ns
Operating free-air temperature	C suffix	T_A	0		70	°C
	I Suffix	T_A	-40		85	

Electrical Characteristics (5V)

V_{CC} = 5.0V, V_{REF} = 5V, f_{CLK} = 250 KHz, T_A = T_{MIN} to T_{MAX}, tr = tf = 20ns, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs						
High level output voltage	V_{OH}	V_{CC} = 4.75 V, I_{OH} = -360 mA	2.4			V
		V_{CC} = 4.75 V, I_{OH} = -10 mA	4.5			V
Low level output voltage	V_{OL}	V_{CC} = 5.25 V, I_{OH} = 1.6 mA			0.4	V
High level input current	I_{IH}	V_{IH} = 5 V		0.005	1	µA
Low level input current	I_{IL}	V_{IL} = 0 V		-0.005	-1	µA
High level output (source) current	I_{OH}	V_{OH} = 0 V	-6.5	-24		mA
Low level output (sink) current	I_{OL}	V_{OL} = V_{CC}	8	26		mA
High impedance-state output current (DO)	I_{OZ}	V_O = 5 V		0.01	3	µA
		V_O = 0 V		-0.01	-3	µA
Input capacitance	C_i			5		pF
Output capacitance	C_o			5		pF
Converter and Multiplexer						
Total unadjusted error	TUE	V_{REF} = 5 V. (note 7)			±1	LSB
Differential Linearity		(note 8)	8			Bits
Supply voltage variation error	$V_{s(error)}$	V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4	LSB
Common mode error		Differential mode		±1/16	±1/4	LSB
Common mode input voltage range	V_{ICR}	(note 9)	GND-0.05 V_{CC}+0.05			V
Standby input leakage current (note 10)	$I_{I(stdby)}$	On-channel VI = 5 V at ON ch.			1	µA
		Off-channel VI = 0 V at OFF ch.			-1	µA
		On-channel VI = 0 V at ON ch.			-1	µA
		Off-channel VI = 5 V at OFF ch.			1	µA
Conversion time	tconv	Excluding MUX addressing time			8	clock periods
Reference Inputs						
Input resistance to reference ladder	$R_{i(REF)}$		1.3	2.4	5.9	kΩ
Total device						
Supply current	I_{CC}			0.6	1.25	mA
Timing Parameters						
Setup time, $\overline{CS}$ low or data valid before clock ↑	t_{su}		350			ns
Hold time, data valid after clock ↑	t_h		90			ns
Propagation delay time, output data after clock ↓	t_{pd}	MSB data first. C_L = 100 pF			1500	ns
		LSB data first. C_L = 100 pF			600	ns
Output disable time, DO after $\overline{CS}$ ↑	t_{dis}	C_L = 10 pF, R_L = 10 kΩ		125	250	ns
		CL = 100 pF, R_L = 2 kΩ			500	ns

Recommended Operating Conditions (3.3V)

		SYMBOL	MIN	NOMINAL	MAX	UNIT
Supply voltage		V_{CC}	2.7	3.3	3.6	V
High level input voltage		V_{IH}	2			V
Low level input voltage		V_{IL}			0.8	V
Clock frequency (Vcc = 3.3V)		f_{clock}	10		600	KHz
Clock duty cycle (see Note 4)		D_{clk}	40		60	%
Pulse duration $\overline{CS}$ high		$t_{WH(CS)}$	220			ns
Operating free-air temperature	C suffix	T_A	0		70	°C
	I Suffix	T_A	-40		85	

Electrical Characteristics (3.3V)

V_{CC} = 3.3V, f_{CLK} = 250 KHz, $T_A = T_{MIN}$ to T_{MAX}, tr = tf = 20ns, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs						
High level output voltage	V_{OH}	V_{CC} = 3.0 V, I_{OH} = -360 mA	2.4			V
		V_{CC} = 3.0V, I_{OH} = -10 mA	2.8			V
Low level output voltage	V_{OL}	V_{CC} =3.0V, I_{OH} = 1.6 mA			0.4	V
High level input current	I_{IH}	V_{IH} = 3.6V		0.005	1	µA
Low level input current	I_{IL}	V_{IL} = 0 V		-0.005	-1	µA
High level output (source) current	I_{OH}	V_{OH} = 0 V, T_A = 25°C	6.5	15		mA
Low level output (sink) current	I_{OL}	$V_{OL} = V_{CC}$, T_A = 25°C	8	16		mA
High impedance-state output current (DO)	I_{OZ}	V_O = 3.3 V, T_A = 25°C		0.01	3	µA
		V_O = 0 V, T_A = 25°C		-0.01	-3	µA
Input capacitance	C_i			5		pF
Output capacitance	C_o			5		pF
Converter and Multiplexer						
Total unadjusted error	TUE	V_{REF} = 3.3 V. (note 7)			±1	LSB
Differential Linearity		(note 8)	8			Bits
Supply voltage variation error	$V_{s(error)}$	V_{CC} = 3.0 V to 3.6 V		±1/16	±1/4	LSB
Common mode error		Differential mode		±1/16	±1/4	LSB
Common mode input voltage range	V_{ICR}	(note 9)	GND-0.05 V_{CC}+0.05			V
Standby input leakage current (note 10)	$I_{I(stdby)}$	On-channel VI =3.3 V at ON ch.			1	µA
		Off-channel VI = 0 V at OFF ch.			-1	µA
		On-channel VI = 0 V at ON ch.			-1	µA
		Off-channel VI =3.3V at OFF ch			1	µA
Conversion time	tconv	Excluding MUX addressing time			8	clock periods
Reference Inputs						
Input resistance to reference ladder	$R_{i(REF)}$		1.3	2.4	5.9	kΩ
Total device						
Supply current	I_{CC}			0.2	0.75	mA
Timing Parameters						
Setup time, $\overline{CS}$ low or data valid before clock ↑	t_{su}		350			ns
Hold time, data valid after clock ↑	t_h		90			ns
Propagation delay time, output data after clock ↓	t_{pd}	MSB data first. C_L = 100 pF			500	ns
		LSB data first. C_L = 100 pF			200	ns
Output disable time, DO after $\overline{CS}$ ↑	t_{dis}	C_L = 10 pF, R_L = 10 kΩ			80	ns
		CL = 100 pF, R_L = 2 kΩ			250	ns

Electrical Characteristics (continued)

Notes:

1. Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating range limits are given under Recommended Operating Conditions. Guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

2. All voltage values, except differential voltages are with respect to the ground.

3. When the input voltage V_{IN} at any pin exceeds the power supply rails ($GND > V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA supply current to four.

4. A clock duty cycle range of 40% to 60% ensures correct operation at all clock frequencies. For a clock with a duty cycle outside these limits, the minimum time the clock is high or low must be at least 666 ns, with the maximum time for clock high or low being 60 ms.

5. All typical values are at V_{CC} = 5 V, T_A = 25°C for 5V devices and V_{CC} = 3.3 V, T_A = 25°C for 3.3V devices.

6. All parameters are measured under open-loop conditions with zero common mode input voltage (unless otherwise stated).

7. Total Unadjusted Error (TUE) is the sum of integral linearity error, zero code error and full scale error over the output code range.

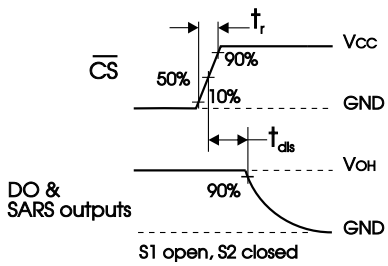
8. A Differential linearity of "n" bits ensures a code width exist to "n" bits. Hence a Differential Linearity of 8 bits for an 8 bit ADC guarantees no missing codes.

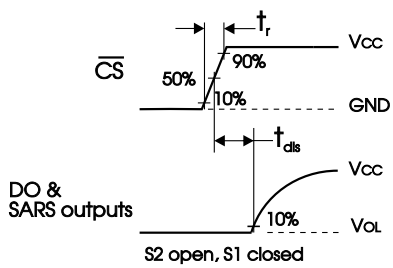
9. For $V_{IN}(-)$ greater than or equal to $V_{IN}(+)$ the digital output code will be 00 Hex. Connected to each analogue input are two diodes which will forward conduct for a diode drop outside the supply rails, V_{CC} and GND. If an analogue input voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To use an absolute input voltage range of 0 to V_{CC} a minimum V_{CC} - 0.05 V is required for all variations of temperature. Care should be exercised when testing at low V_{CC} levels with a maximum analogue voltage as this can cause the input diode to conduct, especially at high temperature, and cause errors for analogue inputs near full scale.

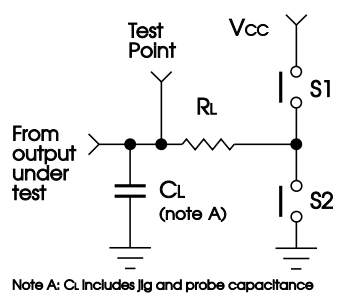
10. Standby input leakage currents, are currents going in or out of the on or off channels when the ADC is not performing conversion and the clock input is in a high or low steady-state condition.

Test Circuits and Waveforms

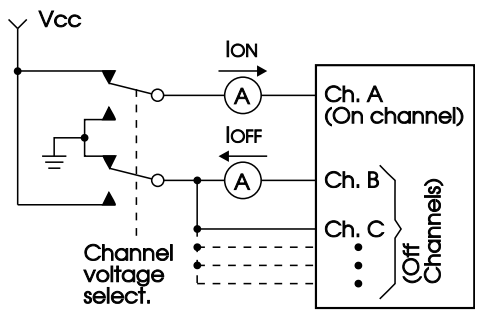
Output Disable Time Voltage Waveforms and Test Circuits





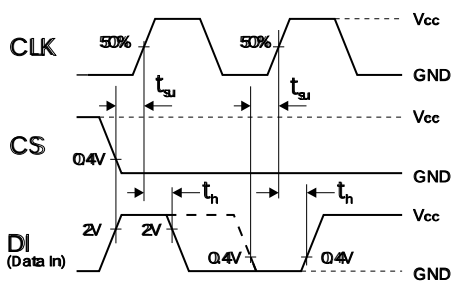


Standby Leakage Current Test Circuit

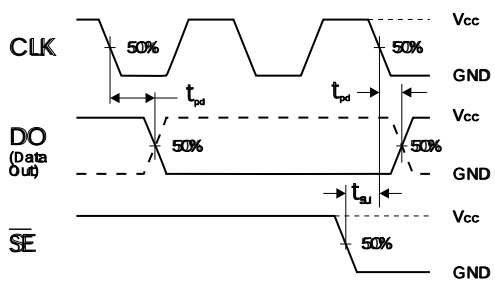


Detailed Timing Diagrams

Data Input Timing

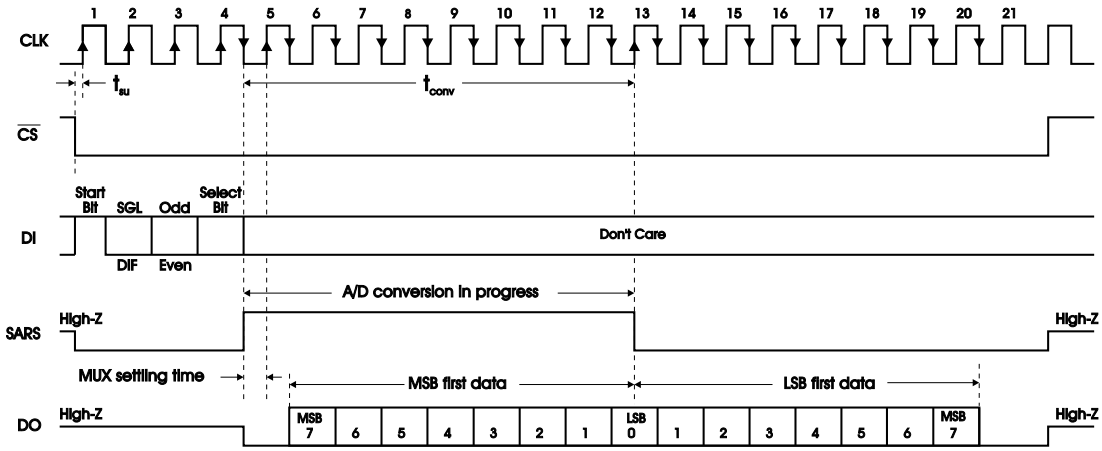


Data Output Timing

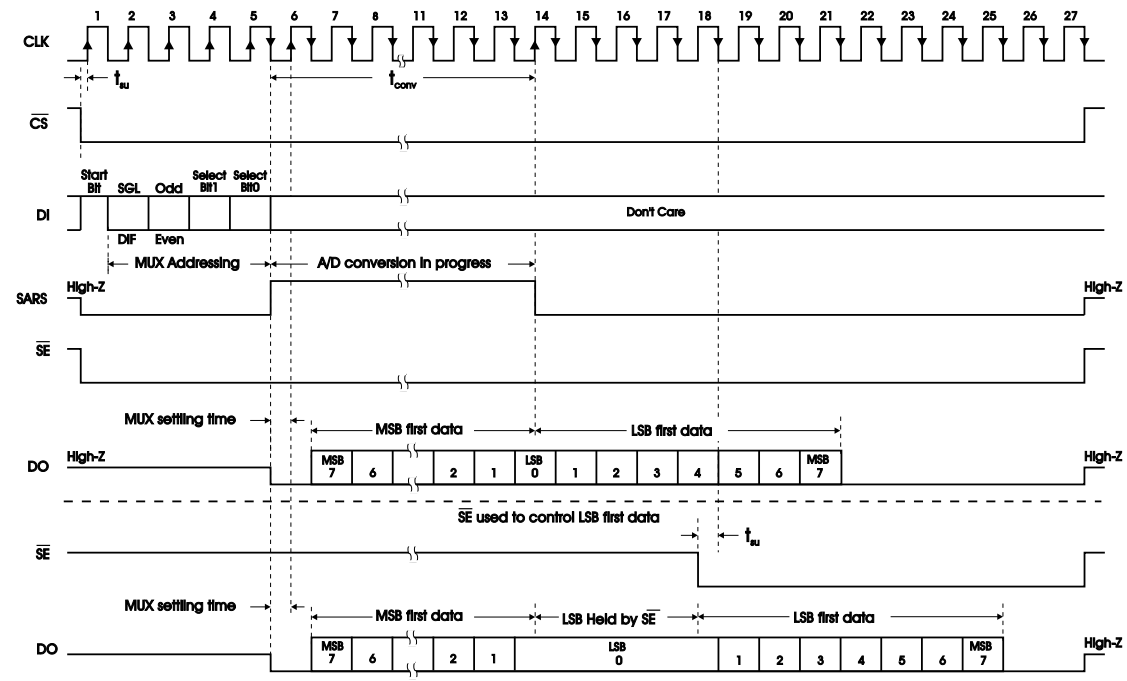


Functional Timing Diagrams

WM0834 Timing



WM0838 Timing



Pin Descriptions

WM0834			
Pin	**Name**	**Type**	**Function**
1	NC		No connection
2	$\overline{CS}$	Digital	Chip Select (active low)
3	CH0	Analogue input	Channel 0 input to multiplexer (MUX)
4	CH1	Analogue input	Channel 1 input to multiplexer (MUX)
5	CH2	Analogue input	Channel 2 input to multiplexer (MUX)
6	CH3	Analogue input	Channel 3 input to multiplexer (MUX)
7	DGND	Supply	Digital ground pin
8	AGND	Supply	Analogue ground pin
9	V_{REF}	Analogue input	Voltage reference input
10	DO	Digital output	Data output
11	SARS	Digital output	Successive approximation registar status line
12	CLK	Digital input	Clock input
13	DI	Digital input	Data input
14	V_{CC}	Supply	Positive supply voltage

WM0832			
Pin	**Name**	**Type**	**Function**
1	CH0	Analogue input	Channel 0 input to multiplexer (MUX)
2	CH1	Analogue input	Channel 1 input to multiplexer (MUX)
3	CH2	Analogue input	Channel 2 input to multiplexer (MUX)
4	CH3	Analogue input	Channel 3 input to multiplexer (MUX)
5	CH4	Analogue input	Channel 4 input to multiplexer (MUX)
6	CH5	Analogue input	Channel 5 input to multiplexer (MUX)
7	CH6	Analogue input	Channel 6 input to multiplexer (MUX)
8	CH7	Analogue input	Channel 7 input to multiplexer (MUX)
9	COM	Analogue input	Common input for pseudo differential mode
10	DGND	Supply	Digital ground pin
11	AGND	Supply	Analogue ground pin
12	VREF	Analogue input	Voltage reference input
13	SE	Digital input	Shift enable control line (active low)
14	DO	Digital output	Data Output
15	SARS	Digital output	Successive approximation register status line output
16	CLK	Digital input	Clock input
17	DI	Digital input	Data input
18	CS	Digital	Chip Select (active low)
19	NC		No connection
20	VCC	Supply	Positive supply voltage

Multiplexer / Package Options			
Device No	**Number of Analogue Channels**		**Number of Package Pins**
	Single Ended	**Differential**	
WM0834	4	2	14
WM0838	8	4	20

Functional Description

Multiplexer Operation and Addressing

WM0834 and WM0838 use an input multiplexer scheme thet provides multiple analogue channels, configurable for single-ended or differential operation and also for WM0838, a pseudo-differential mode that will perform an analogue to digital (A/D) conversion of the voltage difference between any analogue input and a common terminal (COM).

WM0834/8 uses a successive approximation routine to perform A/D conversion that employs a sample data comparator structure which always performs conversion on a differential voltage. Conversion takes place on the voltage difference between assigned "+" and "-" inputs and the converter expects the "+" input to be the most positive. If the "+" input is more negative than "-" then the converter gives an all zeros output.

Assignment of inputs is made for a single-ended signal between an "+" input and analogue ground (AGND) or COM for WM0838, or for differential inputs between adjacent pairs of inputs of either polarity.

The COM input of WM0838 acts as the "-" input for pseudo-differential "+" inputs and can be an arbitrary voltage such as an analogue common not at ground potential in single supply applications.

Prior to the start of every conversion the input configuration is assigned during the MUX addressing sequence achieved by serially shifting data into the Data Input (DI) on the rising edges of the clock input.

The MUX address selects which analogue inputs are enabled, either single-ended, differential or pseudo-differential (WM0838). For differential inputs the polarity of the selected pairs of adjacent inputs are also assigned. Differential inputs can only be assigned to adjacent channel pairs.

The MUX addressing tables give full details of input assignments.

Initiating Conversion and the Digital Interface

WM0834 and WM0838 are controlled from a processor via a serial interface comprising Data In (DI) and Data Out (DO), Chip Select ($\overline{CS}$) and Clock (CLK) inputs and a SAR Status (SARS) output.

A conversion is initiated by pulling the chip select ($\overline{CS}$) line low. $\overline{CS}$ must be kept low for an entire conversion.

The start bit and the MUX assignment bits on DI are clocked in on the rising edges of the clock input, which may be generated by the processor or run continuously.

WM0834 uses three MUX assignment bits and WM0838 uses four.

When the logic "1" start bit is clocked into the start conversion location of the multiplexer input register, the analogue MUX inputs are selected. After 1/2 a clock period delay to allow for the selected MUX output to settle, the conversion commences using the successive approximation technique. At this time, the SARS output goes high to indicate a conversion is in progress and the DI input is disabled.

When conversion begins, the A/D conversion result from the output of the SARS comparator appears at the DO output on each falling edge of the clock (see Functional Timing Diagrams).

With the successive approximation A/D conversion routine, the analogue input is compared with the output of a digital to analogue converter (DAC) for each bit by the SARS comparator and a decision made on whether the analogue input is higher or lower than the DAC output.

Successive bits, MSB to LSB are input to the DAC and remain in its input if the analogue comparison decides the analogue input is higher than the DAC output. If not, the bit is removed from the DAC input. The output from the SARS comparator forms the resulting input to the DAC and the A/D conversion output, and is read by the processor as conversion takes place in MSB to LSB order. After 8 clock periods, the conversion is complete and this is indicated by SARS being brought low a 1/2 clock period later.

All bits of the conversion are stored in an output shift register after a conversion has completed and MSB first data has been output.

For WM0838, the commencement of output data in a LSB first format can be controlled by use of the SE input. If the SE input is held high, the LSB output will remain on the DO output. When SE is brought low, LSB first data output will begin on DO. After 8-bits of LSB first data have been output, the DO output goes low and remains low until CS is brought high, when outputs (DO & SARS) go into a high impedance state.

Functional Description (continued)

WM0834 MUX Addressing						
MUX Address			Channel Number			
SGL/DIF	ODD/EVEN	Select bit	0	1	2	3
Differential MUX Mode (Between adjacent pairs of points)						
0	0	0	+	-		
0	0	1			+	-
0	1	0	-	+		
0	1	1			-	+
Single Ended MUX Mode (between selected input(s) and AGND)						
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

Note: Analogue common input 'COM' used with single ended mode is internally tied to AGND

All internal registers are cleared when $\overline{CS}$ is high. To initiate another conversion, $\overline{CS}$ must make a high to low transition and MUX address assignments input to DI.

The DI inpit and DO output can be tied together and controlled via a bidirectional processor I/O bit line.

Reference Input

The analogue input voltage range Vmax to Vmin for differential and pseudo-differential input is defined by the voltage applied to the reference input with respect to AGND.

WM0834/8 can be used in ratiometric appliacations or those requiring absolute accuracy. A ratiometric input is typically the Vcc and is the same supply used to power analogue input circuitry and sensors. In such systems under a given input condition, the same code will be output with variations in supply voltage, because the same ratio change occurs in both the analogue and reference input to the A/D. When used in applications requiring absolute accuracy, a suitable time and temperature stable voltage reference source should be used.

The voltage source used to drive the reference input should be capable of driving the 2.4kΩ typical of the SAR resistor ladder. The maximum input voltage to the reference input is the Vcc supply voltage. The minimum can be as least as low as 1V to allow for direct conversion of sensor outputs with output voltage ranges less than 5V.

Analogue Inputs

While sampling the analogue inputs, short spikes of current enter a "+" input and flow out of the corresponding "-" input at the clock edges during conversion. This current does not cause errors as it decays rapidly and the internal comparator is strobed at the end of a clock period. Care should be exercised if bypass capacitors are used at the inputs as an apparant offset error can be caused by the capacitor averaging the input current and developing a voltage across the source resistance. Bypass capacitors should not be used with a source resistance greater than 1kΩ.

In considering error sources, input leakage current will also cause a voltage drop across the source resistance and hence, high impedance sources should be buffered.

In differential mode, there is a 1/2 clock period interval between sampling the "+" and the "-" inputs. If there is a change in common mode voltage during this interval, an errorcould notionally result.

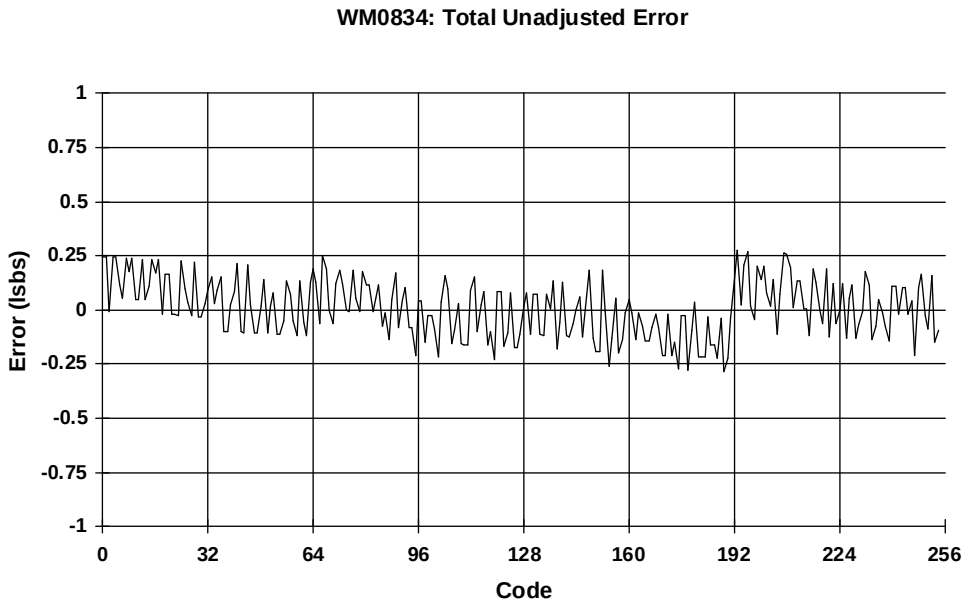
For a sinusoidal common mode signal, the error is given by:

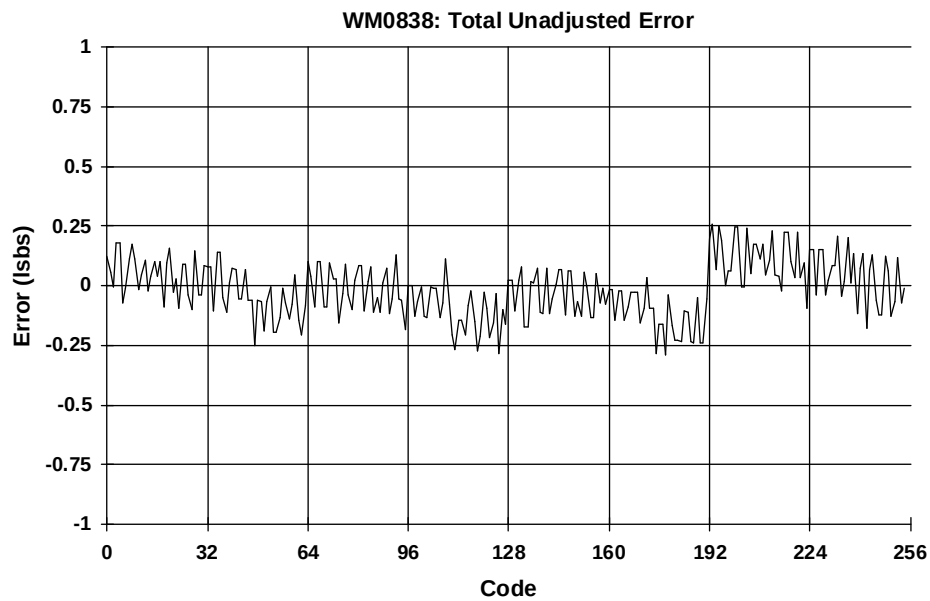
$$V_{ERROR} = V_{PEAK} (2\pi f_{CM}) (1/(2f_{CLK}))$$

Where V_{PEAK} = peak common mode voltage
f_{CM} = common mode signal frequency
f_{CLK} = clock frequency

WM0838 MUX Addressing												
MUX Address				Channel Number								
SGL/ DIF	ODD/ EVEN	Select biits 1	Select biits 0	0	1	2	3	4	5	6	7	COM
Differential MUX Mode (between adjacent pairs of inputs)												
0	0	0	0	+	-							
0	0	0	1			+	-					
0	0	1	0					+	-			
0	0	1	1							+	-	
0	1	0	0	-	+							
0	1	0	1			-	+					
0	1	1	0					-	+			
0	1	1	1							-	+	
Single Ended MUX Mode (between selected input(s) and 'COM' pseudo analogue ground)												
1	0	0	0	+								-
1	0	0	1			+						-
1	0	1	0					+				-
1	0	1	1							+		-
1	1	0	0		+							-
1	1	0	1				+					-
1	1	1	0						+			-
1	1	1	1								+	-

Performance Data



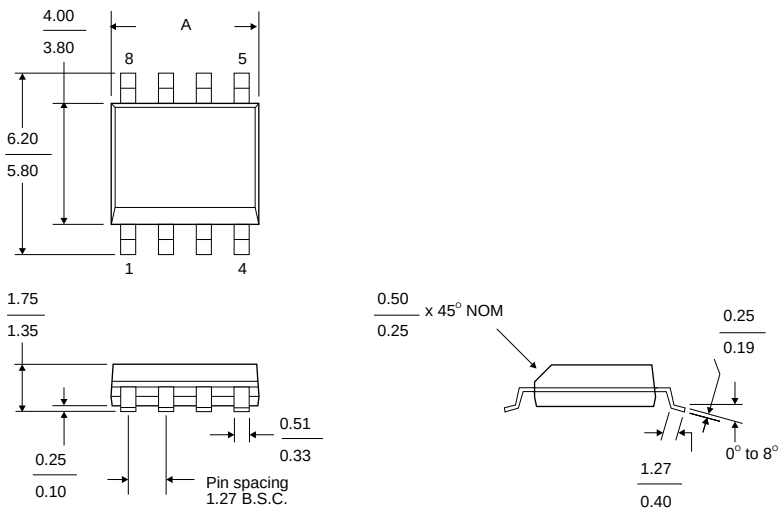


Test conditions: V_{DD} = 5V, V_{REF} = 5V, Temp = 25°C, F_{CLK} = 250kHz

Package Descriptions

Plastic Small-Outline Package

D - 8 pins shown



Dimension 'A' Variations

N	Min	Max
8	4.80	5.00
14	8.55	8.75
16	9.80	10.00

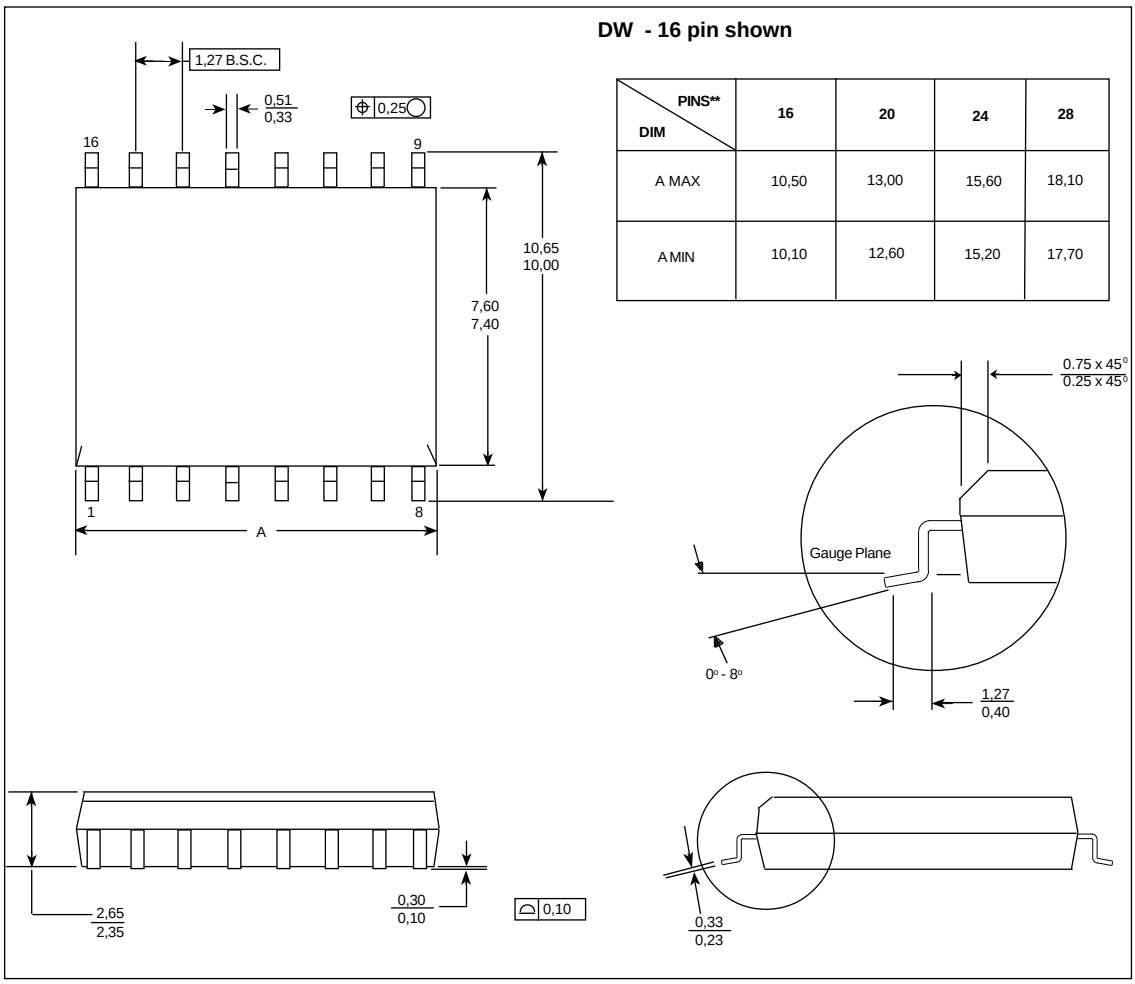
Notes:

A. Dimensions in millimeters.
B. Complies with Jedec standard MS-012.
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold flash or protrusion.
E. Dimension A, mould flash or protrusion shall not exceed 0.15mm. Body width, interlead flash or protrusions shall not exceed 0.25mm.

Package Description

Wide body Plastic Small-Outline Package

DW - 16 pin shown



DIM \ PINS**	16	20	24	28
A MAX	10,50	13,00	15,60	18,10
A MIN	10,10	12,60	15,20	17,70

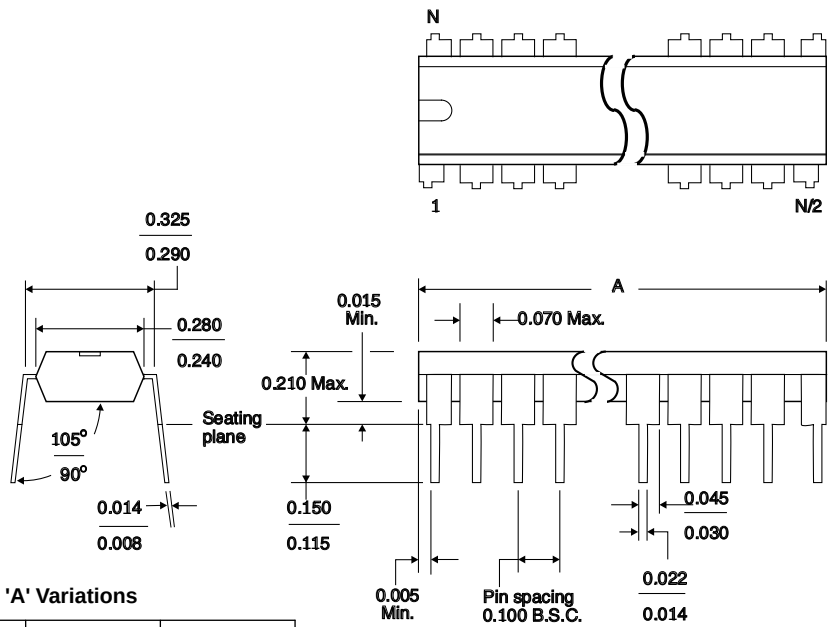
Notes:

A. Dimensions in millimeters.
B. Complies with Jedec standard MS-013.
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold flash or protrusion.
E. Dimension A, mould flash or protrusion shall not exceed 0.15mm. Body width, interlead flash or protrusions shall not exceed 0.25mm.

Package Descriptions

Dual-In-Line Package

N or P



Dimension 'A' Variations

N	Min	Max
8	0.355	0.400
14	0.735	0.775
16	0.735	0.775
20	0.940	0.975

Notes:

A. Dimensions are in inches
B. Falls within JEDEC MS-001(20 pin package is shorter than MS-001)
C. N is the maximum number of terminals
D. All end pins are partial width pins as shown, except the 14 pin package which is full width.