# PSOC™ 62 MCU

## Arm® Cortex®-M4

## General description

PSOC™ 6 MCU is a high-performance, ultra-low-power and secured MCU platform, purpose-built for IoT applications. The CY8C62x6/7 product line, based on the PSOC™ 6 MCU platform, is a combination of a high-performance microcontroller with low-power flash technology, digital programmable logic, high-performance analog-to-digital conversion and standard communication and timing peripherals.

## Features

- 32-bit dual CPU subsystem
  - 150-MHz Arm® Cortex®-M4F (CM4) CPU with single-cycle multiply, floating point, and memory protection unit (MPU)
  - 100-MHz Cortex®-M0+ (CM0+) CPU with single-cycle multiply and MPU
  - User-selectable core logic operation at either 1.1 V or 0.9 V, Ordering information
  - Active CPU current slope with 1.1-V core operation
    - Cortex®-M4: 40 µA/MHz
    - Cortex®-M0+: 20 µA/MHz
  - Active CPU current slope with 0.9-V core operation
    - Cortex®-M4: 22 µA/MHz
    - Cortex®-M0+: 15 µA/MHz
  - Two DMA controllers with 16 channels each
- Memory subsystem
  - 1-MB application flash, 32-KB auxiliary flash (AUXFlash), and 32-KB supervisory flash (SFlash); read-while-write (RWW) support. Two 8-KB flash caches, one for each CPU
  - 288-KB SRAM with power and data retention control
  - One-time-programmable (OTP) 1-Kb eFuse array
- Low-power 1.7-V to 3.6-V operation
  - Six power modes for fine-grained power management
  - Deep Sleep mode current of 7 µA with 64-KB SRAM retention
  - On-chip Single-In Multiple Out (SIMO) DC-DC buck converter, <1 µA quiescent current
  - Backup domain with 64 bytes of memory and real-time clock
- Flexible clocking options
  - 8-MHz Internal Main Oscillator (IMO) with ±2% accuracy
  - Ultra-low-power 32-kHz Internal Low-speed Oscillator (ILO)
  - On-chip crystal oscillators (16 to 35 MHz, and 32 kHz)
  - Phase-locked loop (PLL) for multiplying clock frequencies
  - Frequency-locked loop (FLL) for multiplying IMO frequency
  - Integer and fractional peripheral clock dividers
- Quad SPI (QSPI)/Serial Memory Interface (SMIF)
  - Execute-In-Place (XIP) from external quad SPI Flash
  - On-the-fly encryption and decryption
  - 4-KB cache for greater XIP performance with lower power
  - Supports single, dual, quad, dual-quad, and octal interfaces with throughput up to 640 Mbps
- Segment LCD drive
  - Supports up to 99 segments and up to 8 commons

## Features

- Serial communication
  - Nine run-time configurable Serial Communication Blocks (SCBs)
    - Eight SCBs: configurable as SPI, $I^2C$, or UART
    - One Deep Sleep SCB: configurable as SPI or $I^2C$
  - USB full-speed device/host interface
- Audio subsystem
  - Two pulse density modulation (PDM) channels and one $I^2S$ channel with time division multiplexed (TDM) mode
- Timing and pulse-width modulation
  - Thirty-two timer/counter/pulse-width modulators (TCPWM)
  - Center-aligned, edge, and pseudo-random modes
  - Comparator-based triggering of Kill signals
- Programmable analog
  - 12-bit 1-Msps SAR ADC with differential and single-ended modes and 16-channel sequencer with result averaging
  - Two low-power comparators available in Deep Sleep and Hibernate modes
  - Built-in temperature sensor connected to ADC
  - One 12-bit voltage-mode digital-to-analog converter (DAC) with < 2-µs settling time
  - Two opamps with low-power operation modes
- Up to 100 programmable GPIOs
  - Two Smart I/O ports (16 I/Os) enable Boolean operations on GPIO pins; available during system Deep Sleep
  - Programmable drive modes, strengths, and slew rates
  - Six overvoltage-tolerant (OVT) pins
- Capacitive sensing
  - CAPSENSE™ provides best-in-class signal-to-noise ratio (SNR), liquid tolerance, and proximity sensing
  - Enables dynamic usage of both self and mutual sensing
  - Automatic hardware tuning (SmartSense)
- Security built into platform architecture
  - Step-wise authentication of execution images
  - Secured execution of code in execute-only mode for protected routines
  - All debug and test ingress paths can be disabled
  - Up to eight protection contexts
- Cryptography accelerator
  - Hardware acceleration for symmetric and asymmetric cryptographic methods and hash functions
  - True random number generation (TRNG) function
- Programmable digital
  - Twelve programmable logic blocks, each with 8 Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
  - Usable as drag-and-drop Boolean primitives (gates, registers), or as Verilog-programmable blocks
  - Infineon-provided peripheral component library using UDBs to implement functions such as communication peripherals (for example, LIN, UART, SPI, $I^2C$, S/PDIF and other protocols), waveform generators, Pseudo-Random Sequence (PRS) generation, and many other functions
- Profiler
  - Eight counters provide event or duration monitoring of on-chip resources

- Packages
  - 124-BGA (9 mm x 9 mm x 1 mm and 7 mm x 7 mm x 0.8 mm)
  - 80-WLCSP (in 0.33 and 0.43 mm heights)
- Device identification and revisions
  - Product line ID (12-bit): 0x100
  - Major/minor die revision ID: 2/4
  - Firmware revisions: Rom Boot: 4.1

**Table 1 Flash boot versions**

| Flash boot revision | Description of change |
|---|---|
| 1.20.1.45 | Baseline production release |
| 1.20.1.53 | Implements manual clock transition from FLL output to IMO to resolve Table 65 errata. |

See Boot code section for more details on boot code

This product line has a JTAG ID which is available through the SWJ interface. It is a 32-bit ID, where:

- The most significant digit is the device revision, based on the major die revision
- The next four digits correspond to the part number, for example "E4B0" as a hexadecimal number
- The three least significant digits are the manufacturer ID, in this case "069" as a hexadecimal number

The Silicon ID system call can be used by firmware to get Silicon ID and ROM Boot data. For more information, see the reference manuals.

The Flash Boot version can be read directly from a designated address 0x1600 2004. For more information, see the reference manuals.

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# 1 Development ecosystem

## 1.1 PSOC™ 6 MCU resources

Infineon provides a wealth of data at www.infineon.com to help you select the right PSOC™ device and quickly and effectively integrate it into your design. The following is an abbreviated, hyperlinked list of resources for PSOC™ 6 MCU:

- **Overview**: PSOC™ portfolio
- **Product selectors**: PSOC™ 6 MCU
- Application notes cover a broad range of topics, from basic to advanced level, and include the following:
  - AN221774: Getting started with PSOC™ 6 MCU on PSOC™ Creator
  - AN210781: Getting started with PSOC™ 6 MCU with Bluetooth® Low Energy connectivity on PSOC™ Creator
  - AN218241: PSOC™ 6 MCU hardware design considerations
  - AN213924: PSOC™ 6 MCU Device Firmware Update (DFU) software development kit guide
  - AN215656: PSOC™ 6 MCU dual-core system design
  - AN219528: PSOC™ 6 MCU low-power modes and power reduction techniques
  - AN221111: PSOC™ 6 MCU designing a custom secured system
  - AN85951: PSOC™ 4 and PSOC™ 6 MCU CAPSENSE™ design guide
- Code examples demonstrate product features and usage, and are also available on Infineon GitHub repositories
- Reference manuals provide detailed descriptions of PSOC™ 6 MCU architecture and registers
- PSOC™ 6 MCU programming specification provides the information necessary to program PSOC™ 6 MCU nonvolatile memory
- Development tools
  - ModusToolbox™ software enables cross platform code development with a robust suite of tools and software libraries
  - PSOC™ 6 CAD libraries provide footprint and schematic support for common tools. BSDL files and IBIS models are also available
- Training videos are available on a wide range of topics including the PSOC™ 6 MCU 101 series
- Infineon Developer Community enables connection with fellow PSOC™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated PSOC™ 6 MCU Community

## 1.2 ModusToolbox™ software

ModusToolbox™ software is Infineon's comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code repositories on GitHub. This includes:

- Board Support Packages (BSPs) aligned with Infineon kits
- Low-level resources, including a Hardware Abstraction Layer (HAL) and Peripheral Driver Library (PDL)
- Middleware enabling industry-leading features such as CAPSENSE™, Bluetooth® Low Energy, and mesh networks
- An extensive set of thoroughly tested code example applications

***Note**: The HAL provides a high-level, simplified interface to configure and use the hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. For example, it wraps the PSOC™ 6 PDL with a simplified API, but the PDL exposes all low-level peripheral functionality. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control.*

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional Eclipse IDE for ModusToolbox™, as Figure 1 shows. For information on using Infineon tools, refer to the documentation delivered with ModusToolbox™ software, and AN228571 - Getting started with PSOC™ 6 MCU on ModusToolbox™.

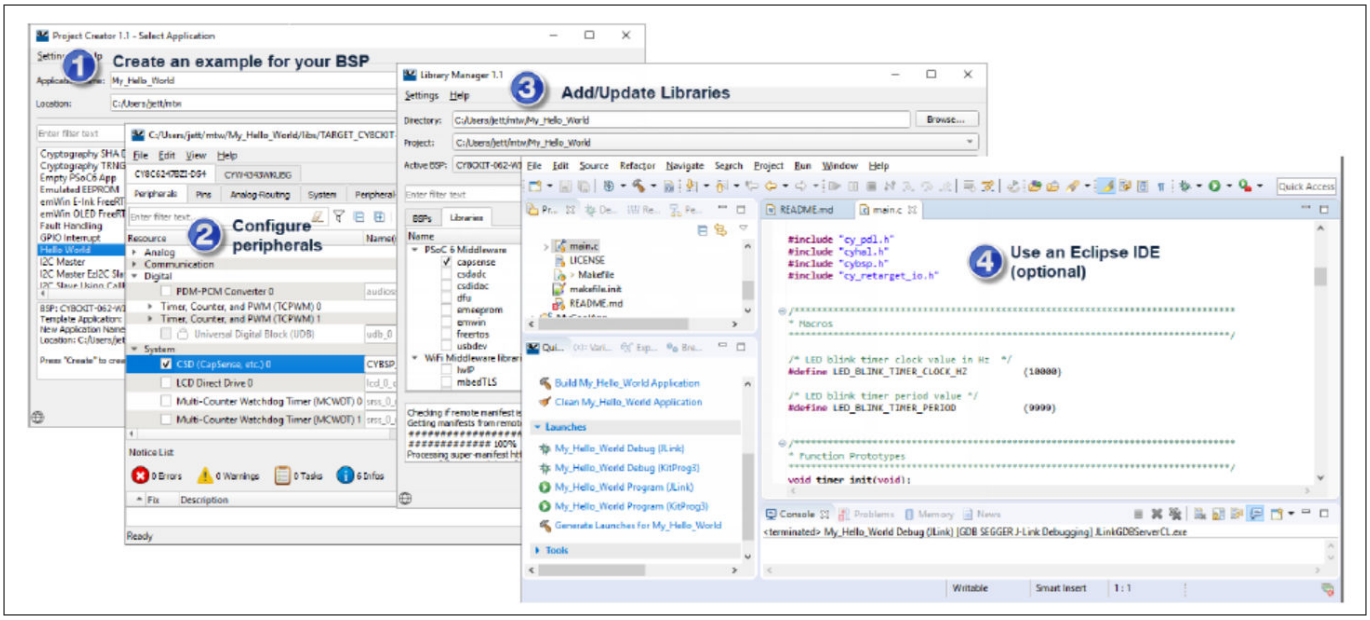



**Figure 1 ModusToolbox™ software tools**

## 1.3 PSOC™ Creator

PSOC™ Creator is a free Windows-based Integrated Design Environment (IDE). It enables you to design hardware and firmware systems concurrently, based on the PSOC™ 6 MCU. Figure 2 shows that with PSOC™ Creator, you can:

1. Explore the library of 200+ Components in PSOC™ Creator
2. Drag and drop Component icons to complete your hardware system design in the main design workspace
3. Configure Components using the Component Configuration Tools and the Component datasheets
4. Co-design your application firmware and hardware in the PSOC™ Creator IDE or build project for third-party IDE
5. Prototype your solution with the PSOC™ 6 Pioneer Kits. If a design change is needed, PSOC™ Creator and Components enable you to make changes on-the-fly without the need for hardware revisions

## 1 Development ecosystem

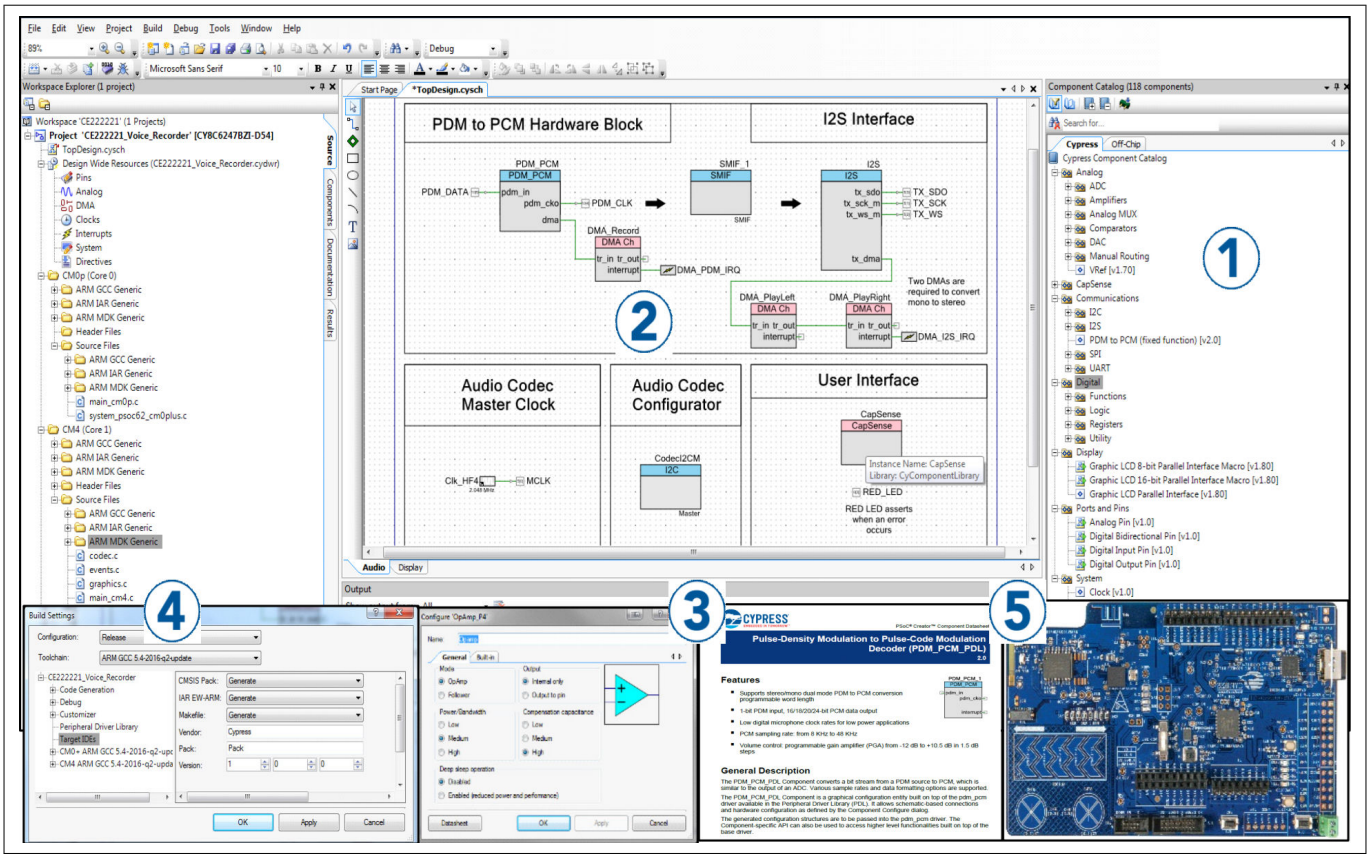



**Figure 2 PSOC™ Creator schematic entry and components**

# 2 Blocks and functionality

Figure 3 shows the major subsystems and a simplified view of their interconnections. The color coding shows the lowest power mode where a block is still functional. For example, the SRAM is functional down to Deep Sleep mode.

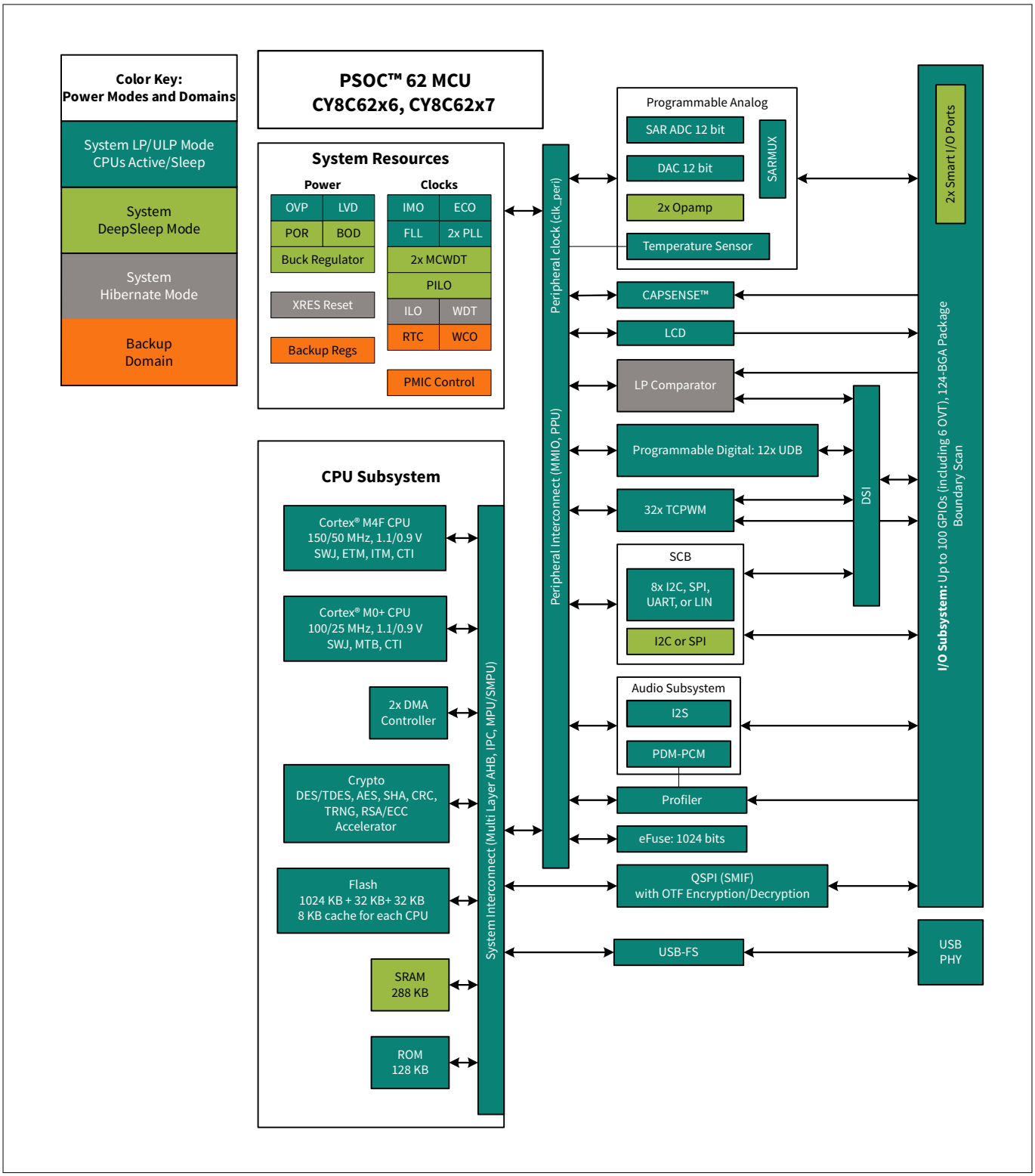



**Figure 3 Block diagram**

There are three debug access ports, one each for CM4 and CM0+, and a system port. PSOC™ 6 MCU devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. All device interfaces can be permanently disabled for applications concerned about a reprogrammed device or starting and interrupting flash programming sequences. All programming, debug, and test interfaces can be disabled.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The Eclipse IDE for ModusToolbox™software [1)] and PSOC™ Creator [2)] Integrated Development Environment (IDE) provide fully integrated programming and debug support for these devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, PSOC™ 6 provides multiple levels of device security.

1 ModusToolbox™ software does not support UDBs or UDB-based Components.
2 PSOC™ Creator is not recommended for new designs.

# 3 Functional description

The following sections provide an overview of the features, capabilities and operation of each functional block identified in the block diagram in Figure 3. For more detailed information, refer to the following documentation:

- Board Support Package (BSP) documentation

BSPs are available on GitHub. They are aligned with Infineon kits and provide files for basic device functionality such as hardware configuration files, startup code, and linker files. The BSP also includes other libraries that are required to support a kit. Each BSP has its own documentation, but typically includes an API reference such as the example here. This search link finds all currently available BSPs on the Infineon GitHub site.

- Hardware Abstraction Layer API reference manual

The Hardware Abstraction Layer (HAL) provides a high-level interface to configure and use hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control. The HAL API Reference provides complete details. Example applications that use the HAL download it automatically from the GitHub repository.

- Peripheral Driver Library (PDL) Application Programming Interface (API) reference manual

The Peripheral Driver Library (PDL) integrates device header files and peripheral drivers into a single package and supports all PSOC™ 6 MCU product lines. The drivers abstract the hardware functions into a set of easy-to-use APIs. These are fully documented in the PDL API Reference. Example applications that use the PSOC™ 6 PDL download it automatically from the GitHub repository.

- Architecture reference manual

The architecture reference manual provides a detailed description of each resource in the device. This is the next reference to use if it is necessary to understand the operation of the hardware below the software provided by PDL. It describes the architecture and functionality of each resource and explains the operation of each resource in all modes. It provides specific guidance regarding the use of associated registers.

- Register reference manual

The register reference manual provides a complete list of all registers in the device. It includes the breakdown of all register fields, their possible settings, read/write accessibility, and default states. All registers that have a reasonable use in typical applications have functions to access them from within PDL. Note that ModusToolbox™ and PDL may provide software default conditions for some registers that are different from and override the hardware defaults.

## 3.1 CPU and memory subsystem

PSOC™ 6 has multiple bus masters, as Figure 3 shows. They are: CPUs, DMA controllers, QSPI, USB, and a Crypto block. Generally, all memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm® AMBA high-performance bus (AHB) arbitration. Accesses between CPUs can be synchronized using an inter-processor communication (IPC) block.

### 3.1.1 CPUs

There are two Arm® Cortex® CPUs:

The Cortex®-M4 (CM4) has single-cycle multiply, a floating-point unit (FPU), and a memory protection unit (MPU). It can run at up to 150 MHz. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.

CM4 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the ARMv7-M Architecture Reference Manual).

The Cortex®-M0+ (CM0+) has single-cycle multiply, and an MPU. It can run at up to 100 MHz; however, for CM4 speeds above 100 MHz, CM0+ and bus peripherals are limited to half the speed of CM4. Thus, for CM4 running at

150 MHz, CM0+ and peripherals are limited to 75 MHz in system low power (LP) mode. In system ultra-low power (ULP) mode, CPU speeds are limited to 50 MHz and 25 MHz respectively.

CM0+ is the secondary CPU; it is used to implement system calls and device-level safety and protection features.

CM0+ provides a secured, uninterruptible boot function. This helps ensure that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

CM0+ implements the Armv6-M Thumb instruction set (defined in the ARMv6-M Architecture Reference Manual).

The CPUs have the following power draw, at $V_{DDD}$ = 3.3 V and using the internal buck regulator:

**Table 2 Active current slope at $V_{DDD}$ = 3.3 V using the internal buck regulator**

| | | System Power mode | |
|---|---|---|---|
| | | **ULP** | **LP** |
| CPU | Cortex®-M0+ | 15 µA/MHz | 20 µA/MHz |
| | Cortex®-M4 | 22 µA/MHz | 40 µA/MHz |

The CPUs can be selectively placed in their Sleep and Deep Sleep power modes as defined by Arm®.

Both CPUs have nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response, and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

The CPUs have extensive debug support. PSOC™ 6 has a debug access port (DAP) that acts as the interface for device programming and debug. An external programmer or debugger (the “host”) communicates with the DAP through the device serial wire debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to restrictions), the host can access the device memory and peripherals as well as the registers in both CPUs.

Each CPU offers debug and trace features as follows:

- CM4 supports six hardware breakpoints and four watchpoints, 4-bit embedded trace macrocell (ETM), serial wire viewer (SWV), and printf()-style debugging through the single wire output (SWO) pin
- CM0+ supports four hardware breakpoints and two watchpoints, and a micro trace buffer (MTB) with 4-KB dedicated RAM

PSOC™ 6 also has an Embedded Cross Trigger for synchronized debugging and tracing of both CPUs.

### 3.1.2 Interrupts

This product line has 147 system and peripheral interrupt sources and supports interrupts and system exceptions on both CPUs. CM4 has 147 interrupt request lines (IRQ), with the interrupt source ‘n’ directly connected to IRQn. CM0+ has 32 interrupts IRQ[31:0] with configurable mapping of one system interrupt source to any of the IRQ[31:0].

Each interrupt supports configurable priority levels (eight levels for CM4 and four levels for CM0+). One system interrupt can be mapped to each of the CPUs' non-maskable interrupts (NMI). Up to 41 interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC. See the reference manual for details.

### 3.1.3 InterProcessor Communication (IPC)

In addition to the Arm® SEV and WFE instructions, a hardware InterProcessor Communication (IPC) block is included. It includes 16 IPC channels and 16 IPC interrupt structures. The IPC channels can be used to implement data communication between the processors. Each IPC channel also implements a locking scheme which can be used to manage shared resources. The IPC interrupts let one processor interrupt the other, signaling an event. This is used to trigger events such as notify and release of the corresponding IPC channels. Some IPC channels and other resources are reserved, as Table 3 shows:

**Table 3 Distribution of IPC channels and other resources**

| Resources available | Resources consumed |
|---|---|
| IPC channels, 16 available | 8 reserved |
| IPC interrupts, 16 available | 8 reserved |
| Other interrupts | 1 reserved |
| CM0+ NMI | Reserved |
| Other resources: clock dividers, DMA channels, etc. | 1 CM0+ interrupt mux |

### 3.1.4 DMA controllers

There are two DMA controllers with 16 channels each, which support CPU-independent accesses to memory and peripherals. The descriptors for DMA channels can be in SRAM or flash. Therefore, the number of descriptors are limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination. The size of data transfer per descriptor varies based on the type of DMA channel. See the reference manual for detail.

### 3.1.5 Cryptography accelerator (Crypto)

This subsystem consists of hardware implementation and acceleration of cryptographic functions and random number generators.

The Crypto subsystem supports the following:

- Encryption/Decryption functions
  - Data Encryption Standard (DES)
  - Triple DES (3DES)
  - Advanced Encryption Standard (AES) (128-, 192-, 256-bit)
  - Elliptic Curve Cryptography (ECC)
  - RSA cryptography functions
- Hashing functions
  - Secure Hash Algorithm (SHA)
  - SHA-1
  - SHA-224/-256/-384/-512
- Message authentication functions (MAC)
  - Hashed message authentication code (HMAC)
  - Cipher-based message authentication code (CMAC)
- 32-bit cyclic redundancy; code (CRC) generator
- Random number generators
  - Pseudo random number generator (PRNG)
  - True random number generator (TRNG)

### 3.1.6 Protection units

This product line has multiple types of protection units to control erroneous or unauthorized access to memory and peripheral registers. CM4 and CM0+ have Arm® MPUs for protection at the bus master level. Other bus masters use additional MPUs. Shared memory protection units (SMPUs) help implement memory protection for

memory resources that are shared among multiple bus masters. Peripheral protection units (PPU) are similar to SMPUs but are designed for protecting the peripheral register space.

Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secured/non-secured, and protection context. Some protection unit resources are reserved for system usage; see the reference manual for details.

### 3.1.7 Memory

PSOC™ 6 contains flash, SRAM, ROM, and eFuse memory blocks.

- Flash

There is up to 1 MB of application flash, organized in 256-KB sectors. There are also two 32-KB flash sectors:

- Auxiliary flash (AUXFlash), typically used for EEPROM emulation
- Supervisory flash (SFlash). Data stored in SFlash includes device trim values, Flash Boot code, and encryption keys. After the device transitions into the “Secure” lifecycle stage, SFlash can no longer be changed

The flash has 128-bit-wide accesses to reduce power. Write operations can be performed at the row level. A row is 512 bytes. Read operations are supported in both Low Power and Ultra-Low Power modes, however write operations may not be performed in Ultra-Low Power mode.

The flash controller has two caches, one for each CPU. Each cache is 8 KB, with 4-way set associativity.

- SRAM

Up to 288 KB of SRAM is provided. Power control and retention granularity is implemented in 32-KB blocks allowing the user to control the amount of memory retained in Deep Sleep. Memory is not retained in Hibernate mode.

- ROM

The 128-KB ROM, also referred to as the supervisory ROM (SROM), provides code (ROM Boot) for several system functions. The ROM contains device initialization, flash write, security, eFuse programming, and other system-level routines. ROM code is executed only by the CM0+ CPU, in protection context 0. A system function can be initiated by either CPU, or through the DAP. This causes an NMI in CM0+, which causes CM0+ to execute the system function.

- eFuse

A one-time-programmable (OTP) eFuse array consists of 1024 bits, of which 512 are reserved for system use such as die ID, device ID, initial trim settings, device life cycle, and security settings. The remaining bits are available for storing key information, hash values, unique IDs or similar custom content.

Each fuse is individually programmed; once programmed (or “blown”), its state cannot be changed. Blowing a fuse transitions it from the default state of 0 to 1. To program an eFuse, $V_{DDIO0}$ must be at 2.5 V ±5%, at 14 mA.

Because blowing an eFuse is an irreversible process, programming is recommended only in mass production under controlled factory conditions. For more information, see PSOC™ 6 MCU programming specifications.

### 3.1.8 Boot code

Two blocks of code, ROM Boot and Flash Boot, are pre-programmed into the device and work together to provide device startup and configuration, basic security features, life-cycle stage management and other system functions.

- ROM Boot

On a device reset, the boot code in ROM is the first code to execute. This code performs the following:

- Integrity checks of flash boot code
- Device trim setting (calibration)

- Setting the device protection units
- Setting device access restrictions for life-cycle states

ROM cannot be changed and acts as the Root of Trust in a secured system.

- Flash Boot

Flash boot is a firmware module stored in SFlash and application flash. It ensures that only a validated application may run on the device. It also ensures that the firmware image has not been modified, such as by a malicious third party.

Flash boot:

- Is validated by ROM Boot
- Runs after ROM Boot and before the user application
- Enables system calls
- Configures the Debug Access Port
- Launches the user application

If the user application cannot be validated, then flash boot ensures that the device is transitioned into a safe state.

### 3.1.9 Memory map

Both CPUs have a fixed address map, with shared access to memory and peripherals. The 32-bit (4 GB) address space is divided into the regions shown in Table 4. Note that code can be executed from the Code and External RAM.

**Table 4 Address map for CM4 and CM0+**

| Address range | Name | Use |
|---|---|---|
| 0x0000 0000 – 0x1FFF FFFF | Code | Program code region. Data can also be placed here. It includes the exception vector table, which starts at address 0. |
| 0x2000 0000 – 0x3FFF FFFF | SRAM | Data region. This region is not supported in PSOC™ 6. |
| 0x4000 0000 – 0x5FFF FFFF | Peripheral | All peripheral registers. Code cannot be executed from this region. CM4 bit-band in this region is not supported in PSOC™ 6. |
| 0x6000 0000 – 0x9FFF FFFF | External RAM | SMIF or Quad SPI, (see the QSPI Interface Serial Memory Interface (SMIF) section). Code can be executed from this region. |
| 0xA000 0000 – 0xDFFF FFFF | External device | Not used. |
| 0xE000 0000 – 0xE00F FFFF | Private peripheral bus | Provides access to peripheral registers within the CPU core. |
| 0xE010 0A000 – 0xFFFF FFFF | Device | Device-specific system registers. |

The device memory map shown in Table 5 applies to both CPUs. That is, the CPUs share access to all PSOC™ 6 MCU memory and peripheral registers.

**Table 5 Internal memory address map for CM4 and CM0+**

| Address range | Memory type | Size |
|---|---|---|
| 0x0000 0000 – 0x0001 FFFF | ROM | 128 KB |
| 0x0800 0000 – 0x0804 7FFF | SRAM | Up to 288 KB |
| 0x1000 0000 – 0x100F FFFF | Application flash | Up to 1 MB |
| 0x1400 0000 – 0x1400 7FFF | Auxiliary flash, can be used for EEPROM emulation | 32 KB |
| 0x1600 0000 – 0x1600 7FFF | Supervisory flash | 32 KB |

Note that the SRAM is located in the Arm® Code region for both CPUs (see Table 4). There is no physical memory located in the CPUs' Arm® SRAM regions.

## 3.2 System resources

### 3.2.1 Power system

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the reset occurring. There are no voltage sequencing requirements.

The $V_{DDD}$ supply (1.7 to 3.6 V) powers an on-chip buck regulator or a low-dropout regulator (LDO), selectable by the user. In addition, both the buck and the LDO offer a selectable (0.9 or 1.1 V) core operating voltage ($V_{CCD}$). The selection lets users choose between two system power modes:

- System Low Power (LP) operates $V_{CCD}$ at 1.1 V and offers high performance, with no restrictions on device configuration
- System Ultra Low Power (ULP) operates $V_{CCD}$ at 0.9 V for exceptional low power, but imposes limitations on clock speeds

In addition, a backup domain adds an "always on" functionality using a separate power domain supplied by a backup supply ($V_{BACKUP}$) such as a battery or supercapacitor. It includes a real-time clock (RTC) with alarm feature, supported by a 32.768-kHz watch crystal oscillator (WCO), and power-management IC (PMIC) control. See the Power supply considerations for more details.

### 3.2.2 Power modes

PSOC™ 6 MCU can operate in four system and three CPU power modes. These modes are intended to minimize the average power consumption in an application. For more details on power modes and other power-saving configuration options, see the application note, AN219528: PSOC™ 6 MCU low-power modes and power reduction techniques and the architecture reference manual.

Power modes supported by PSOC™ 6 MCUs, in the order of decreasing power consumption, are:

- System Low Power (LP) – All peripherals and CPU power modes are available at maximum speed
- System Ultra Low Power (ULP) – All peripherals and CPU power modes are available, but with limited speed
- CPU Active – CPU is executing code in system LP or ULP mode
- CPU Sleep – CPU code execution is halted in system LP or ULP mode

- CPU Deep Sleep – CPU code execution is halted and system Deep Sleep is requested in system LP or ULP mode
- System Deep Sleep – Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- System Hibernate – Device and I/O states are frozen and the device resets on wakeup

CPU Active, Sleep, and Deep Sleep are standard Arm® - defined power modes supported by the Arm® CPU instruction set architecture (ISA). System LP, ULP, Deep Sleep and Hibernate modes are additional low-power modes supported by PSOC™ 6 MCU.

### 3.2.3 Clock system

Figure 4 shows that the clock system consists of the following:

- Internal main oscillator (IMO)
- Internal low-speed oscillator (ILO)
- Precision ILO (PILO)
- Watch crystal oscillator (WCO)
- External MHz crystal oscillators (ECOs)
- External clock input
- Phase-locked loop (PLL)
- Frequency-locked loop (FLL)

Clocks may be buffered and brought out to a pin on a smart I/O port.

The default clocking when the application starts is CLK_HF[0] being driven by the IMO and the FLL. CLK_HF[0], clk_fast, clk_peri, and clk_slow are all either 50 MHz (LP mode) or 25 MHz (ULP mode). All other clocks, including all peripheral clocks, are off.

### 3.2.4 Internal Main Oscillator (IMO)

The IMO is the primary source of internal clocking. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz and tolerance is ±2%.

### 3.2.5 Internal Low-speed Oscillator (ILO)

The ILO is a very low power oscillator, nominally 32 kHz, which operates in all power modes. The ILO can be calibrated against a higher accuracy clock for better accuracy.

*Precision ILO (PILO)*

PILO is a 32.768-kHz clock that can provide a more accurate clock than ILO when periodically calibrated using a high-accuracy clock such as the ECO.

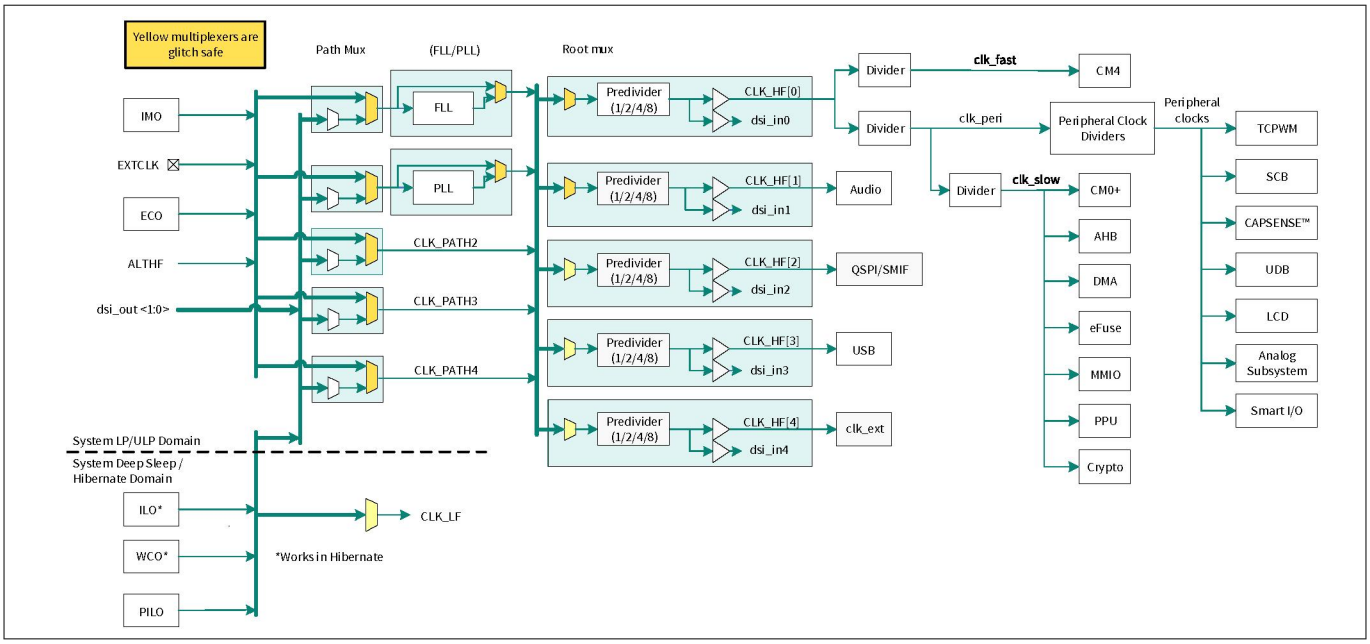



**Figure 4 Clocking diagram**

## 3.2.6 External Crystal Oscillators

Figure 5 shows all of the external crystal oscillator circuits for this product line. The component values shown are typical; check ECO specifications for the crystal values, and the crystal datasheet for the load capacitor values. The ECO and WCO require balanced external load capacitors. For more information, see the reference manual and AN218241 - PSOC™ 6 MCU hardware design considerations.

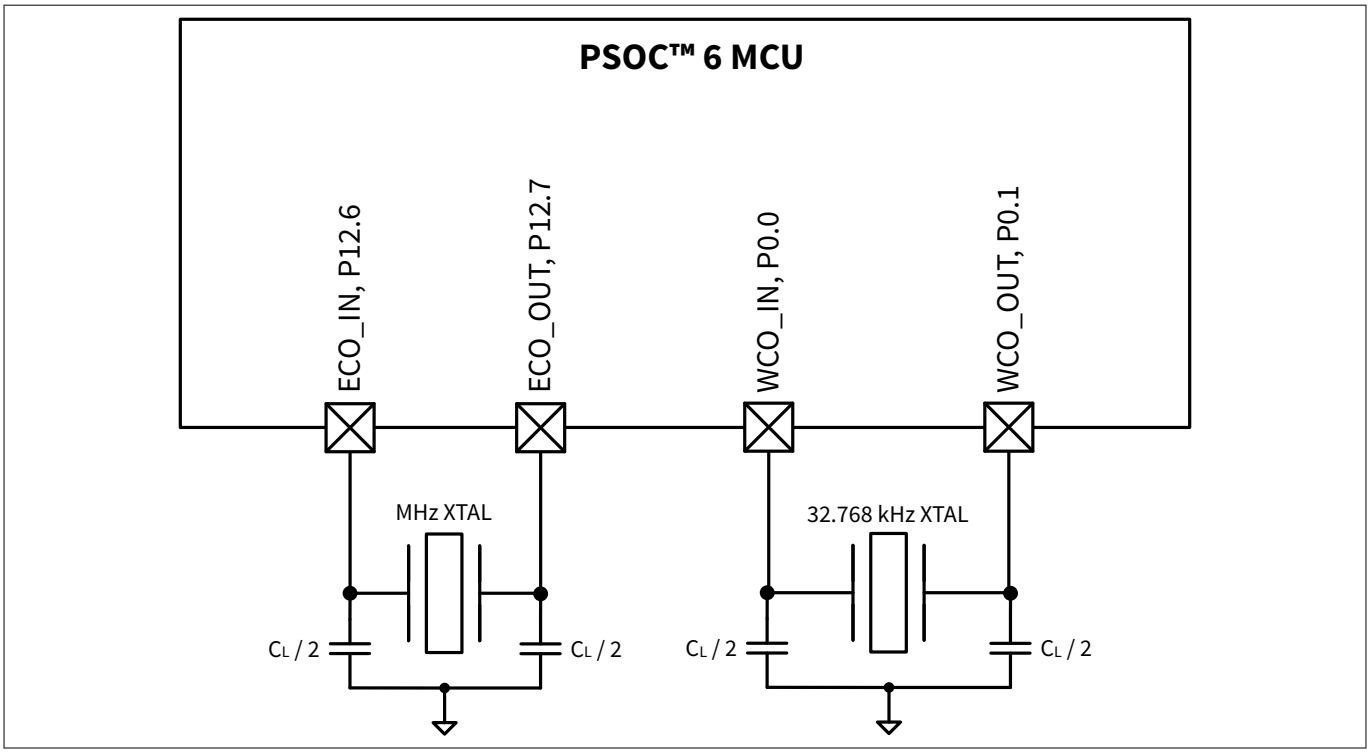



**Figure 5 Oscillator circuits**

If the ECO is used, note that its performance is affected by GPIO switching noise. GPIO ports should be used as Table 6 shows. See also Table 7 for additional restrictions for general analog subsystem use.

**Table 6 ECO usage guidelines**

| Ports | Maximum frequency | Drive strength for $V_{DDD} \leq 2.7$ V | Drive strength for $V_{DDD} > 2.7$ V |
|---|---|---|---|
| Port 11 | 60 MHz for SMIF (QSPI) | DRIVE_SEL 2 | DRIVE_SEL 3 |
| Ports 12 and 13 | Slow slew rate setting | No restrictions | No restrictions |

### 3.2.7 Watchdog timers (WDT, MCWDT)

PSOC™ 6 MCU has one WDT and two multi-counter WDTs (MCWDTs). The WDT has a 16-bit free-running counter. Each MCWDT has two 16-bit counters and one 32-bit counter, with multiple operating modes. All of the 16-bit counters can generate a watchdog device reset. All of the counters can generate an interrupt on a match event.

The WDT is clocked by the ILO. It can do interrupt/wakeup generation in system LP/ULP, Deep Sleep, and Hibernate power modes. The MCWDTs are clocked by LFCLK (ILO or WCO). It can do periodic interrupt/wakeup generation in system LP/ULP and Deep Sleep power modes.

### 3.2.8 Clock dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are:

- Eight 8-bit clock dividers
- Sixteen 16-bit integer clock dividers
- Four 16.5-bit fractional clock dividers
- One 24.5-bit fractional clock divider

### 3.2.9 Trigger routing

PSOC™ 6 MCU contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

There are two types of trigger routing. Trigger multiplexers have reconfigurability in the source and destination. There are also hardwired switches called “one-to-one triggers”, which connect a specific source to a destination. The user can enable or disable the route.

### 3.2.10 Reset

PSOC™ 6 MCU can be reset from a variety of sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up
- Brown-out detect (BOD) reset to monitor the digital voltage supply $V_{DDD}$ and generate a reset if $V_{DDD}$ falls below the minimum required logic operating voltage
- External reset dedicated pin (XRES) to reset the device using an external source. The XRES pin is active low. It can be connected either to a pull-up resistor to $V_{DDD}$, or to an active drive circuit, as Figure 6 shows. If a pull-up resistor is used, select its value to minimize current draw when the pin is pulled low; 4.7 kΩ to 100 kΩ is typical

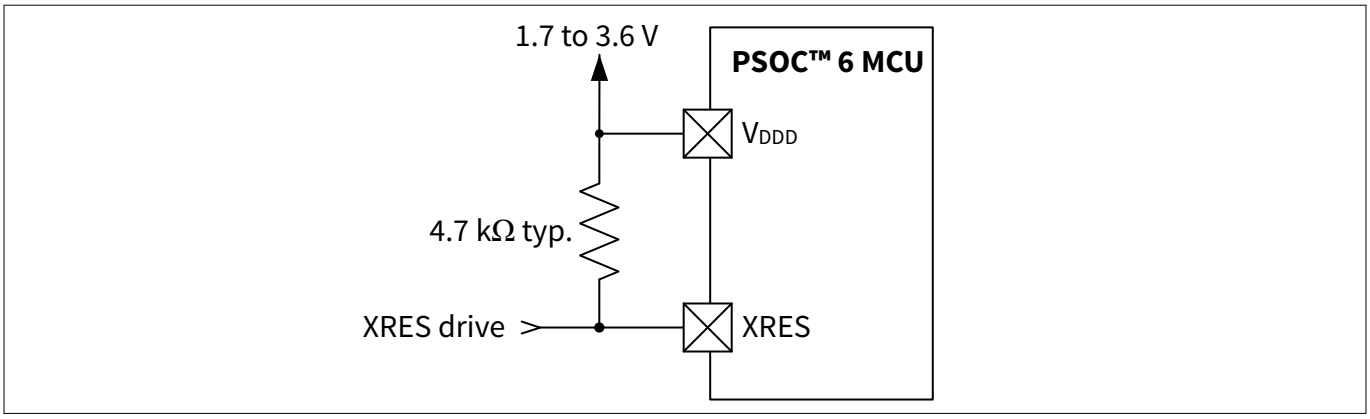



**Figure 6 XRES connection diagram**

- Watchdog timer (WDT or MCWDT) to reset the device if firmware fails to service it within a specified timeout period
- Software-initiated reset to reset the device on demand using firmware
- Logic-protection fault can trigger an interrupt or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code
- Hibernate wakeup reset to bring the device out of the system Hibernate low-power mode

Reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows software to determine the cause of the reset.

## 3.3 Programmable analog subsystem

### 3.3.1 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion. One of three internal references may be used for the ADC reference voltage: $V_{DDA}$, $V_{DDA/2}$, and an analog reference (AREF). AREF is nominally 1.2 V, trimmed to ±1%; see Table 24. An external reference may also be used, by driving the $V_{REF}$ pin. When using $V_{DDA/2}$ or AREF as a reference, an external bypass capacitor may be connected to the $V_{REF}$ pin to improve performance in noisy conditions. These reference options allow ratio-metric readings or absolute readings at the accuracy of the reference used. The input range of the ADC is the full supply voltage between $V_{SS}$ and $V_{DDA}/V_{DDIOA}$. The SAR ADC may be configured with a mix of single-ended and differential signals in the same configuration.

The SAR ADC's sample-and-hold (S/H) aperture is programmable to allow sufficient time for signals with a high impedance to settle sufficiently, if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it.

The SAR is connected to a fixed set of pins through an input multiplexer. The multiplexer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The result of each channel is buffered, so that an interrupt may be triggered only when a full scan of all channels is complete. Also, a pair of range registers can be set to detect and cause an interrupt if an input exceeds a minimum and/or maximum value. This allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. The SAR can also be connected, under firmware control, to most other GPIO pins via the Analog Multiplexer Bus (AMUXBUS). The SAR is not available in Deep Sleep and Hibernate modes as it requires a high -speed clock (up to 18 MHz). The SAR operating range is 1.71 to 3.6 V.

ADC accuracy is affected by GPIO switching noise. To improve accuracy, implement the GPIO port restrictions listed in Table 7. In addition, there should be no switching outputs on ports 9 and 10.

### 3.3.2 Temperature sensor

An on-chip temperature sensor is part of the SAR and may be scanned by the SAR ADC. It consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor may be connected directly to the SAR ADC as one of the measurement channels. The ADC digitizes the temperature sensor's output and a Infineon-supplied software function may be used to convert the reading to temperature which includes calibration and linearization.

### 3.3.3 12-bit digital-analog converter

There is a 12-bit voltage mode DAC on the chip, which can settle in less than 2 µs. The DAC may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output using an opamp in the CTBm block.

### 3.3.4 Continuous Time Block mini (CTBm) with two opamps

This block consists of two opamps, which have their inputs and outputs connected to pins and other analog blocks, as Figure 7 shows. They have three power modes (high, medium, and low) and a comparator mode. The opamps can be used to buffer SAR inputs and DAC outputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware. The opamps also support operation in system Deep Sleep mode, with lower performance and reduced power consumption.

### 3.3.5 Low-power comparators

Two low-power comparators are provided, which can operate in all power modes. This allows other analog system resources to be disabled while retaining the ability to monitor external voltage levels during system Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Figure 7 shows an overview of the analog subsystem. This diagram is a high-level abstraction. See the architecture reference manual for detailed connectivity information.

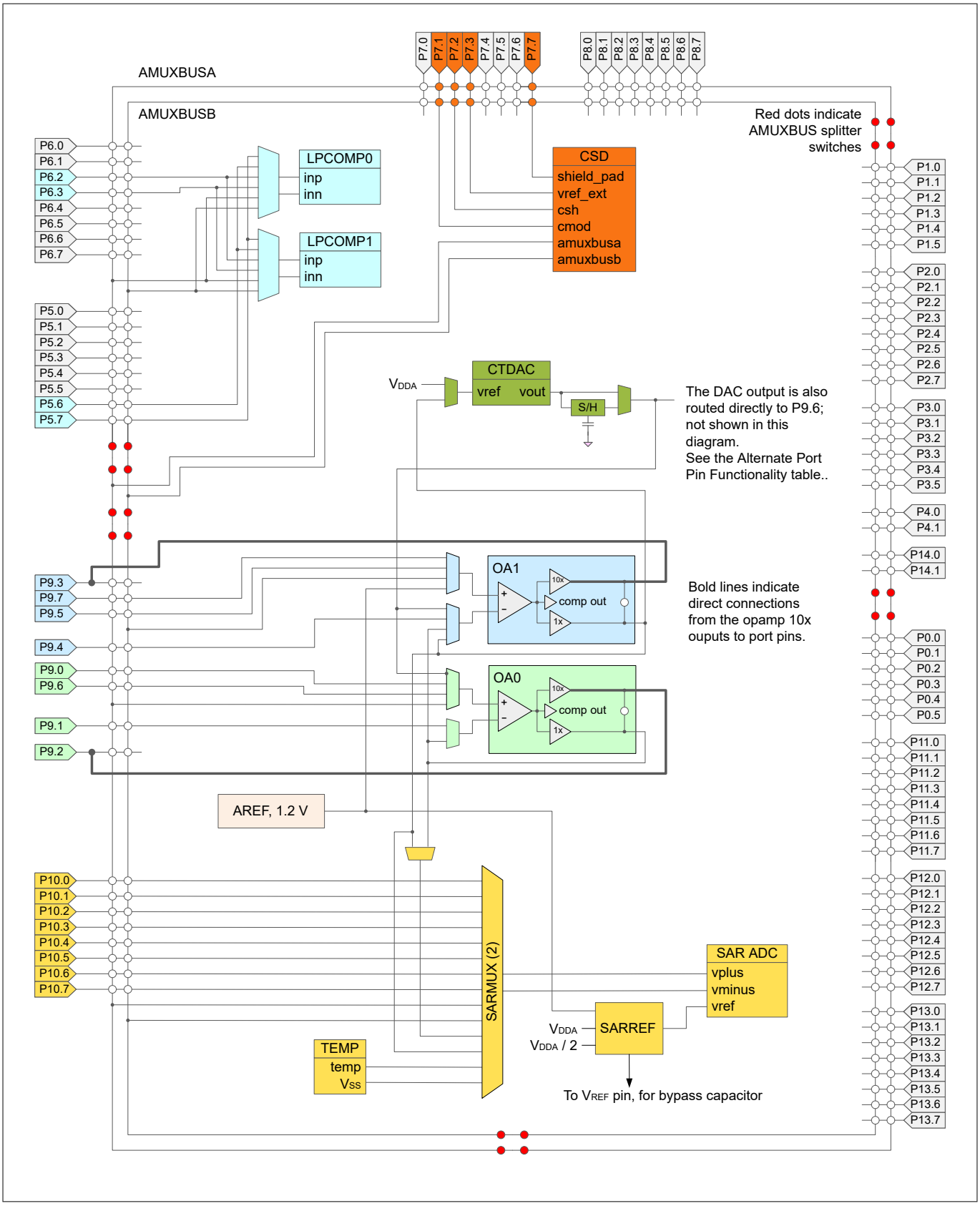



**Figure 7 Analog subsystem**

## 3.4 Programmable digital

### 3.4.1 Smart I/O

Smart I/O is a programmable logic fabric that enables Boolean operations on signals traveling from device internal resources to the GPIO pins or on signals traveling into the device from external sources. A Smart I/O block sits between the GPIO pins and the high-speed I/O matrix (HSIOM) and is dedicated to a single port.

There are two Smart I/O blocks: one on Port 8 and one on Port 9. When Smart I/O is not enabled, all signals on Port 8 and Port 9 bypass the Smart I/O hardware.

Smart I/O supports:

- System Deep Sleep operation
- Boolean operations without CPU intervention
- Asynchronous or synchronous (clocked) operation

Each Smart I/O block contains a data unit (DU) and eight lookup tables (LUTs).

The DU:

- Performs unique functions based on a selectable opcode
- Can source input signals from internal resources, the GPIO port, or a value in the DU register

Each LUT:

- Has three selectable input sources. The input signals may be sourced from another LUT, an internal resource, an external signal from a GPIO pin, or from the DU
- Acts as a programmable Boolean logic table
- Can be synchronous or asynchronous

### 3.4.2 Universal digital blocks (UDBs)

This product line has 12 UDBs. Each UDB is a collection of uncommitted logic (PLD) and nano-CPU (datapath) optimized to create common embedded peripherals and custom functionality, as Figure 8 shows. UDB datapaths are 8 bits wide, and can be chained to form 16, 24, and 32-bit functions. Included with the UDBs is the digital system interconnect (DSI), which routes signals among UDBs, fixed function peripherals, I/O pins and other system blocks to implement full featured device connectivity. The DSI enables routing between any digital function and any pin. Port adapter blocks extend the UDBs to provide an interface to the GPIOs through the HSIOM.

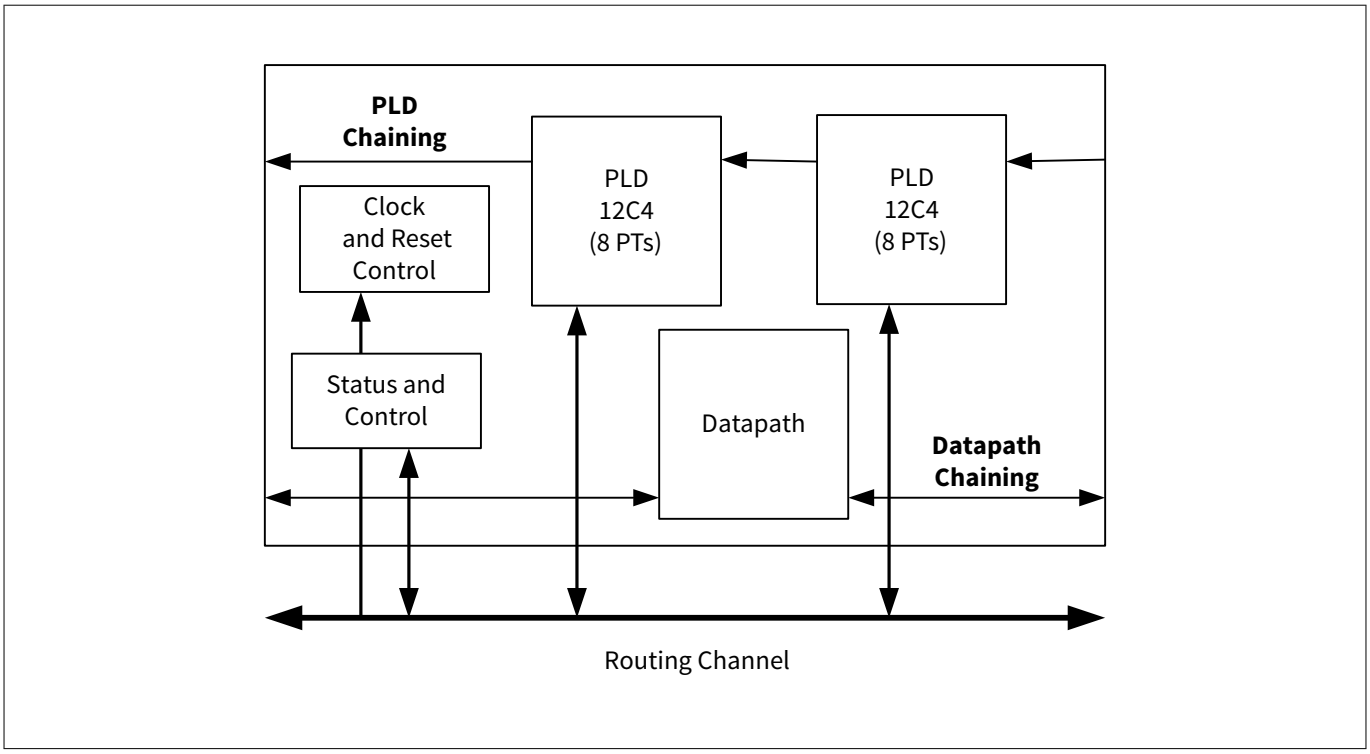



**Figure 8 UDB block diagram**

## 3.5 Fixed-function digital

### 3.5.1 Timer/counter/pulse-width modulator (TCPWM) block

- The TCPWM supports the following operational modes:
  - Timer-counter with compare
  - Timer-counter with capture
  - Quadrature decoding
  - Pulse width modulation (PWM)
  - Pseudo-random PWM
  - PWM with dead time
- Up, down, and up/down counting modes
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
  - Terminal count – Depends on the mode; typically occurs on overflow or underflow
  - Capture/compare – The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM; with rising edge, falling edge, both edges, and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state

In this device there are:

- Eight 32-bit TCPWMs
- Twenty-four 16-bit TCPWMs

### 3.5.2 Serial Communication Blocks (SCB)

This product line has nine SCBs:

- Eight can implement either I²C, UART, or SPI
- One SCB (SCB #8) can operate in system Deep Sleep mode with an external clock; this SCB can be either SPI slave or I²C slave

**I²C mode:** The SCB can implement a full multi-master and slave interface (it is capable of multimaster arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). It also supports EZI2C, which creates a mailbox address range and effectively reduces I²C communication to reading from and writing to an array in the memory.The SCB supports a 256-byte FIFO for receive and transmit.

The I²C peripheral is compatible with I²C standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

**UART mode:** This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.

**SPI mode:** The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block supports an EZSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with a 25-MHz clock.

### 3.5.3 USB Full-Speed device/host Interface

PSOC™ 6 has a USB full-speed interface that can be configured either as a USB device or a USB host. The USB device can have up to eight endpoints. A 512-byte SRAM buffer is provided, and DMA-based data transfer is supported. The USB host supports both full-speed (12 Mbps) and low-speed (1.5 Mbps) devices, and is designed to be compliant with USB Specification Revision 2.0. For more details on USB device/host features, see Technical Reference Manual.

***Note**: The USB pins are not frozen in system hibernate mode.*

### 3.5.4 QSPI Interface Serial Memory Interface (SMIF)

A serial memory interface is provided, running at up to 80 MHz. It supports single, dual, quad, dual-quad and octal SPI configurations, and supports up to four external memory devices. It supports two modes of operation:

- Memory-mapped I/O (MMIO), a command mode interface that provides data access via the SMIF registers and FIFOs
- Execute in Place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers

In XIP mode, the external memory is mapped into the PSOC™ 6 MCU internal address space, enabling code execution directly from the external memory. To improve performance, a 4-KB cache is included. XIP mode also supports AES-128 on-the-fly encryption and decryption, enabling secured storage and access of code and data in the external memory.

### 3.5.5 LCD

This block drives LCD commons and segments; routing is available to most of the GPIOs. One to eight of the GPIOs must be used for commons, the rest can be used for segments.

The LCD block has two modes of operation: high speed (8 MHz) and low speed (32 kHz). Both modes operate in system LP and ULP modes. Low-speed mode operates with reduced contrast in system Deep Sleep mode- review the number of common and segment lines, viewing angle requirements, and prototype performance before using this mode.

## 3.6 GPIO

This product line has up to 100 GPIOs, which implement:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Hold mode for latching previous state (used for retaining the I/O state in system Hibernate mode)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are up to 8 pins in width. Data output and pin state registers store, respectively, the values to be driven on the pins and the input states of the pins.

Every pin can generate an interrupt if enabled; each port has an interrupt request (IRQ) associated with it.

The port 1 pins are capable of overvoltage-tolerant (OVT) operation, where the input voltage may be higher than $V_{DDD}$. OVT pins are commonly used with $I^2C$, to allow powering the chip OFF while maintaining a physical connection to an operating $I^2C$ bus without affecting its functionality.

GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than the absolute maximum; see Electrical specifications.

During power-on and reset, the pins are forced to the analog input drive mode, with input and output buffers disabled, so as not to crowbar any inputs and/or cause excess turn-on current.

A multiplexing network known as the high-speed I/O matrix (HSIOM) is used to multiplex between various peripheral and analog signals that may connect to an I/O pin.

Analog performance is affected by GPIO switching noise. In order to get the best analog performance, the following frequency and drive mode constraints must be applied. The DRIVE_SEL values (refer to Table 7) represent drive strengths (see the architecture and register reference manuals for further detail).

See also Table 6 for additional restrictions for ECO use.

**Table 7 DRIVE_SEL values**

| Ports | Max frequency | Drive strength for $V_{DDD} \leq 2.7$ V | Drive strength for $V_{DDD} > 2.7$ V |
|---|---|---|---|
| Port 0 | 8 MHz | DRIVE_SEL 2 | DRIVE_SEL 3 |

**(table continues...)**

**Table 7 (continued) DRIVE_SEL values**

| Ports | Max frequency | Drive strength for $V_{DDD} \leq 2.7$ V | Drive strength for $V_{DDD} > 2.7$ V |
|---|---|---|---|
| Port 1 | 1 MHz; slow slew rate, 2 outputs max | | |
| Port 2 | 50 MHz | | |
| Ports 3 to 10 | 16 MHz; 25 MHz for SPI | | |
| Ports 11 to 13 | 80 MHz for SMIF (QSPI). | DRIVE_SEL 1 | DRIVE_SEL 2 |
| Ports 9 and 10 | 8 MHz; slow slew rate setting for TQFP Packages for ADC performance | No restrictions | No restrictions |

## 3.7 Special-function peripherals

### 3.7.1 Audio subsystem

This subsystem consists of the following hardware blocks:

- One Inter-IC Sound ($I^2S$) interface
- Two pulse-density modulation (PDM) to pulse-code modulation (PCM) decoder channels

The $I^2S$ interface implements two independent hardware FIFO buffers – TX and RX, which can operate in master or slave mode. The following features are supported:

- Multiple data formats – $I^2S$, left-justified, Time Division Multiplexed (TDM) mode A, and TDM mode B
- Programmable channel/word lengths – 8/16/18/20/24/32 bits
- Internal/external clock operation. Up to 192 ksps
- Interrupt mask events – trigger, not empty, full, overflow, underflow, watchdog
- Configurable FIFO trigger level with DMA support

The $I^2S$ interface is commonly used to connect with audio codecs, simple DACs, and digital microphones.

The PDM-to-PCM decoder implements a single hardware Rx FIFO that decodes a stereo or mono 1-bit PDM input stream to PCM data output. The following features are supported:

- Programmable data output word length – 16/18/20/24 bits
- Programmable gain amplifier (PGA) for volume control – from –12 dB to +10.5 dB in 1.5 dB steps
- Configurable PDM clock generation. Range from 384 kHz to 3.072 MHz
- Droop correction and configurable decimation rate for sampling; up to 48 ksps
- Programmable high-pass filter gain
- Interrupt mask events – not empty, overflow, trigger, underflow
- Configurable FIFO trigger level with DMA support

The PDM-to-PCM decoder is commonly used to connect to digital PDM microphones. Up to two microphones can be connected to the same PDM Data line.

### 3.7.2 CAPSENSE™ subsystem

CAPSENSE™ is supported in PSOC™ 6 MCU through a CAPSENSE™ sigma-delta (CSD) hardware block. It is designed for high-sensitivity self-capacitance and mutual-capacitance measurements, and is specifically built for user interface solutions.

In addition to CAPSENSE™, the CSD hardware block supports three general-purpose functions. These are available when CAPSENSE™ is not being used. Alternatively, two or more functions can be time-multiplexed in an application under firmware control. The four functions supported by the CSD hardware block are:

- CAPSENSE™
- 10-bit ADC
- Programmable current sources (IDAC)
- Comparator

**CAPSENSE™**

Capacitive touch sensors are designed for user interfaces that rely on human body capacitance to detect the presence of a finger on or near a sensor. CAPSENSE™ solutions bring elegant, reliable, and simple capacitive touch sensing functions to applications including IoT, industrial, automotive, and home appliances.

The CAPSENSE™ technology offers the following features:

- Best-in-class signal-to-noise ratio (SNR) and robust sensing under harsh and noisy conditions
- Self-capacitance (CSD) and mutual-capacitance (CSX) sensing methods
- Support for various widgets, including buttons, matrix buttons, sliders, touchpads, and proximity sensors
- High-performance sensing across a variety of materials
- Best-in-class liquid tolerance
- SmartSense auto-tuning technology that helps avoid complex manual tuning processes
- Superior immunity against external noise
- Spread-spectrum clocks for low radiated emissions
- Gesture and built-in self-test libraries
- Ultra-low power consumption
- An integrated graphical CAPSENSE™ tuner for real-time tuning, testing, and debugging

CAPSENSE™ sensitivity and accuracy are affected by GPIO switching noise. To improve sensitivity and accuracy, implement the GPIO port restrictions listed in Table 7, and do the following:

- Restrict CAPSENSE™ pins to ports 6 and 7
- There should be no other GPIO output activity on ports 6 and 7
- There should be no more than two GPIO outputs on ports 5 and 8
- Restrict GPIO output switching in ports 5 and 8 to 1 MHz, with slow slew rate setting

**ADC**

The CAPSENSE™ subsystem slope ADC offers the following features:

- Selectable 8- or 10-bit resolution
- Selectable input range: GND to $V_{REF}$ and GND to $V_{DDA}$ on any GPIO input
- Measurement of $V_{DDA}$ against an internal reference without the use of GPIO or external components

**IDAC**

The CSD block has two programmable current sources, which offer the following features:

- 7-bit resolution
- Sink and source current modes
- A current source programmable from 37.5 nA to 609 µA
- Two IDACs that can be used in parallel to form one 8-bit IDAC

**Comparator**

The CAPSENSE™ subsystem comparator operates in the system Low Power and Ultra-Low Power modes. The inverting input is connected to an internal programmable reference voltage and the non-inverting input can be connected to any GPIO via the AMUXBUS.

### CAPSENSE™ hardware subsystem

Figure 9 shows the high-level hardware overview of the CAPSENSE™ subsystem, which includes a delta sigma converter, internal clock dividers, a shield driver, and two programmable current sources.

The inputs are managed through analog multiplexed buses (AMUXBUS A/B). The input and output of all functions offered by the CSD block can be provided on any GPIO or on a group of GPIOs under software control, with the exception of the comparator output and external capacitors that use dedicated GPIOs.

Self-capacitance is supported by the CSD block using AMUXBUS A, an external modulator capacitor, and a GPIO for each sensor. There is a shield electrode (optional) for self-capacitance sensing. This is supported using AMUXBUS B and an optional external shield tank capacitor (to increase the drive capability of the shield driver) should this be required. Mutual-capacitance is supported by the CSD block using AMUXBUS A, two external integrated capacitors, and a GPIO for transmit and receive electrodes.

The ADC does not require an external component. Any GPIO that can be connected to AMUXBUS A can be an input to the ADC under software control. The ADC can accept $V_{DDA}$ as an input without needing GPIOs (for applications such as battery voltage measurement).

The two programmable current sources (IDACs) in general-purpose mode can be connected to AMUXBUS A or B. They can therefore connect to any GPIO pin. The comparator resides in the delta-sigma converter. The comparator inverting input can be connected to the reference. Both comparator inputs can be connected to any GPIO using AMUXBUS B; see Figure 9. The reference has a direct connection to a dedicated GPIO; see Table 10.

The CSD block can operate in active and sleep CPU power modes, and seamlessly transition between system LP and ULP modes. It can be powered down in system Deep Sleep and Hibernate modes. Upon wakeup from Hibernate mode, the CSD block requires re-initialization. However, operation can be resumed without re-initialization upon exit from Deep Sleep mode, under firmware control.

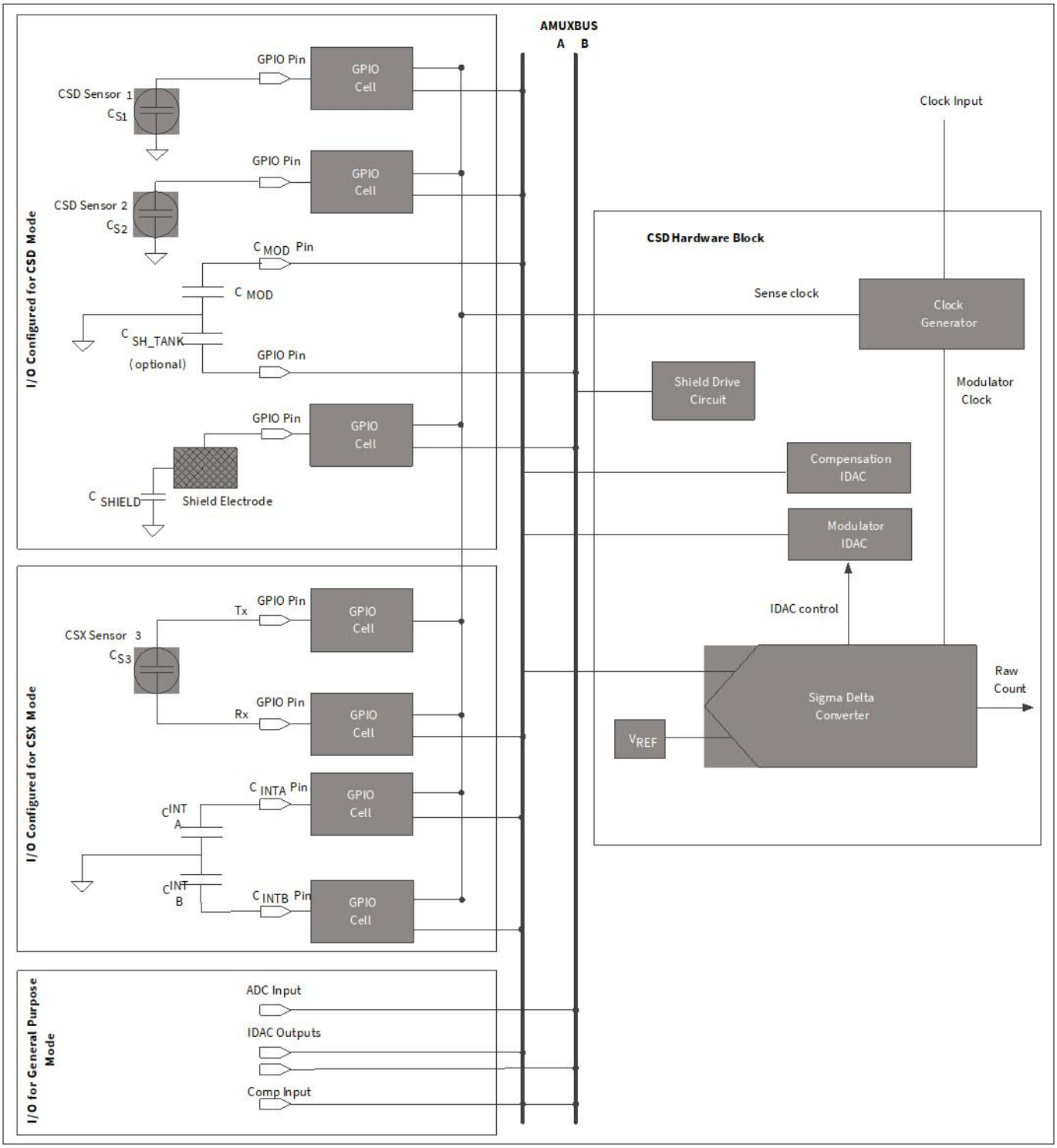



**Figure 9 CAPSENSE™ hardware subsystem**

Figure 10 shows the high-level software overview. Infineon provides middleware libraries for CAPSENSE™, ADC, and IDAC on GitHub to enable quick integration. The Board Support Package for any kit with CAPSENSE™ capabilities automatically includes the CAPSENSE™ library in any application that uses the BSP.

User applications interact only with middleware to implement functions of the CSD block. The middleware interacts with underlying drivers to access hardware as necessary. The CSD driver facilitates time-multiplexing of the CSD hardware if more than one piece of CSD-related middleware is present in a project. It prevents access conflicts in this case.

ModusToolbox™ software provides a CAPSENSE™ configurator to enable fast library configuration. It also provides a tuner for performance evaluation and real-time tuning of the system. The tuner requires an EZI2C communication interface in the application to enable real-time tuning capability. The tuner can update configuration parameters directly in the device as well as in the configurator.

CAPSENSE™ and ADC middleware use the CSD interrupt to implement non-blocking sensing and A-to-D conversion. Therefore, interrupt service routines are a defined part of the middleware, which must be initialized by the application. Middleware and drivers can operate on either CPU. Infineon recommends using the middleware only in one CPU. If both CPUs must access the CSD driver, memory access should be managed in the application.

Refer to AN85951: PSOC™ 4 and PSOC™ 6 MCU CAPSENSE™ design guide for more details on CSX sensing, CSD sensing, shield electrode usage and its benefits, and capacitive system design guidelines.

Refer to the API reference guides for CAPSENSE™, ADC, and IDAC available on GitHub.

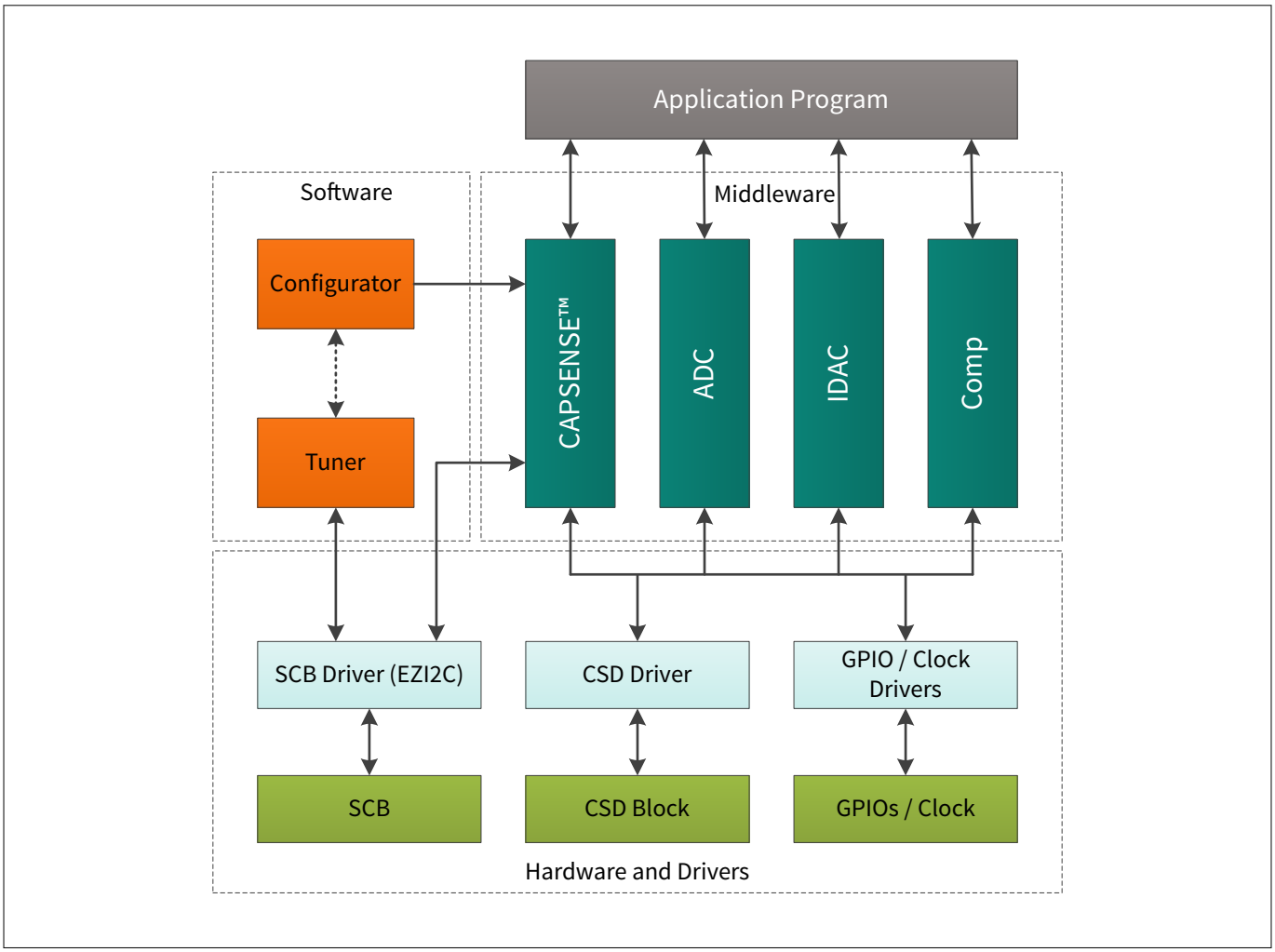



**Figure 10 CAPSENSE™ software/firmware subsystem**

# 4 Pinouts

***Note**: The CY8C62x6/CY8C62x7 Table 8 and Table 9 contains a spreadsheet with a consolidated list of pinouts and pin alternate functions with HSIOM mapping.*

GPIO ports are powered by $V_{DDx}$ pins as follows:

- P0: $V_{BACKUP}$
- P1: $V_{DDD}$. Port 1 pins are overvoltage tolerant (OVT)
- P2, P3, P4: $V_{DDIO2}$
- P5, P6, P7, P8: $V_{DDIO1}$
- P9, P10: $V_{DDIOA}$, $V_{DDA}$($V_{DDIOA}$, when present, and $V_{DDA}$ must be connected together on the PCB)
- P11, P12, P13: $V_{DDIO0}$
- P14: $V_{DDUSB}$

**Table 8 Packages and pin information**

| Pin | Packages | |
|---|---|---|
| | **124-BGA** | **80-WLCSP** |
| $V_{DDD}$ | A1 | B11 |
| $V_{CCD}$ | A2 | A10 |
| $V_{DDA}$ | A12 | F1 |
| $V_{DDIOA}$ | A13 | - |
| $V_{DDIO0}$ | C4 | A6 |
| $V_{DDIO1}$ | K12 | M1 |
| $V_{DDIO2}$ | L4 | - |
| $V_{BACKUP}$ | D1 | D11 |
| $V_{DDUSB}$ | M1 | P11 |
| $V_{SS}$ | B12, C3, D4, D10, K4, K10 | A8, D1, P5, R8 |
| $V_{DD_NS}$ | J1 | K11 |
| $V_{IND1}$ | J2 | L10 |
| $V_{IND2}$ | K2 | M11 |
| $V_{BUCK1}$ | K3 | N10 |
| $V_{RF}$ | K1 | - |
| XRES | F1 | G10 |
| $V_{REF}$ | B13 | - |
| P0.0 | E3 | C10 |
| P0.1 | E2 | D9 |
| P0.2 | E1 | E10 |
| P0.3 | F3 | F9 |
| P0.4 | F2 | G8 |

**(table continues...)**

**Table 8 (continued) Packages and pin information**

| Pin | Packages | |
|---|---|---|
| | 124-BGA | 80-WLCSP |
| P0.5 | G3 | F11 |
| P1.0 | G2 | H11 |
| P1.1 | G1 | H9 |
| P1.2 | H3 | - |
| P1.3 | H2 | - |
| P1.4 | H1 | K9 |
| P1.5 | J3 | J10 |
| P2.0 | M2 | - |
| P2.1 | N2 | - |
| P2.2 | L3 | - |
| P2.3 | M3 | - |
| P2.4 | N3 | - |
| P2.5 | N1 | - |
| P2.6 | M4 | - |
| P2.7 | N4 | - |
| P3.0 | L5 | - |
| P3.1 | M5 | - |
| P3.2 | N5 | - |
| P3.3 | L6 | - |
| P3.4 | M6 | - |
| P3.5 | N6 | - |
| P4.0 | L7 | - |
| P4.1 | M7 | - |
| P5.0 | N7 | M9 |
| P5.1 | L8 | N8 |
| P5.2 | M8 | R6 |
| P5.3 | N8 | P7 |
| P5.4 | L9 | L8 |
| P5.5 | M9 | M7 |
| P5.6 | N9 | R4 |
| P5.7 | N10 | N6 |
| P6.0 | M10 | J8 |

**(table continues...)**

**Table 8 (continued) Packages and pin information**

| Pin | Packages | |
|---|---|---|
| | 124-BGA | 80-WLCSP |
| P6.1 | L10 | K7 |
| P6.2 | L11 | L6 |
| P6.3 | M11 | R2 |
| P6.4 | N11 | P3 |
| P6.5 | M12 | N4 |
| P6.6 | N12 | M5 |
| P6.7 | M13 | J6 |
| P7.0 | L13 | N2 |
| P7.1 | L12 | M3 |
| P7.2 | K13 | L4 |
| P7.3 | N13 | K5 |
| P7.4 | K11 | - |
| P7.5 | J13 | - |
| P7.6 | J12 | - |
| P7.7 | J11 | L2 |
| P8.0 | H13 | H3 |
| P8.1 | H12 | K1 |
| P8.2 | H11 | K3 |
| P8.3 | G13 | J4 |
| P8.4 | G12 | J2 |
| P8.5 | G11 | - |
| P8.6 | F13 | - |
| P8.7 | F12 | - |
| P9.0 | E11 | H1 |
| P9.1 | E12 | G2 |
| P9.2 | E13 | E2 |
| P9.3 | F11 | C2 |
| P9.4 | D13 | F3 |
| P9.5 | D12 | - |
| P9.6 | D11 | - |
| P9.7 | C13 | A2 |
| P10.0 | C12 | G4 |

**(table continues...)**

**Table 8 (continued) Packages and pin information**

| Pin | Packages | |
|---|---|---|
| | 124-BGA | 80-WLCSP |
| P10.1 | A11 | H5 |
| P10.2 | B11 | - |
| P10.3 | C11 | - |
| P10.4 | A10 | B3 |
| P10.5 | B10 | D3 |
| P10.6 | C10 | - |
| P10.7 | A9 | - |
| P11.0 | B9 | E4 |
| P11.1 | C9 | F5 |
| P11.2 | A8 | G6 |
| P11.3 | B8 | A4 |
| P11.4 | C8 | C4 |
| P11.5 | A7 | B5 |
| P11.6 | B7 | D5 |
| P11.7 | C7 | C6 |
| P12.0 | A6 | B7 |
| P12.1 | B6 | D7 |
| P12.2 | C6 | C8 |
| P12.3 | A5 | B9 |
| P12.4 | B5 | E6 |
| P12.5 | C5 | E8 |
| P12.6 | A4 | F7 |
| P12.7 | B4 | H7 |
| P13.0 | B1 | - |
| P13.1 | A3 | - |
| P13.2 | B3 | - |
| P13.3 | B2 | - |
| P13.4 | C2 | - |
| P13.5 | C1 | - |
| P13.6 | D3 | - |
| P13.7 | D2 | - |
| P14.0/USBDP | L2 | R10 |
| P14.1/USBDM | L1 | P9 |

***Note**: If the USB pins are not used, connect $V_{DDUSB}$ to ground and leave the P14.0/USBDP and P14.1/USBDM pins unconnected.*

Each port pin has multiple alternate functions. These are defined in Table 9.

**Table 9 Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P0.0 | tcpwm[0].line[0]:0 | tcpwm[1].line[0]:0 | | srss.ext_clk:0 | | | | scb[0].spi_select1:0 | | | peri.tr_io_input[0]:0 | | | | | | |
| P0.1 | tcpwm[0].line_compl[0]:0 | tcpwm[1].line_compl[0]:0 | | | | | | scb[0].spi_select2:0 | | | peri.tr_io_input[1]:0 | | | | | cpuss.swj_trstn | |
| P0.2 | tcpwm[0].line[1]:0 | tcpwm[1].line[1]:0 | | | | scb[0].uart_rx:0 | scb[0].i2c_scl:0 | scb[0].spi_mosi:0 | | | | | | | | | |
| P0.3 | tcpwm[0].line_compl[1]:0 | tcpwm[1].line_compl[1]:0 | | | | scb[0].uart_tx:0 | scb[0].i2c_sda:0 | scb[0].spi_miso:0 | | | | | | | | | |
| P0.4 | tcpwm[0].line[2]:0 | tcpwm[1].line[2]:0 | | | | scb[0].uart_rts:0 | | scb[0].spi_clk:0 | | | | peri.tr_io_output[0]:2 | | | | | |
| P0.5 | tcpwm[0].line_compl[2]:0 | tcpwm[1].line_compl[2]:0 | | srss.ext_clk:1 | | scb[0].uart_cts:0 | | scb[0].spi_select0:0 | | | | peri.tr_io_output[1]:2 | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P1.0 | tcpwm[0].line[3]:0 | tcpwm[1].line[3]:0 | | | | scb[7].uart_rx:0 | scb[7].i2c_scl:0 | scb[7].spi_mosi:0 | | | peri.tr_io_input[2]:0 | | | | | | |
| P1.1 | tcpwm[0].line_compl[3]:0 | tcpwm[1].line_compl[3]:0 | | | | scb[7].uart_tx:0 | scb[7].i2c_sda:0 | scb[7].spi_miso:0 | | | peri.tr_io_input[3]:0 | | | | | | |
| P1.2 | tcpwm[0].line[4]:4 | tcpwm[1].line[12]:1 | | | | scb[7].uart_rts:0 | | scb[7].spi_clk:0 | | | | | | | | | |
| P1.3 | tcpwm[0].line_compl[4]:4 | tcpwm[1].line_compl[12]:1 | | | | scb[7].uart_cts:0 | | scb[7].spi_select0:0 | | | | | | | | | |
| P1.4 | tcpwm[0].line[5]:4 | tcpwm[1].line[13]:1 | | | | | | scb[7].spi_select1:0 | | | | | | | | | |
| P1.5 | tcpwm[0].line_compl[5]:4 | tcpwm[1].line_compl[14]:1 | | | | | | scb[7].spi_select2:0 | | | | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P2.0 | tcpwm[0].line[6]:4 | tcpwm[1].line[15]:1 | | | | scb[1].uart_rx:0 | scb[1].i2c_scl:0 | scb[1].spi_mosi:0 | | | peri.tr_io_input[4]:0 | | | | bless.mxd_dpslp_ret_switch_hv | | |
| P2.1 | tcpwm[0].line_-compl[ | tcpwm[1].line_compl[15]:1 | | | | scb[1].uart_tx:0 | scb[1].i2c_sda:0 | scb[1].spi_miso:0 | | | peri.tr_io_input[5]:0 | | | | bless.mxd_dpslp_ret_ldo_ol_hv | | |
| P2.2 | tcpwm[0].line[7]:4 | tcpwm[1].line[16]:1 | | | | scb[1].uart_rts:0 | | scb[1].spi_clk:0 | | | | | | | bless.mxd_dpslp_-buck_en | | |
| P2.3 | tcpwm[0].line_-compl[7]:4 | tcpwm[1].line_compl[16]:1 | | | | scb[1].uart_cts:0 | | scb[1].spi_select0:0 | | | | | | | bless.mxd_dpslp_reset_n | | |
| P2.4 | tcpwm[0].line[0]:5 | tcpwm[1].line[17]:1 | | | | | | scb[1].spi_select1:0 | | | | | | | bless.mxd_dpslp_-clk_en | | |
| P2.5 | tcpwm[0].line_-compl[0]:5 | tcpwm[1].line_compl[17]:1 | | | | | | scb[1].spi_select2:0 | | | | | | | bless.mxd_dpslp_isolate_n | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P2.6 | tcpwm[0].line[1]:5 | tcpwm[1].line[18]:1 | | | | | | scb[1].spi_select3:0 | | | | | | | bless.mxd_dpslp_act_ldo_en | | |
| P2.7 | tcpwm[0].line_-compl[1]:5 | tcpwm[1].line_compl[18]:1 | | | | | | | | | | | | | bless.mxd_dpslp_xtal_en | | |
| P3.0 | tcpwm[0].line[2]:5 | tcpwm[1].line[19]:1 | | | | scb[2].uart_rx:1 | scb[2].i2c_scl:1 | scb[2].spi_mosi:1 | | | peri.tr_io_input[6]:0 | | | | bless.mxd_dpslp_dig_ldo_en | | |
| P3.1 | tcpwm[0].line_compl[2]:5 | tcpwm[1].line_compl[19]:1 | | | | scb[2].uart_tx:1 | scb[2].i2c_sda:1 | scb[2].spi_miso:1 | | | peri.tr_io_input[7]:0 | | bless.mxd_act_dbus_rx_en | | | | |
| P3.2 | tcpwm[0].line[3]:5 | tcpwm[1].line[20]:1 | | | | scb[2].uart_rts:1 | | scb[2].spi_clk:1 | | | | | bless.mxd_act_dbus_tx_en | | | | |
| P3.3 | tcpwm[0].line_compl[3]:5 | tcpwm[1].line_compl[20]:1 | | | | scb[2].uart_cts:1 | | scb[2].spi_select0:1 | | | | | bless.mxd_act_bpktctl | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P3.4 | tcpwm[0].line[4]:5 | tcpwm[1].line[21]:1 | | | | | | scb[2].spi_select1:1 | | | | | bless.mxd_act_txd_rxd | | | | |
| P3.5 | tcpwm[0].line_compl[4]:5 | tcpwm[1].line_compl[21]:1 | | | | | | scb[2].spi_select2:1 | | | | | bless.mxd_dpslp_rcb_data | | | | |
| P4.0 | tcpwm[0].line[5]:5 | tcpwm[1].line[22]:1 | | | | scb[7].uart_rx:1 | scb[7].i2c_scl:1 | scb[7].spi_mosi:1 | | | peri.tr_io_input[8]:0 | | bless.mxd_dpslp_rcb_clk | | | | |
| P4.1 | tcpwm[0].line_compl[5]:5 | tcpwm[1].line_compl[22]:1 | | | | scb[7].uart_tx:1 | scb[7].i2c_sda:1 | scb[7].spi_miso:1 | | | peri.tr_io_input[9]:0 | | bless.mxd_dpslp_rcb_le | | | | |
| P5.0 | tcpwm[0].line[4]:0 | tcpwm[1].line[4]:0 | | | | scb[5].uart_rx:0 | scb[5].i2c_scl:0 | scb[5].spi_mosi:0 | | audioss.clk_i2s_if | peri.tr_io_input[10]:0 | | | | | | |
| P5.1 | tcpwm[0].line_compl[4]:0 | tcpwm[1].line_compl[4]:0 | | | | scb[5].uart_tx:0 | scb[5].i2c_sda:0 | scb[5].spi_miso:0 | | audioss.tx_sck | peri.tr_io_input[11]:0 | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P5.2 | tcpwm[0].line[5]:0 | tcpwm[1].line[5]:0 | | | | scb[5].uart_rts:0 | | scb[5].spi_clk:0 | | audioss.tx_ws | | | | | | | |
| P5.3 | tcpwm[0].line_compl[5]:0 | tcpwm[1].line_compl[5]:0 | | | | scb[5].uart_cts:0 | | scb[5].spi_select0:0 | | audioss.tx_sdo | | | | | | | |
| P5.4 | tcpwm[0].line[6]:0 | tcpwm[1].line[6]:0 | | | | | | scb[5].spi_select1:0 | | audioss.rx_sck | | | | | | | |
| P5.5 | tcpwm[0].line_compl[6]:0 | tcpwm[1].line_compl[6]:0 | | | | | | scb[5].spi_select2:0 | | audioss.rx_ws | | | | | | | |
| P5.6 | tcpwm[0].line[7]:0 | tcpwm[1].line[7]:0 | | | | | | scb[5].spi_select3:0 | | audioss.rx_sdi | | | | | | | |
| P5.7 | tcpwm[0].line_compl[7]:0 | tcpwm[1].line_compl[7]:0 | | | | | | scb[3].spi_select3:0 | | | | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P6.0 | tcpwm[0].line[0]:1 | tcpwm[1].line[8]:0 | scb[8].i2c_scl:0 | | | scb[3].uart_rx:0 | scb[3].i2c_scl:0 | scb[3].spi_mosi:0 | | | | cpuss.fault_out[0] | | | | | scb[8].spi_mosi:0 |
| P6.1 | tcpwm[0].line_compl[0]:1 | tcpwm[1].line_compl[8]:0 | scb[8].i2c_sda:0 | | | scb[3].uart_tx:0 | scb[3].i2c_sda:0 | scb[3].spi_miso:0 | | | | cpuss.fault_out[1] | | | | | scb[8].spi_miso:0 |
| P6.2 | tcpwm[0].line[1]:1 | tcpwm[1].line[9]:0 | | | | scb[3].uart_rts:0 | | scb[3].spi_clk:0 | | | | | | | | | scb[8].spi_clk:0 |
| P6.3 | tcpwm[0].line_compl[1]:1 | tcpwm[1].line_compl[9]:0 | | | | scb[3].uart_cts:0 | | scb[3].spi_select0:0 | | | | | | | | | scb[8].spi_select0:0 |
| P6.4 | tcpwm[0].line[2]:1 | tcpwm[1].line[10]:0 | scb[8].i2c_scl:1 | | | scb[6].uart_rx:2 | scb[6].i2c_scl:2 | scb[6].spi_mosi:2 | | | peri.tr_io_input[12]:0 | peri.tr_io_output[0]:1 | | | | cpuss.swj_swo_tdo | scb[8].spi_mosi:1 |
| P6.5 | tcpwm[0].line_compl[2]:1 | tcpwm[1].line_compl[10]:0 | scb[8].i2c_sda:1 | | | scb[6].uart_tx:2 | scb[6].i2c_sda:2 | scb[6].spi_miso:2 | | | peri.tr_io_input[13]:0 | peri.tr_io_output[1]:1 | | | | cpuss.swj_swdoe_tdi | scb[8].spi_miso:1 |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P6.6 | tcpwm[0].line[3]:1 | tcpwm[1].line[11]:0 | | | | scb[6].uart_rts:2 | | scb[6].spi_clk:2 | | | | | | | | cpuss.swj_swdio_tms | scb[8].spi_clk:1 |
| P6.7 | tcpwm[0].line_compl[3]:1 | tcpwm[1].line_compl[11]:0 | | | | scb[6].uart_cts:2 | | scb[6].spi_select0:2 | | | | | | | | cpuss.swj_swclk_tclk | scb[8].spi_select0:1 |
| P7.0 | tcpwm[0].line[4]:1 | tcpwm[1].line[12]:0 | | | | scb[4].uart_rx:1 | scb[4].i2c_scl:1 | scb[4].spi_mosi:1 | | | peri.tr_io_input[14]:0 | | cpuss.trace_clock | | | | |
| P7.1 | tcpwm[0].line_compl[4]:1 | tcpwm[1].line_compl[12]:0 | | | | scb[4].uart_tx:1 | scb[4].i2c_sda:1 | scb[4].spi_miso:1 | | | peri.tr_io_input[15]:0 | | | | | | |
| P7.2 | tcpwm[0].line[5]:1 | tcpwm[1].line[13]:0 | | | | scb[4].uart_rts:1 | | scb[4].spi_clk:1 | | | | | | | | | |
| P7.3 | tcpwm[0].line_compl[5]:1 | tcpwm[1].line_compl[13]:0 | | | | scb[4].uart_cts:1 | | scb[4].spi_select0:1 | | | | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P7.4 | tcpwm[0].line[6]:1 | tcpwm[1].line[14]:0 | | | | | | scb[4].spi_select1:1 | | | | | bless.ext_lna_rx_ctl_out | cpuss.trace_data[3]:2 | | | |
| P7.5 | tcpwm[0].line_compl[6]:1 | tcpwm[1].line_compl[14]:0 | | | | | | scb[4].spi_select2:1 | | | | | bless.ext_pa_tx_ctl_out | cpuss.trace_data[2]:2 | | | |
| P7.6 | tcpwm[0].line[7]:1 | tcpwm[1].line[15]:0 | | | | | | scb[4].spi_select3:1 | | | | | bless.ext_pa_lna_chip_en_out | cpuss.trace_data[1]:2 | | | |
| P7.7 | tcpwm[0].line_compl[7]:1 | tcpwm[1].line_compl[15]:0 | | | | | | scb[3].spi_select1:0 | cpuss.clk_fm_pump | | | | | cpuss.trace_data[0]:2 | | | |
| P8.0 | tcpwm[0].line[0]:2 | tcpwm[1].line[16]:0 | | | | scb[4].uart_rx:0 | scb[4].i2c_scl:0 | scb[4].spi_mosi:0 | | | peri.tr_io_input[16]:0 | | | | | | |
| P8.1 | tcpwm[0].line_compl[0]:2 | tcpwm[1].line_compl[16]:0 | | | | scb[4].uart_tx:0 | scb[4].i2c_sda:0 | scb[4].spi_miso:0 | | | peri.tr_io_input[17]:0 | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P8.2 | tcpwm[0].line[1]:2 | tcpwm[1].line[17]:0 | | | | scb[4].uart_rts:0 | | scb[4].spi_clk:0 | | | | | | | | | |
| P8.3 | tcpwm[0].line_compl[1]:2 | tcpwm[1].line_compl[17]:0 | | | | scb[4].uart_cts:0 | | scb[4].spi_select0:0 | | | | | | | | | |
| P8.4 | tcpwm[0].line[2]:2 | tcpwm[1].line[18]:0 | | | | | | scb[4].spi_select1:0 | | | | | | | | | |
| P8.5 | tcpwm[0].line_compl[2]:2 | tcpwm[1].line_compl[18]:0 | | | | | | scb[4].spi_select2:0 | | | | | | | | | |
| P8.6 | tcpwm[0].line[3]:2 | tcpwm[1].line[19]:0 | | | | | | scb[4].spi_select3:0 | | | | | | | | | |
| P8.7 | tcpwm[0].line_compl[3]:2 | tcpwm[1].line_compl[19]:0 | | | | | | scb[3].spi_select2:0 | | | | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P9.0 | tcpwm[0].line[4]:2 | tcpwm[1].line[20]:0 | | | | scb[2].uart_rx:0 | scb[2].i2c_scl:0 | scb[2].spi_mosi:0 | | | peri.tr_io_input[18]:0 | | | cpuss.trace_data[3]:0 | | | |
| P9.1 | tcpwm[0].line_compl[4]:2 | tcpwm[1].line_compl[20]:0 | | | | scb[2].uart_tx:0 | scb[2].i2c_sda:0 | scb[2].spi_miso:0 | | | peri.tr_io_input[19]:0 | | | cpuss.trace_data[2]:0 | | | |
| P9.2 | tcpwm[0].line[5]:2 | tcpwm[1].line[21]:0 | | | | scb[2].uart_rts:0 | | scb[2].spi_clk:0 | | pass.dsi_ctb_cmp0:1 | | | | cpuss.trace_data[1]:0 | | | |
| P9.3 | tcpwm[0].line_compl[5]:2 | tcpwm[1].line_compl[21]:0 | | | | scb[2].uart_cts:0 | | scb[2].spi_select0:0 | | pass.dsi_ctb_cmp1:1 | | | | cpuss.trace_data[0]:0 | | | |
| P9.4 | tcpwm[0].line[7]:5 | tcpwm[1].line[0]:2 | | | | | | scb[2].spi_select1:0 | | | | | | | | | |
| P9.5 | tcpwm[0].line_compl[7]:5 | tcpwm[1].line_compl[0]:2 | | | | | | scb[2].spi_select2:0 | | | | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P9.6 | tcpwm[0].line[0]:6 | tcpwm[1].line[1]:2 | | | | | | scb[2].spi_select3:0 | | | | | | | | | |
| P9.7 | tcpwm[0].line_compl[0]:6 | tcpwm[1].line_compl[1]:2 | | | | | | | | | | | | | | | |
| P10.0 | tcpwm[0].line[6]:2 | tcpwm[1].line[22]:0 | | | | scb[1].uart_rx:1 | scb[1].i2c_scl:1 | scb[1].spi_mosi:1 | | | peri.tr_io_input[20]:0 | | | cpuss.trace_data[3]:1 | | | |
| P10.1 | tcpwm[0].line_compl[6]:2 | tcpwm[1].line_compl[22]:0 | | | | scb[1].uart_tx:1 | scb[1].i2c_sda:1 | scb[1].spi_miso:1 | | | peri.tr_io_input[21]:0 | | | cpuss.trace_data[2]:1 | | | |
| P10.2 | tcpwm[0].line[7]:2 | tcpwm[1].line[23]:0 | | | | scb[1].uart_rts:1 | | scb[1].spi_clk:1 | | | | | | cpuss.trace_data[1]:1 | | | |
| P10.3 | tcpwm[0].line_compl[7]:2 | tcpwm[1].line_compl[23]:0 | | | | scb[1].uart_cts:1 | | scb[1].spi_select0:1 | | | | | | cpuss.trace_data[0]:1 | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P10.4 | tcpwm[0].line[0]:3 | tcpwm[1].line[0]:1 | | | | | | scb[1].spi_select1:1 | audioss.pdm_clk | | | | | | | | |
| P10.5 | tcpwm[0].line_compl[0]:3 | tcpwm[1].line_compl[0]:1 | | | | | | scb[1].spi_select2:1 | audioss.pdm_data | | | | | | | | |
| P10.6 | tcpwm[0].line[1]:6 | tcpwm[1].line[2]:2 | | | | | | scb[1].spi_select3:1 | | | | | | | | | |
| P10.7 | tcpwm[0].line_compl[1]:6 | tcpwm[1].line_compl[2]:2 | | | | | | | | | | | | | | | |
| P11.0 | tcpwm[0].line[1]:3 | tcpwm[1].line[1]:1 | | | smif.spi_select2 | scb[5].uart_rx:1 | scb[5].i2c_scl:1 | scb[5].spi_mosi:1 | | | peri.tr_io_input[22]:0 | | | | | | |
| P11.1 | tcpwm[0].line_compl[1]:3 | tcpwm[1].line_compl[1]:1 | | | smif.spi_select1 | scb[5].uart_tx:1 | scb[5].i2c_sda:1 | scb[5].spi_miso:1 | | | peri.tr_io_input[23]:0 | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P11.2 | tcpwm[0].line[2]:3 | tcpwm[1].line[2]:1 | | | smif.spi_select0 | scb[5].uart_rts:1 | | scb[5].spi_clk:1 | | | | | | | | | |
| P11.3 | tcpwm[0].line_compl[2]:3 | tcpwm[1].line_compl[2]:1 | | | smif.spi_data3 | scb[5].uart_cts:1 | | scb[5].spi_select0:1 | | | | peri.tr_io_output[0]:0 | | | | | |
| P11.4 | tcpwm[0].line[3]:3 | tcpwm[1].line[3]:1 | | | smif.spi_data2 | | | scb[5].spi_select1:1 | | | | peri.tr_io_output[1]:0 | | | | | |
| P11.5 | tcpwm[0].line_compl[3]:3 | tcpwm[1].line_compl[3]:1 | | | smif.spi_data1 | | | scb[5].spi_select2:1 | | | | | | | | | |
| P11.6 | | | | | smif.spi_data0 | | | scb[5].spi_select3:1 | | | | | | | | | |
| P11.7 | | | | | smif.spi_clk | | | | | | | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P12.0 | tcpwm[0].line[4]:3 | tcpwm[1].line[4]:1 | | | smif.spi_data4 | scb[6].uart_rx:0 | scb[6].i2c_scl:0 | scb[6].spi_mosi:0 | | | peri.tr_io_input[24]:0 | | | | | | |
| P12.1 | tcpwm[0].line_compl[4]:3 | tcpwm[1].line_compl[4]:1 | | | smif.spi_data5 | scb[6].uart_tx:0 | scb[6].i2c_sda:0 | scb[6].spi_miso:0 | | | peri.tr_io_input[25]:0 | | | | | | |
| P12.2 | tcpwm[0].line[5]:3 | tcpwm[1].line[5]:1 | | | smif.spi_data6 | scb[6].uart_rts:0 | | scb[6].spi_clk:0 | | | | | | | | | |
| P12.3 | tcpwm[0].line_compl[5]:3 | tcpwm[1].line_compl[5]:1 | | | smif.spi_data7 | scb[6].uart_cts:0 | | scb[6].spi_select0:0 | | | | | | | | | |
| P12.4 | tcpwm[0].line[6]:3 | tcpwm[1].line[6]:1 | | | smif.spi_select3 | | | scb[6].spi_select1:0 | audioss.pdm_clk | | | | | | | | |
| P12.5 | tcpwm[0].line_compl[6]:3 | tcpwm[1].line_compl[6]:1 | | | | | | scb[6].spi_select2:0 | audioss.pdm_data | | | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P12.6 | tcpwm[0].line[7]:3 | tcpwm[1].line[7]:1 | | | | | | scb[6].spi_select3:0 | | | | | | | | | |
| P12.7 | tcpwm[0].line_compl[7]:3 | tcpwm[1].line_compl[7]:1 | | | | | | | | | | | | | | | |
| P13.0 | tcpwm[0].line[0]:4 | tcpwm[1].line[8]:1 | | | | scb[6].uart_rx:1 | scb[6].i2c_scl:1 | scb[6].spi_mosi:1 | | | peri.tr_io_input[26]:0 | | | | | | |
| P13.1 | tcpwm[0].line_compl[0]:4 | tcpwm[1].line_compl[8]:1 | | | | scb[6].uart_tx:1 | scb[6].i2c_sda:1 | scb[6].spi_miso:1 | | | peri.tr_io_input[27]:0 | | | | | | |
| P13.2 | tcpwm[0].line[1]:4 | tcpwm[1].line[9]:1 | | | | scb[6].uart_rts:1 | | scb[6].spi_clk:1 | | | | | | | | | |
| P13.3 | tcpwm[0].line_compl[1]:4 | tcpwm[1].line_compl[9]:1 | | | | scb[6].uart_cts:1 | | scb[6].spi_select0:1 | | | | | | | | | |

**(table continues...)**

**Table 9 (continued) Multiple alternate functions[1)]**

| Port/pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P13.4 | tcpwm[0].line[2]:4 | tcpwm[1].line[10]:1 | | | | | | scb[6].spi_select1:1 | | | | | | | | | |
| P13.5 | tcpwm[0].line_compl[2]:4 | tcpwm[1].line_compl[10]:1 | | | | | | scb[6].spi_select2:1 | | | | | | | | | |
| P13.6 | tcpwm[0].line[3]:4 | tcpwm[1].line[11]:1 | | | | | | scb[6].spi_select3:1 | | | | | | | | | |
| P13.7 | tcpwm[0].line_compl[3]:4 | tcpwm[1].line_compl[11]:1 | | | | | | | | | | | | | | | |

*1)* The notation for a signal is of the form IPName[x].signal_name[u]:y. IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name. For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximize utilization of on-chip resources.

Analog, Smart I/O, and DSI alternate port pin functionality is provided in Table 10.

**Table 10 Port pin analog, Smart I/O, and DSI functions**

| Port/pin | Name | Analog | Digital HV | DSI | SMARTIO | USB |
|---|---|---|---|---|---|---|
| P0.0 | P0.0 | wco_in | | dsi[0].port_if[0] | | |
| P0.1 | P0.1 | wco_out | | dsi[0].port_if[1] | | |
| P0.2 | P0.2 | | | dsi[0].port_if[2] | | |
| P0.3 | P0.3 | | | dsi[0].port_if[3] | | |
| P0.4 | P0.4 | | pmic_wakeup_in hibernate_wakeup[1] | dsi[0].port_if[4] | | |
| P0.5 | P0.5 | | pmic_wakeup_out | dsi[0].port_if[5] | | |
| P1.0 | P1.0 | | | dsi[1].port_if[0] | | |
| P1.1 | P1.1 | | | dsi[1].port_if[1] | | |
| P1.2 | P1.2 | | | dsi[1].port_if[2] | | |
| P1.3 | P1.3 | | | dsi[1].port_if[3] | | |
| P1.4 | P1.4 | | hibernate_wakeup[0] | dsi[1].port_if[4] | | |
| P1.5 | P1.5 | | | dsi[1].port_if[5] | | |
| P14.0 | USBDP | | | | | usb.usb_dp_pad |
| P14.1 | USBDM | | | | | usb.usb_dm_pad |
| P2.0 | P2.0 | | | dsi[2].port_if[0] | | |
| P2.1 | P2.1 | | | dsi[2].port_if[1] | | |
| P2.2 | P2.2 | | | dsi[2].port_if[2] | | |
| P2.3 | P2.3 | | | dsi[2].port_if[3] | | |
| P2.4 | P2.4 | | | dsi[2].port_if[4] | | |
| P2.5 | P2.5 | | | dsi[2].port_if[5] | | |
| P2.6 | P2.6 | | | dsi[2].port_if[6] | | |
| P2.7 | P2.7 | | | dsi[2].port_if[7] | | |
| P3.0 | P3.0 | | | | | |
| P3.1 | P3.1 | | | | | |
| P3.2 | P3.2 | | | | | |
| P3.3 | P3.3 | | | | | |
| P3.4 | P3.4 | | | | | |
| P3.5 | P3.5 | | | | | |

**(table continues...)**

**Table 10 (continued) Port pin analog, Smart I/O, and DSI functions**

| Port/pin | Name | Analog | Digital HV | DSI | SMARTIO | USB |
|---|---|---|---|---|---|---|
| P4.0 | P4.0 | | | dsi[0].port_if[6] | | |
| P4.1 | P4.1 | | | dsi[0].port_if[7] | | |
| P5.0 | P5.0 | | | dsi[3].port_if[0] | | |
| P5.1 | P5.1 | | | dsi[3].port_if[1] | | |
| P5.2 | P5.2 | | | dsi[3].port_if[2] | | |
| P5.3 | P5.3 | | | dsi[3].port_if[3] | | |
| P5.4 | P5.4 | | | dsi[3].port_if[4] | | |
| P5.5 | P5.5 | | | dsi[3].port_if[5] | | |
| P5.6 | P5.6 | lpcomp.inp_comp0 | | dsi[3].port_if[6] | | |
| P5.7 | P5.7 | lpcomp.inn_comp0 | | dsi[3].port_if[7] | | |
| P6.0 | P6.0 | | | dsi[4].port_if[0] | | |
| P6.1 | P6.1 | | | dsi[4].port_if[1] | | |
| P6.2 | P6.2 | lpcomp.inp_comp1 | | dsi[4].port_if[2] | | |
| P6.3 | P6.3 | lpcomp.inn_comp1 | | dsi[4].port_if[3] | | |
| P6.4 | P6.4 | | | dsi[4].port_if[4] | | |
| P6.5 | P6.5 | | | dsi[4].port_if[5] | | |
| P6.6 | P6.6 | | swd_data | dsi[4].port_if[6] | | |
| P6.7 | P6.7 | | swd_clk | dsi[4].port_if[7] | | |
| P7.0 | P7.0 | | | dsi[5].port_if[0] | | |
| P7.1 | P7.1 | csd.cmodpaddcsd.cmodpads | | dsi[5].port_if[1] | | |
| P7.2 | P7.2 | csd.csh_tankpaddcsd.csh_tankpads | | dsi[5].port_if[2] | | |
| P7.3 | P7.3 | csd.vref_ext | | dsi[5].port_if[3] | | |
| P7.4 | P7.4 | | | dsi[5].port_if[4] | | |
| P7.5 | P7.5 | | | dsi[5].port_if[5] | | |
| P7.6 | P7.6 | | | dsi[5].port_if[6] | | |
| P7.7 | P7.7 | csd.cshieldpads | | dsi[5].port_if[7] | | |
| P8.0 | P8.0 | | | dsi[11].port_if[0] | smartio[8].io[0] | |
| P8.1 | P8.1 | | | dsi[11].port_if[1] | smartio[8].io[1] | |

**(table continues...)**

**Table 10 (continued) Port pin analog, Smart I/O, and DSI functions**

| Port/pin | Name | Analog | Digital HV | DSI | SMARTIO | USB |
|---|---|---|---|---|---|---|
| P8.2 | P8.2 | | | dsi[11].port_if[2] | smartio[8].io[2] | |
| P8.3 | P8.3 | | | dsi[11].port_if[3] | smartio[8].io[3] | |
| P8.4 | P8.4 | | | dsi[11].port_if[4] | smartio[8].io[4] | |
| P8.5 | P8.5 | | | dsi[11].port_if[5] | smartio[8].io[5] | |
| P8.6 | P8.6 | | | dsi[11].port_if[6] | smartio[8].io[6] | |
| P8.7 | P8.7 | | | dsi[11].port_if[7] | smartio[8].io[7] | |
| P9.0 | P9.0 | ctb_oa0+ | | dsi[10].port_if[0] | smartio[9].io[0] | |
| P9.1 | P9.1 | ctb_oa0- | | dsi[10].port_if[1] | smartio[9].io[1] | |
| P9.2 | P9.2 | ctb_oa0_out | | dsi[10].port_if[2] | smartio[9].io[2] | |
| P9.3 | P9.3 | ctb_oa1_out | | dsi[10].port_if[3] | smartio[9].io[3] | |
| P9.4 | P9.4 | ctb_oa1- | | dsi[10].port_if[4] | smartio[9].io[4] | |
| P9.5 | P9.5 | ctb_oa1+ | | dsi[10].port_if[5] | smartio[9].io[5] | |
| P9.6 | P9.6 | ctb_oa0+ | | dsi[10].port_if[6] | smartio[9].io[6] | |
| P9.7 | P9.7 | ctb_oa1+ or ext_vref | | dsi[10].port_if[7] | smartio[9].io[7] | |
| P10.0 | P10.0 | sarmux[0] | | dsi[9].port_if[0] | | |
| P10.1 | P10.1 | sarmux[1] | | dsi[9].port_if[1] | | |
| P10.2 | P10.2 | sarmux[2] | | dsi[9].port_if[2] | | |
| P10.3 | P10.3 | sarmux[3] | | dsi[9].port_if[3] | | |
| P10.4 | P10.4 | sarmux[4] | | dsi[9].port_if[4] | | |
| P10.5 | P10.5 | sarmux[5] | | dsi[9].port_if[5] | | |
| P10.6 | P10.6 | sarmux[6] | | dsi[9].port_if[6] | | |
| P10.7 | P10.7 | sarmux[7] | | dsi[9].port_if[7] | | |
| P11.0 | P11.0 | | | dsi[8].port_if[0] | | |
| P11.1 | P11.1 | | | dsi[8].port_if[1] | | |

**(table continues...)**

**Table 10 (continued) Port pin analog, Smart I/O, and DSI functions**

| Port/pin | Name | Analog | Digital HV | DSI | SMARTIO | USB |
|---|---|---|---|---|---|---|
| P11.2 | P11.2 | | | dsi[8].port_if[2] | | |
| P11.3 | P11.3 | | | dsi[8].port_if[3] | | |
| P11.4 | P11.4 | | | dsi[8].port_if[4] | | |
| P11.5 | P11.5 | | | dsi[8].port_if[5] | | |
| P11.6 | P11.6 | | | dsi[8].port_if[6] | | |
| P11.7 | P11.7 | | | dsi[8].port_if[7] | | |
| P12.0 | P12.0 | | | dsi[7].port_if[0] | | |
| P12.1 | P12.1 | | | dsi[7].port_if[1] | | |
| P12.2 | P12.2 | | | dsi[7].port_if[2] | | |
| P12.3 | P12.3 | | | dsi[7].port_if[3] | | |
| P12.4 | P12.4 | | | dsi[7].port_if[4] | | |
| P12.5 | P12.5 | | | dsi[7].port_if[5] | | |
| P12.6 | P12.6 | eco_in | | dsi[7].port_if[6] | | |
| P12.7 | P12.7 | eco_out | | dsi[7].port_if[7] | | |
| P13.0 | P13.0 | | | dsi[6].port_if[0] | | |
| P13.1 | P13.1 | | | dsi[6].port_if[1] | | |
| P13.2 | P13.2 | | | dsi[6].port_if[2] | | |
| P13.3 | P13.3 | | | dsi[6].port_if[3] | | |
| P13.4 | P13.4 | | | dsi[6].port_if[4] | | |
| P13.5 | P13.5 | | | dsi[6].port_if[5] | | |
| P13.6 | P13.6 | | | dsi[6].port_if[6] | | |
| P13.7 | P13.7 | | | dsi[6].port_if[7] | | |

# 5 Power supply considerations

The following power system diagrams show typical connections for power pins for all supported packages, and with and without usage of the buck regulator.

In these diagrams, the package pin is shown with the pin name, for example "$V_{DDA}$, A12". For $V_{DDx}$ pins, the I/O port that is powered by that pin is also shown, for example "$V_{DDD}$, A1; I/O port P1".

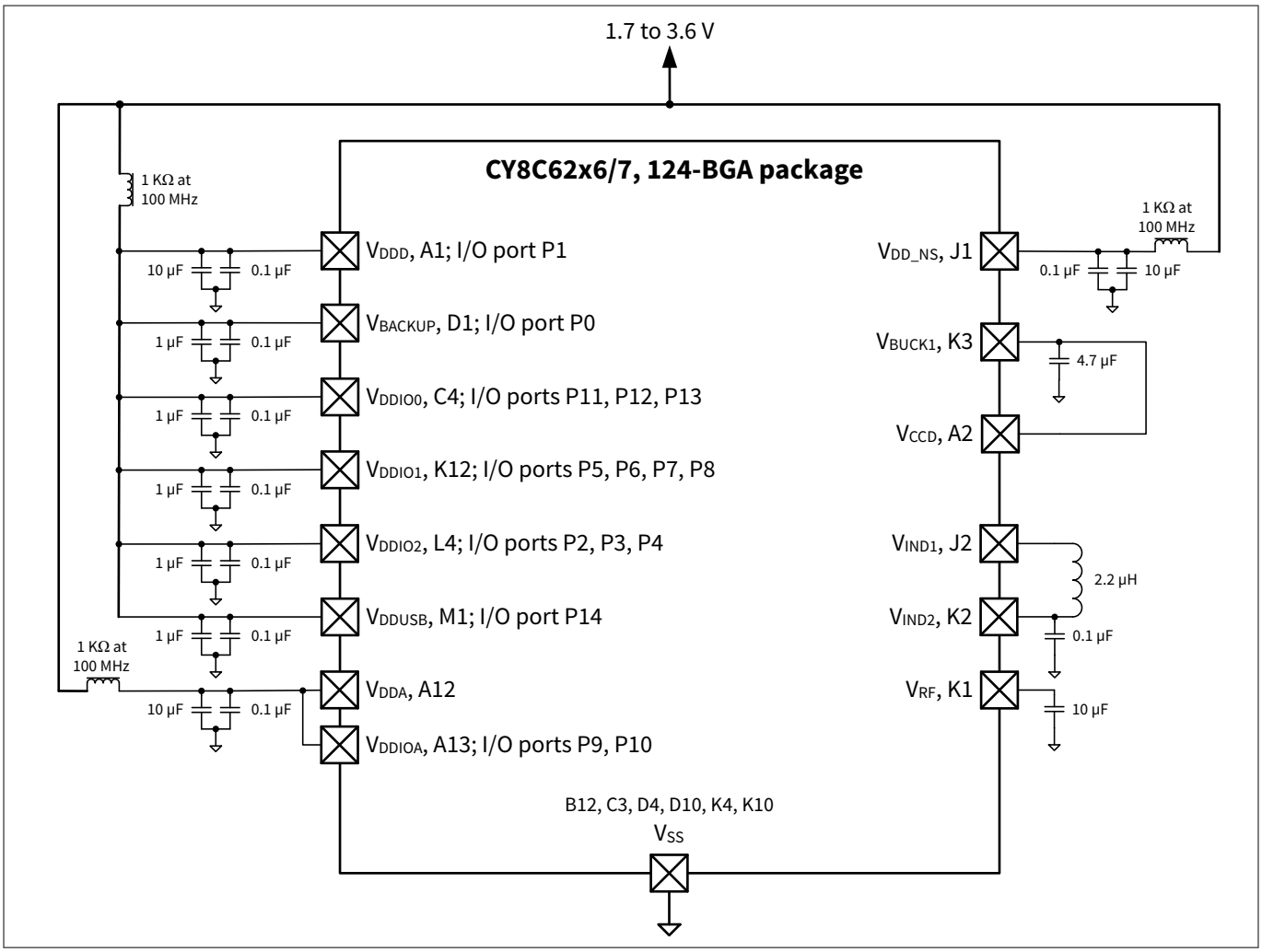



**Figure 11 124-BGA power connection diagram**

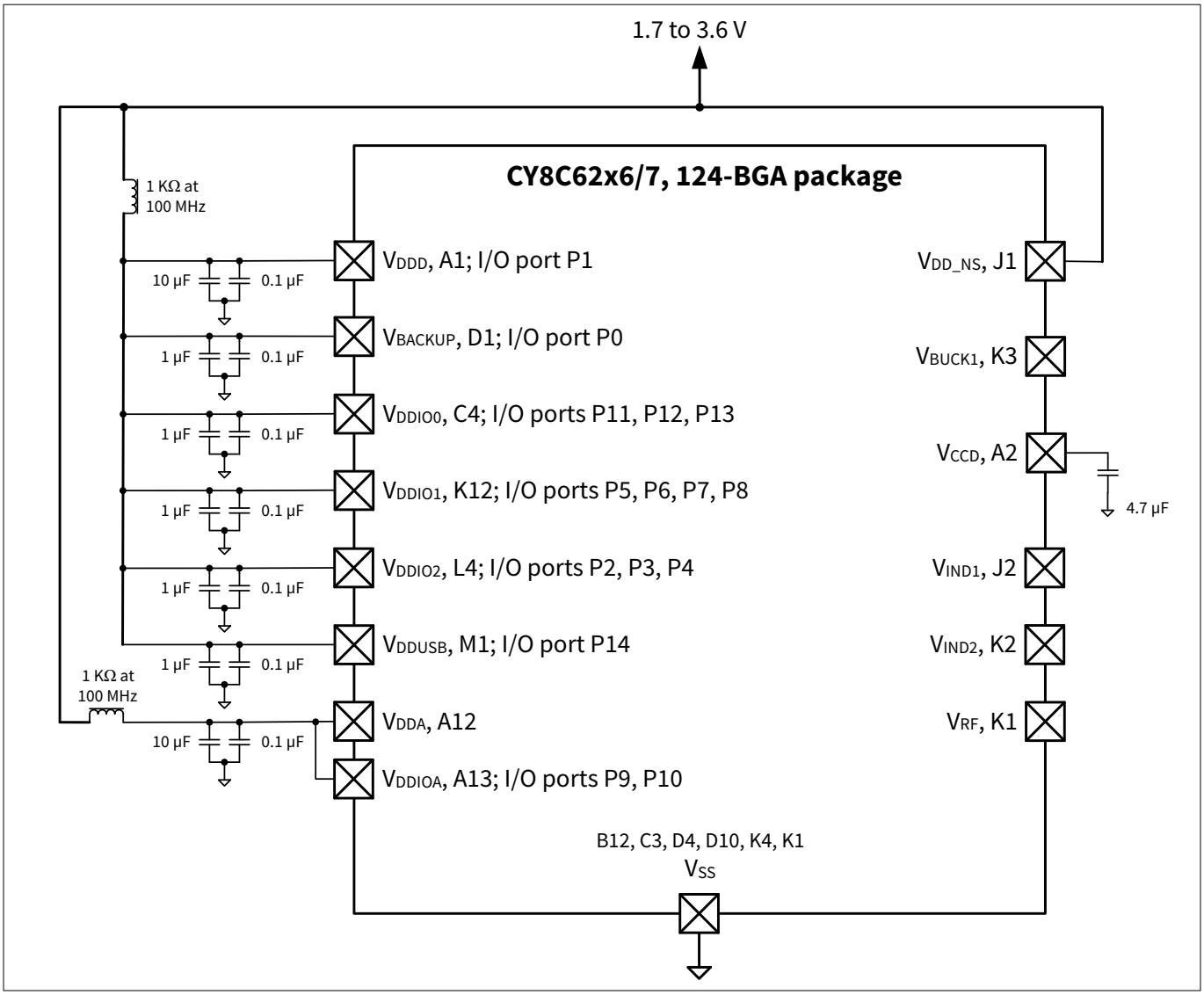



**Figure 12 124-BGA (No buck) power connection diagram**

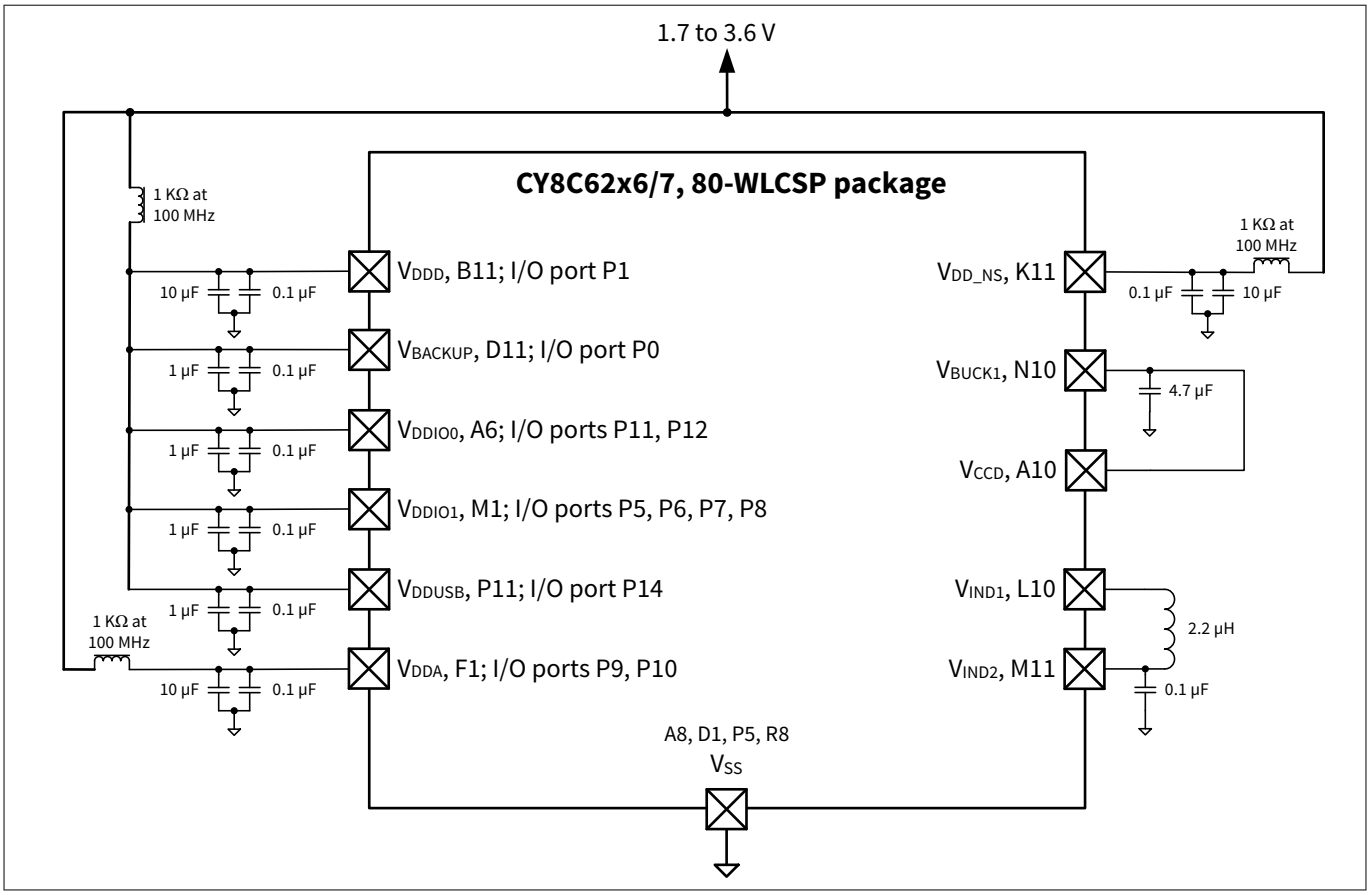



**Figure 13 80-WLCSP power connection diagram**

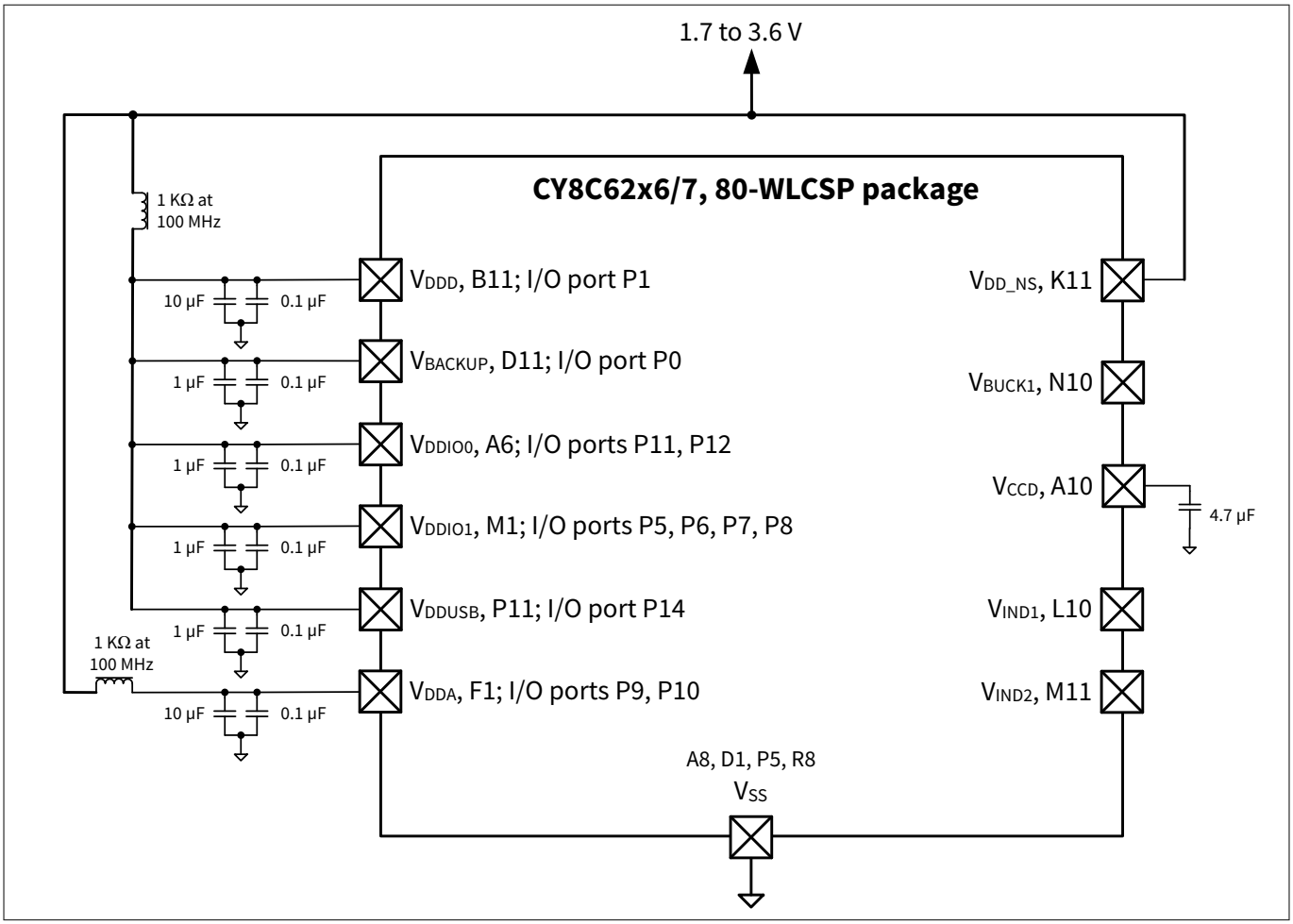



**Figure 14 80-WLCSP (no buck) power connection diagram**

There are as many as eight $V_{DDx}$ supply pins, depending on the package, and multiple $V_{SS}$ ground pins. The power pins are:

- $V_{DDD}$: the main digital supply. It powers the low dropout (LDO) regulators and I/O port 1
- $V_{CCD}$: the main LDO output. It requires a 4.7-µF capacitor for regulation. The LDO can be turned off when $V_{CCD}$ is driven from the switching regulator (see $V_{BUCK1}$ below). For more information, see the power system block diagram in the device reference manual.
- $V_{DDA}$: the supply for the analog peripherals. Voltage must be applied to this pin for correct device initialization and boot up
- $V_{DDIOA}$: the supply for I/O ports 9 and 10. If it is present in the device package, it must be connected to $V_{DDA}$
- $V_{DDIO0}$: the supply for I/O ports 11, 12, and 13
- $V_{DDIO1}$: the supply for I/O ports 5, 6, 7, and 8
- $V_{DDIO2}$: the supply for I/O ports 2, 3, and 4
- $V_{BACKUP}$: the supply for the backup domain, which includes the 32-kHz WCO and the RTC. It can be a separate supply as low as 1.4 V, for battery or supercapacitor backup, as Figure 15 shows. Otherwise it is connected to $V_{DDD}$. It powers I/O port 0

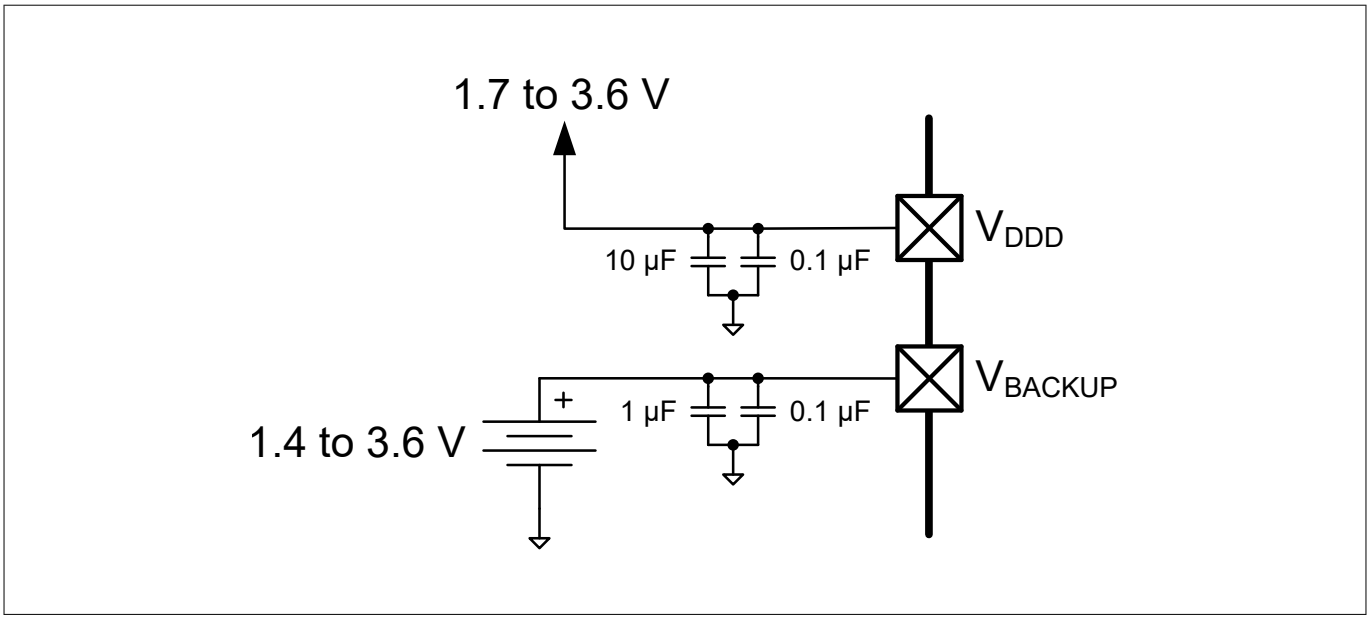



**Figure 15 Separate battery connection to $V_{BACKUP}$**

- $V_{DDUSB}$: the supply for the USB peripheral and the USBDP and USBDM pins. It must be 2.85 V to 3.6 V for USB operation. If USB is not used, it can be 1.7 V to 3.6 V, and the USB pins can be used as limited-capability GPIOs on I/O port 14

Table 11 shows a summary of the I/O port supplies:

**Table 11 I/O port supplies**

| Port | Supply | Alternate supply |
|---|---|---|
| 0 | $V_{BACKUP}$ | $V_{DDD}$ |
| 1 | $V_{DDD}$ | - |
| 2, 3, 4 | $V_{DDIO2}$ | - |
| 5, 6, 7, 8 | $V_{DDIO1}$ | - |
| 9, 10 | $V_{DDIOA}$ | $V_{DDA}$ |
| 11, 12, 13 | $V_{DDIO0}$ | - |
| 14 | $V_{DDUSB}$ | - |

***Note**: If the USB pins are not used, connect $V_{DDUSB}$ to ground and leave the P14.0/USBDP and P14.1/USBDM pins unconnected.*

Voltage must be applied to the $V_{DDD}$ pin, and the $V_{DDA}$ pin as noted above, for correct device initialization and operation. If an I/O port is not being used, applying voltage to the corresponding $V_{DDx}$ pin is optional.

- $V_{SS}$: ground pins for the above supplies. All ground pins should be connected together to a common ground

In addition to the LDO regulator, a single input multiple output (SIMO) switching regulator is included. It provides two regulated outputs using a single inductor. The regulator pins are:

- $V_{DD_NS}$: the regulator supply
- $V_{IND1}$ and $V_{IND2}$: the inductor and capacitor connections
- $V_{BUCK1}$: the first regulator output. It is typically used to drive $V_{CCD}$, see above
- $V_{RF}$: the second regulator output. It is typically not used; the pin may not be available in some packages

## 5 Power supply considerations

The various $V_{DD}$ power pins are not connected together on chip. They can be connected off chip, in one or more separate nets. If separate power nets are used, they can be isolated from noise from the other nets using optional ferrite beads, as indicated in the diagrams.

No external load should be placed on $V_{CCD}$, $V_{RF}$, or any of the switching regulator power pins; whether or not the switching regulator is used.

There are no power pin sequencing requirements; power supplies may be brought up in any order. The power management system holds the device in reset until all power pins are at the voltage levels required for proper operation.

***Note**: If a battery is installed on the PCB first, $V_{DDD}$ must be cycled for at least 50 µs. This prevents premature drain of the battery during product manufacture and storage.*

Bypass capacitors must be connected to a common ground from the $V_{DDx}$ and other pins, as indicated in the diagrams. Typical practice for systems in this frequency range is to use a 10-µF or 1-µF capacitor in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated for optimal bypassing.

All capacitors and inductors should be ±20% or better. The capacitor connected to $V_{IND2}$ should be 100 nF. The recommended inductor value is 2.2 µH ±20% (for example, TDK MLP2012H2R2MT0S1).

It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the applied voltage is a significant percentage of the rated working voltage.

For more information on pad layout, refer to PSOC™ 6 CAD libraries.

# 6 Electrical specifications

All specifications are valid for –40°C ≤ $T_A$ ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

## 6.1 Absolute maximum ratings

**Table 12 Absolute maximum ratings[1)]**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID1 | $V_{DD_ABS}$ | Analog or digital supply relative to $V_{SS}$ ($V_{SSD}$ = $V_{SSA}$) | –0.5 | – | 4 | V | |
| SID2 | $V_{CCD_ABS}$ | Direct digital core voltage input relative to $V_{SSD}$ | –0.5 | – | 1.2 | V | |
| SID3 | $V_{GPIO_ABS}$ | GPIO voltage; $V_{DDD}$ or $V_{DDA}$ | –0.5 | – | $V_{DD}$ + 0.5 | V | |
| SID4 | $I_{GPIO_ABS}$ | Current per GPIO | –25 | – | 25 | mA | |
| SID5 | $I_{GPIO_injection}$ | GPIO injection current per pin | –0.5 | – | 0.5 | mA | |
| SID3A | ESD_HBM | Electrostatic discharge Human Body Model | 2200 | – | – | V | |
| SID4A | ESD_CDM | Electrostatic discharge Charged Device Model | 500 | – | – | V | |
| SID5A | LU | Pin current for latchup-free operation | –100 | – | 100 | mA | |

*1)* Usage above the absolute maximum conditions listed in Table 12 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

## 6.2 Device-level specifications

Table 15 provides detailed specifications of CPU current. Table 13 summarizes these specifications, for rapid review of CPU currents under common conditions. Note that the max frequency for CM4 is 150 MHz, and for CM0+ is 100 MHz. IMO and FLL are used to generate the CPU clocks; FLL is not used when the CPU clock frequency is 8 MHz.

**Table 13 CPU current specifications summary**

| Condition | Range | Typ range | Max range |
|---|---|---|---|
| LP Mode, $V_{DDD}$ = 3.3 V, $V_{CCD}$ = 1.1 V, with buck regulator | | | |
| CM4 active, CM0+ sleep | Across CPUs clock ranges: 8–150/100 MHz; Dhrystone with flash cache enabled | 0.9–6.9 mA | 1.5–8.6 mA |
| CM0+ active, CM4 sleep | | 0.8–3.8 mA | 1.3–4.5 mA |
| CM4 sleep, CM0+ sleep | | 0.7–1.5 mA | 1.3–2.2 mA |
| CM0+ sleep, CM4 off | | 0.7–1.3 mA | 1.3–2 mA |
| Minimum regulator current mode | Across CM4/CM0+ CPU active/sleep modes | 0.6–0.7 mA | 1.1–1.1 mA |
| ULP Mode, $V_{DDD}$ = 3.3 V, $V_{CCD}$ = 0.9 V, with buck regulator | | | |

**(table continues...)**

**Table 13 (continued) CPU current specifications summary**

| Condition | Range | Typ range | Max range |
|---|---|---|---|
| CM4 active, CM0+ sleep | Across CPUs clock ranges: 8 – 50/25 MHz; Dhrystone with flash cache enabled | 0.65–1.6 mA | 0.8–2.2 mA |
| CM0+ active, CM4 sleep | | 0.51–0.91 mA | 0.72–1.25 mA |
| CM4 sleep, CM0+ sleep | | 0.42–0.76 mA | 0.65–1.1 mA |
| CM0+ sleep, CM4 off | | 0.41–0.62 mA | 0.6–0.9 mA |
| Minimum regulator current mode | Across CM4/CM0+ CPU active/sleep modes | 0.39–0.54 mA | 0.6–0.76 mA |
| Deep Sleep | Across SRAM retention | 7–9 µA | - |
| Hibernate | Across $V_{DDD}$ | 300–800 nA | - |

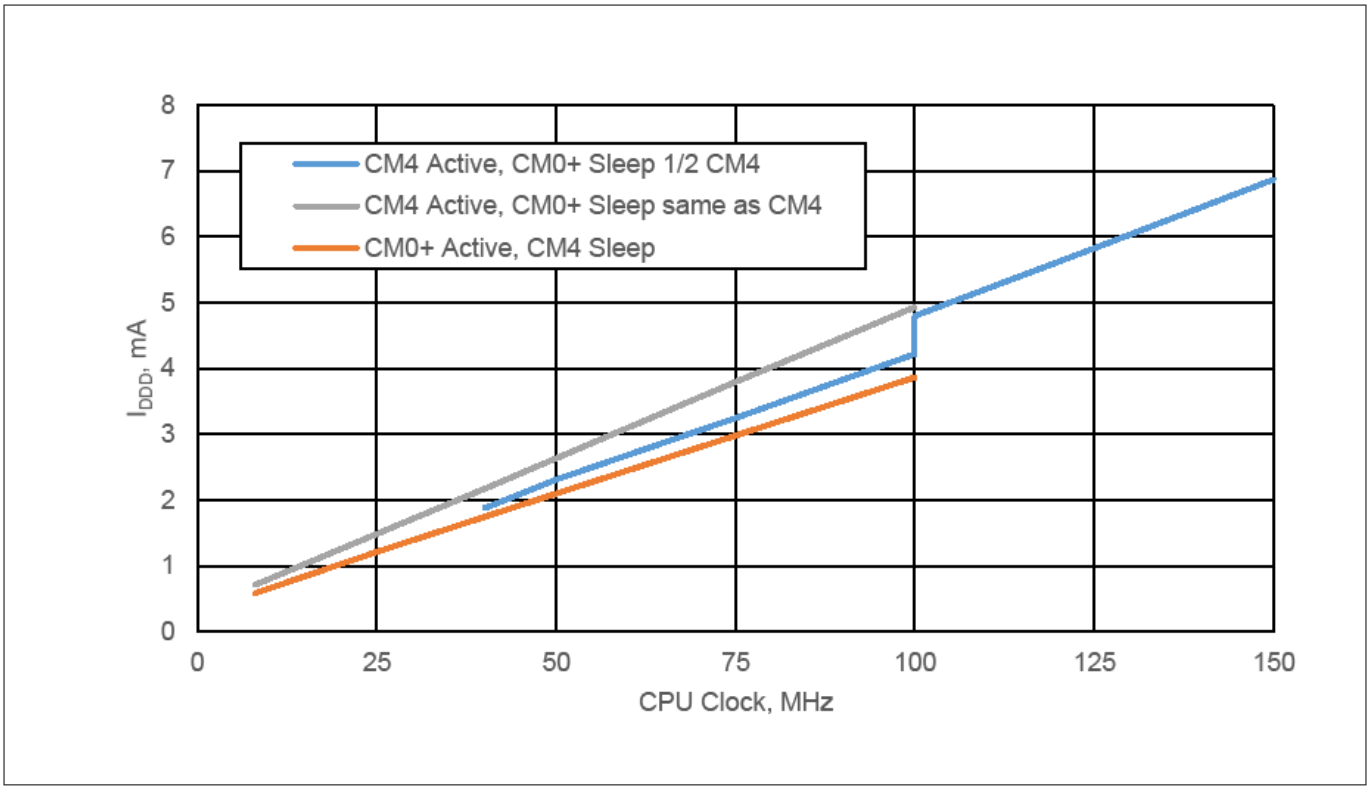



**Figure 16 Typical device currents vs. CPU frequency; System Low Power (LP) mode[3)]**

## 6.2.1 Power supplies

**Table 14 Power supply DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID6 | $V_{DDD}$ | Internal regulator and Port 1 GPIO supply | 1.7 | – | 3.6 | V | – |
| SID7 | $V_{DDA}$ | Analog power supply voltage. Shorted to $V_{DDIOA}$ on PCB. | 1.7 | – | 3.6 | V | Internally unregulated supply |

**(table continues...)**

3 CM4 Active, CM0+ Sleep 1/2 CM4 trace values are higher because above 100 MHz, the PLL must be used instead of the FLL.

**Table 14 (continued) Power supply DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID7A | $V_{DDIO1}$ | GPIO supply for ports 5 to 8 when present | 1.7 | – | 3.6 | V | Must be ≥ $V_{DDA}$ if the CAPSENSE™ (CSD) block is used in the application |
| SID7B | $V_{DDIO0}$ | GPIO supply for ports 11 to 13 when present | 1.7 | – | 3.6 | V | – |
| SID7E | $V_{DDIO0}$ | Supply for eFuse programming | 2.38 | 2.5 | 2.62 | V | |
| SID7C | $V_{DDIO2}$ | GPIO supply for ports 2 to 4 when present | 1.7 | – | 3.6 | V | – |
| SID7D | $V_{DDIOA}$ | GPIO supply for ports 9 and 10 when present. Must be connected to $V_{DDA}$ on PCB. | 1.7 | – | 3.6 | V | – |
| SID7F | $V_{DDUSB}$ | Supply for port 14 (USB or GPIO) when present | 1.7 | – | 3.6 | V | Min. supply is 2.85 V for USB |
| SID6B | $V_{BACKUP}$ | Backup power and GPIO Port 0 supply when present | 1.7 | – | 3.6 | V | Min. is 1.4 V when $V_{DDD}$ is removed. |
| SID8 | $V_{CCD1}$ | Output voltage (for core logic bypass) | – | 1.1 | – | V | System LP mode |
| SID9 | $V_{CCD2}$ | Output voltage (for core logic bypass) | – | 0.9 | – | V | ULP mode. Valid for –20 to 85°C. |
| SID10 | $C_{EFC}$ | External regulator voltage ($V_{CCD}$) bypass | 3.8 | 4.7 | 5.6 | µF | X5R ceramic or better; Value for 0.8 to 1.2 V. |
| SID11 | $C_{EXC}$ | Power supply decoupling capacitor | – | 10 | – | µF | X5R ceramic or better |

## 6.2.2 CPU current and transition times

**Table 15 CPU current and transition times**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **LP RANGE POWER SPECIFICATIONS (for $V_{CCD}$ = 1.1 V with Buck and LDO)** | | | | | | | |
| **Cortex® M4. Active mode** | | | | | | | |
| **Execute with cache disabled (Flash)** | | | | | | | |
| SIDF1 | $I_{DD1}$ | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1). | – | 2.3 | 3.2 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 3.1 | 3.6 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 5.7 | 6.5 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85 °C |

**(table continues...)**

**Table 15 (continued) CPU current and transition times**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SIDF2 | $I_{DD2}$ | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1). | – | 0.9 | 1.5 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.2 | 1.6 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.8 | 3.5 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85 °C |
| **Execute with cache enabled** | | | | | | | |
| SIDC1 | $I_{DD3}$ | Execute from Cache; CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO & PLL. Dhrystone. | – | 6.9 | 8.6 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 10.9 | 13.7 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 13.7 | 15.5 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDC2 | $I_{DD4}$ | Execute from Cache; CM4 Active 100 MHz, CM0+ Sleep 100 MHz. IMO & FLL. Dhrystone. | – | 4.8 | 5.8 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 7.4 | 8.4 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 11.3 | 12 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| SIDC3 | $I_{DD5}$ | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. IMO & FLL. Dhrystone | – | 2.4 | 3.4 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 3.7 | 4.1 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 6.3 | 7.2 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDC4 | $I_{DD6}$ | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone. | – | 0.9 | 1.5 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 1.3 | 1.8 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 3 | 3.8 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85 °C |
| **Cortex® M0+. Active mode** | | | | | | | |
| **Execute with cache disabled (Flash)** | | | | | | | |
| SIDF3 | $I_{DD7}$ | Execute from Flash; CM4 Off, CM0+ Active 50 MHz. With IMO & FLL. While (1). | – | 2.4 | 3.3 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 3.2 | 3.7 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 5.6 | 6.3 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |

**(table continues...)**

**Table 15 (continued) CPU current and transition times**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SIDF4 | $I_{DD8}$ | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While (1). | – | 0.8 | 1.5 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.1 | 1.6 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.60 | 3.4 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| **Execute with cache enabled** | | | | | | | |
| SIDC5 | $I_{DD9}$ | Execute from Cache; CM4 Off, CM0+ Active 100 MHz. With IMO & FLL. Dhrystone. | – | 3.8 | 4.5 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 5.9 | 6.5 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 9 | 9.7 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| SIDC6 | $I_{DD10}$ | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | – | 0.8 | 1.3 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.20 | 1.7 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.60 | 3.4 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| **Cortex® M4. Sleep mode** | | | | | | | |
| SIDS1 | $I_{DD11}$ | CM4 Sleep 100 MHz; CM0+ Sleep 25 MHz. With IMO & FLL. | – | 1.5 | 2.2 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 2.2 | 2.7 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 4 | 4.6 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| SIDS2 | $I_{DD12}$ | CM4 Sleep 50 MHz; CM0+ Sleep 25 MHz. With IMO & FLL. | – | 1.2 | 1.9 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.7 | 2.2 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 3.4 | 4.3 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| SIDS3 | $I_{DD13}$ | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | – | 0.7 | 1.3 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1 | 1.5 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.4 | 3.3 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| **Cortex® M0+. Sleep mode** | | | | | | | |

**(table continues...)**

**Table 15 (continued) CPU current and transition times**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SIDS4 | $I_{DD14}$ | CM4 Off, CM0+ Sleep 50 MHz. With IMO & FLL. | – | 1.3 | 2 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.9 | 2.4 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 3.80 | 4.6 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| SIDS5 | $I_{DD15}$ | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | – | 0.7 | 1.3 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1 | 1.5 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.4 | 3.3 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| **Cortex® M4. Minimum Regulator Current mode** | | | | | | | |
| SIDLPA1 | $I_{DD16}$ | Execute from Flash; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1). | – | 0.9 | 1.5 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.2 | 1.7 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.8 | 3.5 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| SIDLPA2 | $I_{DD17}$ | Execute from Cache; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | – | 0.9 | 1.5 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.3 | 1.8 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.9 | 3.7 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| **Cortex® M0+. Minimum Regulator Current mode** | | | | | | | |
| SIDLPA3 | $I_{DD18}$ | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While (1). | – | 0.8 | 1.4 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.1 | 1.6 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.7 | 3.6 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| SIDLPA4 | $I_{DD19}$ | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | – | 0.8 | 1.4 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.2 | 1.7 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.7 | 3.6 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| **Cortex® M4. Minimum Regulator Current mode** | | | | | | | |

**(table continues...)**

**Table 15 (continued) CPU current and transition times**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SIDLPS1 | $I_{DD20}$ | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | – | 0.7 | 1.1 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1 | 1.5 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.4 | 3.3 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| **Cortex® M0+. Minimum Regulator Current mode** | | | | | | | |
| SIDLPS3 | $I_{DD22}$ | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | – | 0.6 | 1.1 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.9 | 1.5 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| | | | – | 2.4 | 3.3 | mA | $V_{DDD}$ = 1.8 to 3.3 V, LDO, Max at 85°C |
| **ULP RANGE POWER SPECIFICATIONS (for $V_{CCD}$ = 0.9 V using the buck). ULP mode is valid from –20 to +85°C.** | | | | | | | |
| **Cortex® M4. Active mode** | | | | | | | |
| **Execute with cache disabled (Flash)** | | | | | | | |
| SIDF5 | $I_{DD3}$ | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1). | – | 1.7 | 2.2 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 2.1 | 2.4 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| SIDF6 | $I_{DD4}$ | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1) | – | 0.56 | 0.8 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.75 | 1 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Execute with cache enabled** | | | | | | | |
| SIDC8 | $I_{DD10}$ | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. Dhrystone. | – | 1.6 | 2.2 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 2.4 | 2.7 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| SIDC9 | $I_{DD11}$ | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | – | 0.65 | 0.8 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.8 | 1.1 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Cortex® M0+. Active mode** | | | | | | | |
| **Execute with cache disabled (Flash)** | | | | | | | |
| SIDF7 | $I_{DD16}$ | Execute from Flash; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Write(1). | – | 1 | 1.4 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |

**(table continues...)**

**Table 15 (continued) CPU current and transition times**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| | | | – | 1.34 | 1.6 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| SIDF8 | $I_{DD17}$ | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While(1). | – | 0.54 | 0.75 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.73 | 1 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Execute with cache enabled** | | | | | | | |
| SIDC10 | $I_{DD18}$ | Execute from Cache; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Dhrystone. | – | 0.91 | 1.25 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.34 | 1.6 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| SIDC11 | $I_{DD19}$ | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | – | 0.51 | 0.72 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.73 | 0.95 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Cortex® M4. Sleep mode** | | | | | | | |
| SIDS7 | $I_{DD21}$ | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. | – | 0.76 | 1.1 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 1.1 | 1.4 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| SIDS8 | $I_{DD22}$ | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | – | 0.42 | 0.65 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.59 | 0.8 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Cortex® M0+. Sleep mode** | | | | | | | |
| SIDS9 | $I_{DD23}$ | CM4 Off, CM0+ Sleep 25 MHz. With IMO & FLL. | – | 0.62 | 0.9 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.88 | 1.1 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| SIDS10 | $I_{DD24}$ | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | – | 0.41 | 0.6 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.58 | 0.8 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Cortex® M4. Minimum Regulator Current mode** | | | | | | | |
| SIDLPA5 | $I_{DD25}$ | Execute from Flash. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1). | – | 0.52 | 0.75 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.76 | 1 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |

**(table continues...)**

**Table 15 (continued) CPU current and transition times**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SIDLPA6 | $I_{DD26}$ | Execute from Cache. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | – | 0.54 | 0.76 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.78 | 1 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Cortex® M0+. Minimum Regulator Current mode** | | | | | | | |
| SIDLPA7 | $I_{DD27}$ | Execute from Flash. CM4 Off, CM0+ Active 8 MHz. With IMO. While (1). | – | 0.51 | 0.75 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.75 | 1 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| SIDLPA8 | $I_{DD28}$ | Execute from Cache. CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | – | 0.48 | 0.7 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.7 | 0.95 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Cortex® M4. Minimum Regulator Current mode** | | | | | | | |
| SIDLPS5 | $I_{DD29}$ | CM4 Sleep 8 MHz, CM0 Sleep 8 MHz. With IMO. | – | 0.4 | 0.6 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.57 | 0.8 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Cortex® M0+. Minimum Regulator Current mode** | | | | | | | |
| SIDLPS7 | $I_{DD31}$ | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | – | 0.39 | 0.6 | mA | $V_{DDD}$ = 3.3 V, Buck ON, Max at 60°C |
| | | | – | 0.56 | 0.8 | mA | $V_{DDD}$ = 1.8 V, Buck ON, Max at 60°C |
| **Deep Sleep mode** | | | | | | | |
| SIDDS1 | $I_{DD33A}$ | With internal buck enabled and 64K SRAM retention | – | 7 | – | µA | Max value is at 85°C |
| SIDDS1_B | $I_{DD33A_B}$ | With internal buck enabled and 64K SRAM retention | – | 7 | – | µA | Max value is at 60°C |
| SIDDS2 | $I_{DD33B}$ | With internal buck enabled and 256K SRAM retention | – | 9 | – | µA | Max value is at 85°C |
| SIDDS2_B | $I_{DD33B_B}$ | With internal buck enabled and 256K SRAM retention | – | 9 | – | µA | Max value is at 60°C |
| **Hibernate mode** | | | | | | | |
| SIDHIB1 | $I_{DD34}$ | $V_{DDD}$ = 1.8 V | – | 300 | – | nA | No clocks running |
| SIDHIB2 | $I_{DD34A}$ | $V_{DDD}$ = 3.3 V | – | 800 | – | nA | No clocks running |
| **Power Mode transition times** | | | | | | | |
| SID12 | $T_{LPACT_ACT}$ | Minimum regulator current to LP transition time | – | – | 35 | µs | Including PLL lock time |

**(table continues...)**

**Table 15 (continued) CPU current and transition times**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID13 | $T_{DS_LPACT}$ | Deep Sleep to LP transition time | – | – | 25 | µs | Guaranteed by design |
| SID14 | $T_{HIB_ACT}$ | Hibernate to LP transition time | – | 500 | – | µs | Including PLL lock time |

## 6.2.3 XRES

**Table 16 XRES DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID17 | $T_{XRES_IDD}$ | IDD when XRES asserted | – | 300 | – | nA | $V_{DDD}$ = 1.8 V |
| SID17A | $T_{XRES_IDD_1}$ | IDD when XRES asserted | – | 800 | – | nA | $V_{DDD}$ = 3.3 V |
| SID77 | $V_{IH}$ | Input voltage high threshold | 0.7 × $V_{DD}$ | – | – | V | CMOS Input |
| SID78 | $V_{IL}$ | Input voltage low threshold | – | – | 0.3 × $V_{DD}$ | V | CMOS Input |
| SID80 | $C_{IN}$ | Input capacitance | – | 3 | – | pF | – |
| SID81 | $V_{HYSXRES}$ | Input voltage hysteresis | – | 100 | – | mV | – |
| SID82 | $I_{DIODE}$ | Current through protection diode to $V_{DD}/V_{SS}$ | – | – | 100 | µA | – |

**Table 17 XRES AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID15 | $T_{XRES_ACT}$ | Time from XRES release to Cortex®-M0+ executing application code | – | 750 | – | µs | Not minimum regulator current mode; Cortex®-M0+ executing at 50 MHz |
| SID16 | $T_{XRES_PW}$ | XRES Pulse width | 5 | – | – | µs | – |

## 6.2.4 GPIO

**Table 18 GPIO DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID57 | $V_{IH}$ | Input voltage high threshold | 0.7 × $V_{DD}$ | – | – | V | CMOS Input |
| SID57A | $I_{IHS}$ | Input current when Pad > $V_{DDIO}$ for OVT inputs | – | – | 10 | µA | Per $I^2C$ Spec |
| SID58 | $V_{IL}$ | Input voltage low threshold | – | – | 0.3 × $V_{DD}$ | V | CMOS Input |
| SID241 | $V_{IH}$ | LVTTL input, $V_{DD}$ < 2.7 V | 0.7 × $V_{DD}$ | – | – | V | – |

**(table continues...)**

**Table 18 (continued) GPIO DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID242 | $V_{IL}$ | LVTTL input, $V_{DD}$ < 2.7 V | – | – | 0.3 × $V_{DD}$ | V | – |
| SID243 | $V_{IH}$ | LVTTL input, $V_{DD}$ ≥ 2.7 V | 2.0 | – | – | V | – |
| SID244 | $V_{IL}$ | LVTTL input, $V_{DD}$ ≥ 2.7 V | – | – | 0.8 | V | – |
| SID59 | $V_{OH}$ | Output voltage high level | $V_{DD}$ – 0.5 | – | – | V | $I_{OH}$ = 8 mA |
| SID62A | $V_{OL}$ | Output voltage low level | – | – | 0.4 | V | $I_{OL}$ = 8 mA |
| SID63 | $R_{PULLUP}$ | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID65 | $I_{IL}$ | Input leakage current (absolute value) | – | – | 2 | nA | 25°C, $V_{DD}$ = 3.0 V |
| SID65A | $I_{IL_CTBM}$ | Input leakage on CTBm input pins | – | – | 4 | nA | – |
| SID66 | $C_{IN}$ | Input Capacitance | – | – | 5 | pF | – |
| SID67 | $V_{HYSTTL}$ | Input hysteresis LVTTL $V_{DD}$ > 2.7 V | 100 | 0 | – | mV | – |
| SID68 | $V_{HYSCMOS}$ | Input hysteresis CMOS | 0.05 × $V_{DD}$ | – | – | mV | – |
| SID69 | $I_{DIODE}$ | Current through protection diode to $V_{DD}$/$V_{SS}$ | – | – | 100 | µA | – |
| SID69A | $I_{TOT_GPIO}$ | Maximum total source or sink Chip Current | – | – | 200 | mA | – |

**Table 19 GPIO AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID70 | $T_{RISEF}$ | Rise time in Fast Strong Mode. 10% to 90% of $V_{DD}$ | – | – | 2.5 | ns | Cload = 15 pF, 8 mA drive strength |
| SID71 | $T_{FALLF}$ | Fall time in Fast Strong Mode. 10% to 90% of $V_{DD}$ | – | – | 2.5 | ns | Cload = 15 pF, 8 mA drive strength |
| SID72 | $T_{RISES_1}$ | Rise time in Slow Strong Mode. 10% to 90% of $V_{DD}$ | 52 | – | 142 | ns | Cload = 15 pF, 8 mA drive strength, $V_{DD}$ ≤ 2.7 V |
| SID72A | $T_{RISES_2}$ | Rise time in Slow Strong Mode. 10% to 90% of $V_{DD}$ | 48 | – | 102 | ns | Cload = 15 pF, 8 mA drive strength, 2.7 V < $V_{DD}$ ≤ 3.6 V |
| SID73 | $T_{FALLS_1}$ | Fall time in Slow Strong Mode. 10% to 90% of $V_{DD}$ | 44 | – | 211 | ns | Cload = 15 pF, 8 mA drive strength, $V_{DD}$ ≤ 2.7 V |

**(table continues...)**

**Table 19 (continued) GPIO AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID73A | $T_{FALLS_2}$ | Fall time in Slow Strong Mode. 10% to 90% of $V_{DD}$ | 42 | – | 93 | ns | Cload = 15 pF, 8 mA drive strength, 2.7 V < $V_{DD}$ ≤ 3.6 V |
| SID73G | $T_{FALL_I2C}$ | Fall time (30% to 70% of $V_{DD}$) in Slow Strong mode | 20 × $V_{DDIO}$/ 5.5 | – | 250 | ns | Cload = 10 pF to 400 pF, 8-mA drive strength |
| SID74 | $F_{GPIOUT1}$ | GPIO Fout. Fast Strong mode. | – | – | 100 | MHz | 90/10%, 15-pF load, 60/40 duty cycle |
| SID75 | $F_{GPIOUT2}$ | GPIO Fout; Slow Strong mode. | – | – | 16.7 | MHz | 90/10%, 15-pF load, 60/40 duty cycle |
| SID76 | $F_{GPIOUT3}$ | GPIO Fout; Fast Strong mode. | – | – | 7 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID245 | $F_{GPIOUT4}$ | GPIO Fout; Slow Strong mode. | – | – | 3.5 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID246 | $F_{GPIOIN}$ | GPIO input operating frequency;1.71 V ≤ $V_{DD}$ ≤ 3.6 V | – | – | 100 | MHz | 90/10% $V_{IO}$ |

## 6.3 Analog peripherals

### 6.3.1 Opamp

**Table 20 Opamp specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| | $I_{DD}$ | Opamp block current. No load. | – | – | – | | – |
| SID269 | $I_{DD_HI}$ | Power = Hi | – | 1300 | 1500 | µA | – |
| SID270 | $I_{DD_MED}$ | Power = Med | – | 450 | 600 | µA | – |
| SID271 | $I_{DD_LOW}$ | Power = Lo | – | 250 | 350 | µA | – |
| | GBW | Load = 50 pF, 0.1 mA. $V_{DDA}$ ≥ 2.7 V | – | – | – | | – |
| SID272 | $G_{BW_HI}$ | Power = Hi | 6 | – | – | MHz | – |
| SID273 | $G_{BW_MED}$ | Power = Med | 3 | – | – | MHz | – |
| SID274 | $G_{BW_LO}$ | Power = Lo | 1 | – | – | MHz | – |
| | $I_{OUT_MAX}$ | $V_{DDA}$ ≥ 2.7 V, 500 mV from rail | – | – | – | | – |
| SID275 | $I_{OUT_MAX_HI}$ | Power = Hi | 10 | – | – | mA | – |
| SID276 | $I_{OUT_MAX_MID}$ | Power = Med | 10 | – | – | mA | – |

**(table continues...)**

**Table 20 (continued) Opamp specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID277 | $I_{OUT_MAX_LO}$ | Power = Lo | – | 5 | – | mA | – |
| | $I_{OUT}$ | $V_{DDA}$ = 1.71 V, 500 mV from rail | – | – | – | | – |
| SID278 | $I_{OUT_MAX_HI}$ | Power = Hi | 4 | – | – | mA | – |
| SID279 | $I_{OUT_MAX_MID}$ | Power = Med | 4 | – | – | mA | – |
| SID280 | $I_{OUT_MAX_LO}$ | Power = Lo | – | 2 | – | mA | – |
| SID281 | $V_{IN}$ | Input voltage range | 0 | – | $V_{DDA}$ – 0.2 | V | Charge pump ON |
| SID282 | $V_{CM}$ | Input common mode voltage | 0 | – | $V_{DDA}$ – 1.5 | V | Charge pump OFF, $V_{DDA} \geq 2.7$ V |
| | $V_{OUT}$ | $V_{DDA} \geq 2.7$ V | – | – | – | | – |
| SID283 | $V_{OUT_1}$ | Power = Hi, Iload = 10 mA | 0.5 | – | $V_{DDA}$ – 0.5 | V | – |
| SID284 | $V_{OUT_2}$ | Power = Hi, Iload = 1 mA | 0.2 | – | $V_{DDA}$ – 0.2 | V | – |
| SID285 | $V_{OUT_3}$ | Power = Med, Iload = 1 mA | 0.2 | – | $V_{DDA}$ – 0.2 | V | – |
| SID286 | $V_{OUT_4}$ | Power = Lo, Iload = 0.1 mA | 0.2 | – | $V_{DDA}$ – 0.2 | V | – |
| SID288 | $V_{OS_TR}$ | Offset voltage | –1 | ±0.5 | 1 | mV | Power = Hi, 0.2 V < $V_{OUT}$ < ($V_{DDA}$ - 0.2 V) |
| SID288A | $V_{OS_TR}$ | Offset voltage | – | ±1 | – | mV | Power = Med |
| SID288B | $V_{OS_TR}$ | Offset voltage | – | ±2 | – | mV | Power = Lo |
| SID290 | $V_{OS_DR_TR}$ | Offset voltage drift | –10 | ±3 | 10 | µV/°C | Power = Hi, 0.2 V < $V_{OUT}$ < ($V_{DDA}$ - 0.2 V) |
| SID290A | $V_{OS_DR_TR}$ | Offset voltage drift | – | ±10 | – | µV/°C | Power = Med |
| SID290B | $V_{OS_DR_TR}$ | Offset voltage drift | – | ±10 | – | µV/°C | Power = Lo |
| SID291 | CMRR | DC common mode rejection ratio | 67 | 80 | – | dB | $V_{DDA} \geq 2.7$ V |
| SID292 | PSRR | Power supply rejection ratio at 1 kHz, 10-mV ripple | 70 | 85 | – | dB | $V_{DDA} \geq 2.7$ V |
| SID65A | $I_{IL_CTBM}$ | Input leakage on CTBm input pins | – | – | 4 | nA | – |
| **Noise** | | | | | | | |
| SID293 | VN1 | Input-referred, 1 Hz – 1 GHz, power = Hi | – | 100 | – | µVrms | – |

**(table continues...)**

**Table 20 (continued) Opamp specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID294 | VN2 | Input-referred, 1 kHz, power = Hi | – | 180 | – | nV/rtHz | – |
| SID295 | VN3 | Input-referred, 10 kHz, power = Hi | – | 70 | – | nV/rtHz | – |
| SID296 | VN4 | Input-referred, 100 kHz, power = Hi | – | 38 | – | nV/rtHz | – |
| SID297 | CLOAD | Stable up to max. load. Performance specs at 50 pF. | – | – | 125 | pF | – |
| SID298 | SLEW_RATE | Output slew rate | 4 | – | – | V/µs | Cload = 50 pF, Power = Hi, $V_{DDA} \geq$ 2.7 V<br>Refer to Figure 17 and Figure 18. |
| SID299 | T_OP_WAKE | From disable to enable, no external RC dominating | – | 25 | – | µs | – |
| | COMP_MODE | Comparator mode; 50-mV overdrive, Trise = Tfall (approx.) | – | | – | | – |
| SID300 | $T_{PD1}$ | Response time; power = Hi | – | 150 | – | ns | – |
| SID301 | $T_{PD2}$ | Response time; power = Med | – | 400 | – | ns | – |
| SID302 | $T_{PD3}$ | Response time; power = Lo | – | 2000 | – | ns | – |
| SID303 | $V_{HYST_OP}$ | Hysteresis | – | 10 | – | mV | – |
| **Deep Sleep mode** | | Mode 2 is lowest current range. Mode 1 has higher GBW. | | | | | Deep Sleep mode operation: $V_{DDA} \geq$ 2.7 V. $V_{IN}$ is 0.2 to $V_{DDA}$ – 1.5 V |
| SID_DS_1 | $I_{DD_HI_M1}$ | Mode 1, High current | – | | 1500 | µA | Typ at 25 °C |
| SID_DS_2 | $I_{DD_MED_M1}$ | Mode 1, Medium current | – | 460 | 600 | µA | Typ at 25 °C |
| SID_DS_3 | $I_{DD_LOW_M1}$ | Mode 1, Low current | – | 230 | 350 | µA | Typ at 25 °C |
| SID_DS_4 | $I_{DD_HI_M2}$ | Mode 2, High current | – | 120 | – | µA | 25 °C |
| SID_DS_5 | $I_{DD_MED_M2}$ | Mode 2, Medium current | – | 60 | – | µA | 25 °C |
| SID_DS_6 | $I_{DD_LOW_M2}$ | Mode 2, Low current | – | 15 | – | µA | 25 °C |

**(table continues...)**

**Table 20 (continued) Opamp specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID_DS_7 | GBW_HI_M1 | Mode 1, High current | – | 4 | – | MHz | 25 °C |
| SID_DS_8 | GBW_MED_M1 | Mode 1, Medium current | – | 2 | – | MHz | 25 °C |
| SID_DS_9 | GBW_LOW_M1 | Mode 1, Low current | – | 0.5 | – | MHz | 25 °C |
| SID_DS_10 | GBW_HI_M2 | Mode 2, High current | – | 0.5 | – | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA}$ – 1.5 V |
| SID_DS_11 | GBW_MED_M2 | Mode 2, Medium current | – | 0.2 | – | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA}$ – 1.5 V |
| SID_DS_12 | GBW_LOW_M2 | Mode 2, Low current | – | 0.1 | – | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA}$ – 1.5 V |
| SID_DS_13 | $V_{OS_HI_M1}$ | Mode 1, High current | – | 5 | – | mV | 25 °C, 0.2 V to $V_{DDA}$ – 1.5 V |
| SID_DS_14 | $V_{OS_MED_M1}$ | Mode 1, Medium current | – | 5 | – | mV | 25 °C, 0.2 V to $V_{DDA}$ – 1.5 V |
| SID_DS_15 | $V_{OS_LOW_M1}$ | Mode 1, Low current | – | 5 | – | mV | 25 °C, 0.2 V to $V_{DDA}$ – 1.5 V |
| SID_DS_16 | $V_{OS_HI_M2}$ | Mode 2, High current | – | 5 | – | mV | 25 °C, 0.2 V to $V_{DDA}$ – 1.5 V |
| SID_DS_17 | $V_{OS_MED_M2}$ | Mode 2, Medium current | – | 5 | – | mV | 25 °C, 0.2 V to $V_{DDA}$ – 1.5 V |
| SID_DS_18 | $V_{OS_LOW_M2}$ | Mode 2, Low current | – | 5 | – | mV | 25 °C, 0.2 V to $V_{DDA}$ – 1.5 V |
| SID_DS_19 | $I_{OUT_HI_M1}$ | Mode 1, High current | – | 10 | – | mA | Output is 0.5 V to $V_{DDA}$ – 0.5 V |
| SID_DS_20 | $I_{OUT_MED_M1}$ | Mode 1, Medium current | – | 10 | – | mA | Output is 0.5 V to $V_{DDA}$ – 0.5 V |
| SID_DS_21 | $I_{OUT_LOW_M1}$ | Mode 1, Low current | – | 4 | – | mA | Output is 0.5 V to $V_{DDA}$ – 0.5 V |
| SID_DS_22 | $I_{OUT_HI_M2}$ | Mode 2, High current | – | 1 | – | mA | Output is 0.5 V to $V_{DDA}$ – 0.5 V |
| SID_DS_23 | $I_{OUT_MED_M2}$ | Mode 2, Medium current | – | 1 | – | mA | Output is 0.5 V to $V_{DDA}$ – 0.5 V |
| SID_DS_24 | $I_{OUT_LOW_M2}$ | Mode 2, Low current | – | 0.5 | – | mA | Output is 0.5 V to $V_{DDA}$ – 0.5 V |

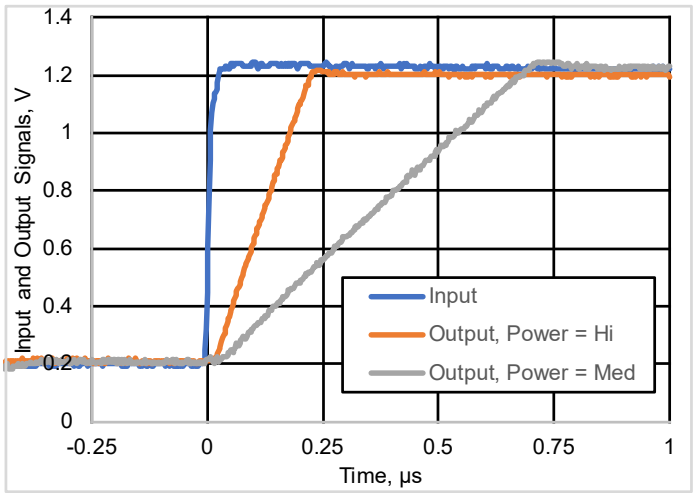



**Figure 17 Opamp step response, rising**

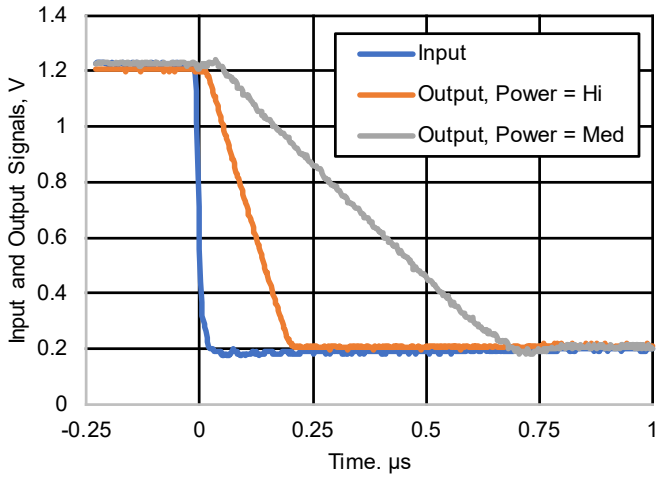



**Figure 18 Opamp step response, falling**

## 6.3.2 Low-Power (LP) Comparator

**Table 21 LP Comparator DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID84 | $V_{OFFSET1}$ | Input offset voltage for COMP1. Normal power mode. | -10 | – | 10 | mV | COMP0 offset is ±25 mV |
| SID85A | $V_{OFFSET2}$ | Input offset voltage. Low-power mode. | -25 | ±12 | 25 | mV | – |

**(table continues...)**

**Table 21 (continued) LP Comparator DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID85B | $V_{OFFSET3}$ | Input offset voltage. Ultra low-power mode. | -25 | ±12 | 25 | mV | – |
| SID86 | $V_{HYST1}$ | Hysteresis when enabled in Normal mode | – | – | 60 | mV | – |
| SID86A | $V_{HYST2}$ | Hysteresis when enabled in Low-power mode | – | – | 80 | mV | – |
| SID87 | $V_{ICM1}$ | Input common mode voltage in Normal mode | 0 | – | $V_{DDIO1}$ – 0.1 | V | – |
| SID247 | $V_{ICM2}$ | Input common mode voltage in Low power mode | 0 | – | $V_{DDIO1}$ – 0.1 | V | – |
| SID247A | $V_{ICM3}$ | Input common mode voltage in Ultra low power mode | 0 | – | $V_{DDIO1}$ – 0.1 | V | – |
| SID88 | CMRR | Common mode rejection ratio in Normal power mode | 50 | – | – | dB | – |
| SID89 | $I_{CMP1}$ | Block Current, Normal mode | – | – | 150 | µA | – |
| SID248 | $I_{CMP2}$ | Block Current, Low power mode | – | – | 10 | µA | – |
| SID259 | $I_{CMP3}$ | Block Current in Ultra low-power mode | – | 0.3 | 0.85 | µA | – |
| SID90 | ZCMP | DC Input impedance of comparator | 35 | – | – | MΩ | – |

**Table 22 LP Comparator AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID91 | $T_{RESP1}$ | Response time, Normal mode, 100 mV overdrive | – | – | 100 | ns | – |
| SID258 | $T_{RESP2}$ | Response time, Low power mode, 100 mV overdrive | – | – | 1000 | ns | – |
| SID92 | $T_{RESP3}$ | Response time, Ultra-low power mode, 100 mV overdrive | – | – | 20 | µs | – |
| SID92E | T_CMP_EN1 | Time from Enabling to operation | – | – | 10 | µs | Normal and Low-power modes |
| SID92F | T_CMP_EN2 | Time from Enabling to operation | – | – | 50 | µs | Ultra low-power mode |

**Table 23 Temperature sensor specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID93 | $T_{SENSACC}$ | Temperature sensor accuracy | –5 | ±1 | 5 | °C | –40 to +85°C |

**Table 24 Internal reference specification**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID93R | $V_{REFBG}$ | – | 1.188 | 1.2 | 1.212 | V | – |

## 6.3.3 SAR ADC

**Table 25 12-bit SAR ADC DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID94 | A_RES | SAR ADC Resolution | – | – | 12 | bits | – |
| SID95 | A_CHNLS_S | Number of channels - single-ended | – | – | 16 | – | 8 full speed. |
| SID96 | A-CHNKS_D | Number of channels - differential | – | – | 8 | – | Diff inputs use neighboring I/O |
| SID97 | A-MONO | Monotonicity | – | – | – | – | Yes |
| SID98 | A_GAINERR | Gain error | – | – | ±0.2 | % | With external reference. |
| SID99 | A_OFFSET | Input offset voltage | – | – | 2 | mV | Measured with 1-V reference |
| SID100 | A_ISAR_1 | Current consumption at 1 Msps | – | – | 1 | mA | At 1 Msps. External Bypass Cap. |
| SID100A | A_ISAR_2 | Current consumption at 1 Msps. Reference = $V_{DD}$ | – | – | 1.25 | mA | At 1 Msps. External Bypass Cap. |
| SID101 | A_VINS | Input voltage range - single-ended | $V_{SS}$ | – | $V_{DDA}$ | V | – |
| SID102 | A_VIND | Input voltage range - differential | $V_{SS}$ | – | $V_{DDA}$ | V | – |
| SID103 | A_INRES | Input resistance | – | – | 2.2 | kΩ | – |
| SID104 | A_INCAP | Input capacitance | – | – | 10 | pF | – |

**Table 26 12-bit SAR ADC AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **12-bit SAR ADC AC specifications** | | | | | | | |
| SID106 | A_PSRR | Power supply rejection ratio | 70 | – | – | dB | – |

**(table continues...)**

**Table 26 (continued) 12-bit SAR ADC AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID107 | A_CMRR | Common mode rejection ratio | 66 | – | – | dB | Measured at 1 V. |
| **One Megasample per second mode:** | | | | | | | |
| SID108 | A_SAMP_1 | Sample rate with external reference bypass cap. | – | – | 1 | Msps | – |
| SID108A | A_SAMP_2 | Sample rate with no bypass cap; Reference = $V_{DD}$ | – | – | 250 | ksps | – |
| SID108B | A_SAMP_3 | Sample rate with no bypass cap. Internal reference. | – | – | 100 | ksps | – |
| SID109 | A_SINAD | Signal-to-noise and Distortion ratio (SINAD). $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps. | 64 | – | – | dB | Fin = 10 kHz |
| SID111A | A_INL | Integral Non Linearity. $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps | –2 | – | 2 | LSB | Measured with internal $V_{REF}$ = 1.2 V and bypass cap. |
| SID111B | A_INL | Integral Non Linearity. $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps | –4 | – | 4 | LSB | Measured with external $V_{REF} \geq 1$ V and $V_{IN}$ common mode < 2 * Vref. |
| SID112A | A_DNL | Differential Non Linearity. $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps | –1 | – | 1.4 | LSB | Measured with internal $V_{REF}$ = 1.2 V and bypass cap. |
| SID112B | A_DNL | Differential Non Linearity. $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps | –1 | – | 1.7 | LSB | Measured with external $V_{REF} \geq 1$ V and $V_{IN}$ common mode < 2 * Vref. |
| SID113 | A_THD | Total harmonic distortion. $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps. | – | – | –65 | dB | Fin = 10 kHz |

## 6.3.4 DAC

**Table 27 12-bit DAC DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| SID108D | DAC_RES | DAC resolution | – | – | 12 | bits | – |
| SID111D | DAC_INL | Integral non-linearity | –4 | – | 4 | LSB | – |
| SID112D | DAC_DNL | Differential non-linearity | –2 | – | 2 | LSB | Monotonic to 11 bits. |

**(table continues...)**

**Table 27 (continued) 12-bit DAC DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| SID99D | DAC_OFFSET | Output Voltage zero offset error | –2 | – | 1 | mV | For 000 (hex) |
| SID103D | DAC_OUT_RES | DAC Output Resistance | – | 15 | – | kΩ | – |
| SID100D | DAC_IDD | DAC Current | – | – | 125 | µA | – |
| SID101D | DAC_QIDD | DAC Current when DAC stopped | – | – | 1 | µA | – |

**Table 28 12-bit DAC AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID109D | DAC_CONV | DAC Settling time | – | – | 2 | µs | Driving through CTBm buffer; 25-pF load |
| SID110D | DAC_Wakeup | Time from Enabling to ready for conversion | – | – | 10 | µs | – |

## 6.3.5 CSD

**Table 29 Capacitive Sigma-Delta (CSD) specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **CSD V2 specifications** | | | | | | | |
| SYS.PER#3 | $V_{DD_RIPPLE}$ | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | $V_{DDA}$ > 2 V (with ripple), 25°C $T_A$, Sensitivity = 0.1 pF |
| SYS.PER#16 | $V_{DD_RIPPLE_1.8}$ | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | $V_{DDA}$ > 1.75 V (with ripple), 25° C $T_A$, Parasitic Capacitance ($C_P$) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD.BLK | $I_{CSD}$ | Maximum block current | | | 4500 | µA | – |
| SID.CSD#15 | $V_{REF}$ | Voltage reference for CSD and Comparator | 0.6 | 1.2 | $V_{DDA}$ – 0.6 | V | $V_{DDA} - V_{REF} \geq 0.6$ V |
| SID.CSD#15A | $V_{REF_EXT}$ | External Voltage reference for CSD and Comparator | 0.6 | | $V_{DDA}$ – 0.6 | V | $V_{DDA} - V_{REF} \geq 0.6$ V |
| SID.CSD#16 | $I_{DAC1IDD}$ | IDAC1 (7-bits) block current | – | – | 1900 | µA | – |
| SID.CSD#17 | $I_{DAC2IDD}$ | IDAC2 (7-bits) block current | – | – | 1900 | µA | – |
| SID308 | $V_{CSD}$ | Voltage range of operation | 1.7 | – | 3.6 | V | 1.71 to 3.6 V |

**(table continues...)**

**Table 29 (continued) Capacitive Sigma-Delta (CSD) specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID308A | $V_{COMPIDAC}$ | Voltage compliance range of IDAC | 0.6 | – | $V_{DDA}$ – 0.6 | V | $V_{DDA} - V_{REF} \geq 0.6$ V |
| SID309 | $I_{DAC1DNL}$ | DNL | –1 | – | 1 | LSB | – |
| SID310 | $I_{DAC1INL}$ | INL | –3 | – | 3 | LSB | If $V_{DDA} < 2$ V then for LSB of 2.4 µA or less |
| SID311 | $I_{DAC2DNL}$ | DNL | –1 | – | 1 | LSB | – |
| SID312 | $I_{DAC2INL}$ | INL | –3 | – | 3 | LSB | If $V_{DDA} < 2$ V then for LSB of 2.4 µA or less |
| **SNRC of the following is ratio of counts of finger to noise. Guaranteed by characterization** | | | | | | | |
| SID313_1A | SNRC_1 | SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5 | – | – | Ratio | 9.5-pF maximum capacitance |
| SID313_1B | SNRC_2 | SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5 | – | – | Ratio | 31-pF maximum capacitance |
| SID313_1C | SNRC_3 | SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5 | – | – | Ratio | 61-pF maximum capacitance |
| SID313_2A | SNRC_4 | PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5 | – | – | Ratio | 12-pF maximum capacitance |
| SID313_2B | SNRC_5 | PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5 | – | – | Ratio | 47-pF maximum capacitance |
| SID313_2C | SNRC_6 | PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5 | – | – | Ratio | 86-pF maximum capacitance |
| SID313_3A | SNRC_7 | PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity | 5 | – | – | Ratio | 27-pF maximum capacitance |
| SID313_3B | SNRC_8 | PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity | 5 | – | – | Ratio | 86-pF maximum capacitance |
| SID313_3C | SNRC_9 | PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity | 5 | – | – | Ratio | 168-pF maximum capacitance |
| SID314 | $I_{DAC1CRT1}$ | Output current of IDAC1 (7 bits) in low range | 4.2 | | 5.7 | µA | LSB = 37.5-nA typ |
| SID314A | $I_{DAC1CRT2}$ | Output current of IDAC1(7 bits) in medium range | 33.7 | | 45.6 | µA | LSB = 300-nA typ. |

**(table continues...)**

**Table 29 (continued) Capacitive Sigma-Delta (CSD) specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID314B | $I_{DAC1CRT3}$ | Output current of IDAC1(7 bits) in high range | 270 | | 365 | µA | LSB = 2.4-µA typ. |
| SID314C | $I_{DAC1CRT12}$ | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | | 11.4 | µA | LSB = 37.5-nA typ. 2X output stage |
| SID314D | $I_{DAC1CRT22}$ | Output current of IDAC1(7 bits) in medium range, 2X mode | 67 | | 91 | µA | LSB = 300-nA typ. 2X output stage |
| SID314E | $I_{DAC1CRT32}$ | Output current of IDAC1(7 bits) in high range, 2X mode. $V_{DDA} > 2$ V | 540 | | 730 | µA | LSB = 2.4-µA typ. 2X output stage |
| SID315 | $I_{DAC2CRT1}$ | Output current of IDAC2 (7 bits) in low range | 4.2 | | 5.7 | µA | LSB = 37.5-nA typ. |
| SID315A | $I_{DAC2CRT2}$ | Output current of IDAC2 (7 bits) in medium range | 33.7 | | 45.6 | µA | LSB = 300-nA typ. |
| SID315B | $I_{DAC2CRT3}$ | Output current of IDAC2 (7 bits) in high range | 270 | | 365 | µA | LSB = 2.4-µA typ. |
| SID315C | $I_{DAC2CRT12}$ | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | | 11.4 | µA | LSB = 37.5-nA typ. 2X output stage |
| SID315D | $I_{DAC2CRT22}$ | Output current of IDAC2(7 bits) in medium range, 2X mode | 67 | | 91 | µA | LSB = 300-nA typ. 2X output stage |
| SID315E | $I_{DAC2CRT32}$ | Output current of IDAC2(7 bits) in high range, 2X mode. $V_{DDA} > 2$ V | 540 | | 730 | µA | LSB = 2.4-µA typ. 2X output stage |
| SID315F | $I_{DAC3CRT13}$ | Output current of IDAC in 8-bit mode in low range | 8 | | 11.4 | µA | LSB = 37.5-nA typ. |
| SID315G | $I_{DAC3CRT23}$ | Output current of IDAC in 8-bit mode in medium range | 67 | | 91 | µA | LSB = 300-nA typ. |
| SID315H | $I_{DAC3CRT33}$ | Output current of IDAC in 8-bit mode in high range. $V_{DDA} > 2V$ | 540 | | 730 | µA | LSB = 2.4-µA typ. |
| SID320 | $I_{DACOFFSET}$ | All zeroes input | – | – | 1 | LSB | Polarity set by Source or Sink |
| SID321 | $I_{DACGAIN}$ | Full-scale error less offset | – | – | ±15 | % | LSB = 2.4-µA typ. |
| SID322 | $I_{DACMISMATCH1}$ | Mismatch between IDAC1 and IDAC2 in Low mode | – | – | 9.2 | LSB | LSB = 37.5-nA typ. |

**(table continues...)**

**Table 29 (continued) Capacitive Sigma-Delta (CSD) specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID322A | $I_{DACMISMATCH2}$ | Mismatch between IDAC1 and IDAC2 in Medium mode | – | – | 6 | LSB | LSB = 300-nA typ. |
| SID322B | $I_{DACMISMATCH3}$ | Mismatch between IDAC1 and IDAC2 in High mode | – | – | 5.8 | LSB | LSB = 2.4-µA typ. |
| SID323 | $I_{DACSET8}$ | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID324 | $I_{DACSET7}$ | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID325 | CMOD | External modulator capacitor. | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap. |

**Table 30 CSD ADC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **CSDv2 ADC specifications** | | | | | | | |
| SIDA94 | A_RES | Resolution | – | – | 10 | bits | Auto-zeroing is required every millisecond |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | – | 16 | – |
| SIDA97 | A-MONO | Monotonicity | – | – | Yes | – | $V_{REF}$ mode |
| SIDA98 | A_GAINERR_VREF | Gain error | – | 0.6 | – | % | Reference Source: SRSS ($V_{REF}$ = 1.20 V, $V_{DDA}$ < 2.2 V), ($V_{REF}$ = 1.6 V, 2.2 V < $V_{DDA}$ < 2.7 V), ($V_{REF}$ = 2.13 V, $V_{DDA}$ > 2.7 V) |
| SIDA98A | A_GAINERR_VDDA | Gain error | – | 0.2 | – | % | Reference Source: SRSS ($V_{REF}$ = 1.20 V, $V_{DDA}$ < 2.2V), ($V_{REF}$ = 1.6 V, 2.2 V < $V_{DDA}$ < 2.7 V), ($V_{REF}$ = 2.13 V, $V_{DDA}$ > 2.7 V) |
| SIDA99 | A_OFFSET_VREF | Input offset voltage | – | 0.5 | – | LSB | After ADC calibration, Ref. Src = SRSS, ($V_{REF}$ = 1.20 V, $V_{DDA}$ < 2.2 V), ($V_{REF}$ = 1.6 V, 2.2 V < $V_{DDA}$ < 2.7 V), ($V_{REF}$ = 2.13 V, $V_{DDA}$ > 2.7 V) |

**(table continues...)**

**Table 30 (continued) CSD ADC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SIDA99A | A_OFFSET_VDDA | Input offset voltage | – | 0.5 | – | LSB | After ADC calibration, Ref. Src = SRSS, ($V_{REF}$ = 1.20 V, $V_{DDA}$ < 2.2 V), ($V_{REF}$ = 1.6 V, 2.2 V < $V_{DDA}$ < 2.7 V), ($V_{REF}$ = 2.13 V, $V_{DDA}$ > 2.7 V) |
| SIDA100 | A_ISAR_VREF | Current consumption | – | 0.3 | – | mA | CSD ADC Block current |
| SIDA100A | A_ISAR_VDDA | Current consumption | – | 0.3 | – | mA | CSD ADC Block current |
| SIDA101 | A_VINS_VREF | Input voltage range - single ended | $V_{SSA}$ | – | $V_{REF}$ | V | ($V_{REF}$ = 1.20 V, $V_{DDA}$ < 2.2 V), ($V_{REF}$ = 1.6 V, 2.2 V < $V_{DDA}$ < 2.7 V), ($V_{REF}$ = 2.13 V, $V_{DDA}$ > 2.7 V) |
| SIDA101A | A_VINS_VDDA | Input voltage range - single ended | $V_{SSA}$ | – | $V_{DDA}$ | V | ($V_{REF}$ = 1.20 V, $V_{DDA}$ < 2.2 V), ($V_{REF}$ = 1.6 V, 2.2 V < $V_{DDA}$ < 2.7 V), ($V_{REF}$ = 2.13 V, $V_{DDA}$ > 2.7 V) |
| SIDA103 | A_INRES | Input charging resistance | – | 15 | – | kΩ | – |
| SIDA104 | A_INCAP | Input capacitance | – | 41 | – | pF | – |
| SIDA106 | A_PSRR | Power supply rejection ratio (DC) | – | 60 | – | dB | – |
| SIDA107 | A_TACQ | Sample acquisition time | – | 10 | – | µs | Measured with 50-Ω source impedance. 10 µs is default software driver acquisition time setting. Settling to within 0.05%. |
| SIDA108 | A_CONV8 | Conversion time for 8-bit resolution at conversion rate = Fhclk/(2"(N+2)). Clock frequency = 50 MHz. | – | 25 | – | µs | Does not include acquisition time. |
| SIDA108A | A_CONV10 | Conversion time for 10-bit resolution at conversion rate = Fhclk/(2"(N+2)). Clock frequency = 50 MHz. | – | 60 | – | µs | Does not include acquisition time. |
| SIDA109 | A_SND_VRE | Signal-to-noise and Distortion ratio (SINAD) | – | 57 | – | dB | Measured with 50-Ω source impedance |
| SIDA109A | A_SND_VDDA | Signal-to-noise and Distortion ratio (SINAD) | – | 52 | – | dB | Measured with 50-Ω source impedance |

**(table continues...)**

**Table 30 (continued) CSD ADC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SIDA111 | A_INL_VREF | Integral non-linearity. 11.6 ksps | – | – | 2 | LSB | Measured with 50-Ω source impedance |
| SIDA111A | A_INL_VDDA | Integral non-linearity. 11.6 ksps | – | – | 2 | LSB | Measured with 50-Ω source impedance |
| SIDA112 | A_DNL_VREF | Differential non-linearity. 11.6 ksps | – | – | 1 | LSB | Measured with 50-Ω source impedance |
| SIDA112A | A_DNL_VDDA | Differential non- linearity. 11.6 ksps | – | – | 1 | LSB | Measured with 50-Ω source impedance |

## 6.4 Digital peripherals

**Table 31 Timer/Counter/PWM (TCPWM) specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.TCPWM.1 | $I_{TCPWM1}$ | Block current consumption at 8 MHz | – | – | 70 | µA | All modes (TCPWM) |
| SID.TCPWM.2 | $I_{TCPWM2}$ | Block current consumption at 24 MHz | – | – | 180 | µA | All modes (TCPWM) |
| SID.TCPWM.2A | $I_{TCPWM3}$ | Block current consumption at 50 MHz | – | – | 270 | µA | All modes (TCPWM) |
| SID.TCPWM.2B | $I_{TCPWM4}$ | Block current consumption at 100 MHz | – | – | 540 | µA | All modes (TCPWM) |
| SID.TCPWM.3 | $TCPWM_{FREQ}$ | Operating frequency | – | – | 100 | MHz | Fc max = Fcpu<br>Maximum = 100 MHz |
| SID.TCPWM.4 | $TPWM_{ENEXT}$ | Input Trigger Pulse Width for all Trigger Events | 2 / Fc | – | – | ns | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. Fc is counter operating frequency. |
| SID.TCPWM.5 | $TPWM_{EXT}$ | Output Trigger Pulse widths | 1.5 / Fc | – | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs |
| SID.TCPWM.5A | $TC_{RES}$ | Resolution of Counter | 1 / Fc | – | – | ns | Minimum time between successive counts |
| SID.TCPWM.5B | $PWM_{RES}$ | PWM Resolution | 1 / Fc | – | – | ns | Minimum pulse width of PWM Output |

**(table continues...)**

**Table 31 (continued) Timer/Counter/PWM (TCPWM) specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.TCPWM.5C | $Q_{RES}$ | Quadrature inputs resolution | 2 / Fc | – | – | ns | Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar. |

**Table 32 Serial Communication Block (SCB) specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **Fixed $I^2C$ DC specifications** | | | | | | | |
| SID149 | $I_{I2C1}$ | Block current consumption at 100 kHz | – | – | 30 | µA | – |
| SID150 | $I_{I2C2}$ | Block current consumption at 400 kHz | – | – | 80 | µA | – |
| SID151 | $I_{I2C3}$ | Block current consumption at 1 Mbps | – | – | 180 | µA | – |
| SID152 | $I_{I2C4}$ | I2C enabled in Deep Sleep mode | – | – | 1.7 | µA | At 60°C |
| **Fixed $I^2C$ AC specifications** | | | | | | | |
| SID153 | $F_{I2C1}$ | Bit rate | – | – | 1 | Mbps | – |
| **Fixed UART DC specifications** | | | | | | | |
| SID160 | $I_{UART1}$ | Block current consumption at 100 kbps | – | – | 30 | µA | – |
| SID161 | $I_{UART2}$ | Block current consumption at 1000 kbps | – | – | 180 | µA | – |
| **Fixed UART AC specifications** | | | | | | | |
| SID162A | $F_{UART1}$ | Bit rate | – | – | 3 | Mbps | ULP Mode |
| SID162B | $F_{UART2}$ | | | – | 8 | | LP Mode |
| **Fixed SPI DC specifications** | | | | | | | |
| SID163 | $I_{SPI1}$ | Block current consumption at 1 Mbps | – | – | 220 | µA | – |
| SID164 | $I_{SPI2}$ | Block current consumption at 4 Mbps | – | – | 340 | µA | – |
| SID165 | $I_{SPI3}$ | Block current consumption at 8 Mbps | – | – | 360 | µA | – |
| SID165A | $I_{SP14}$ | Block current consumption at 25 Mbps | – | – | 800 | µA | – |

**(table continues...)**

**Table 32 (continued) Serial Communication Block (SCB) specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **Fixed SPI AC specifications for LP Mode (1.1 V) unless noted otherwise.** | | | | | | | |
| SID166 | $F_{SPI}$ | SPI Operating Frequency Master and Externally Clocked Slave | – | – | 25 | MHz | 14-MHz max for ULP (0.9 V) mode |
| SID166A | $F_{SPI_IC}$ | SPI Slave Internally Clocked | – | – | 15 | MHz | 5-MHz max for ULP (0.9 V) mode |
| SID166B | $F_{SPI_EXT}$ | SPI Operating Frequency Master ($F_{SCB}$ is SPI Clock) | – | – | $F_{SCB}/4$ | MHz | $F_{SCB}$ max is 100 MHz in LP mode, 25 MHz max in ULP mode |
| **Fixed SPI Master mode AC specifications for LP Mode (1.1 V) unless noted otherwise.** | | | | | | | |
| SID167 | $T_{DMO}$ | MOSI Valid after SClock driving edge | – | – | 12 | ns | 20-ns max for ULP (0.9 V) mode |
| SID168 | $T_{DSI}$ | MISO Valid before SClock capturing edge | 5 | – | – | ns | Full clock, late MISO sampling |
| SID169 | $T_{HMO}$ | MOSI data hold time | 0 | – | – | ns | Referred to Slave capturing edge |
| SID169A | $T_{SSELMSCK1}$ | SSEL Valid to first SCK Valid edge | 18 | – | – | ns | Referred to Master clock edge |
| SID169B | $T_{SSELMSCK2}$ | SSEL Hold after last SCK Valid edge | 18 | – | – | ns | Referred to Master clock edge |
| **Fixed SPI Slave mode AC specifications for LP Mode (1.1 V) unless noted otherwise.** | | | | | | | |
| SID170 | $T_{DMI}$ | MOSI Valid before Sclock Capturing edge | 5 | – | – | ns | – |
| SID171A | $T_{DSO_EXT}$ | MISO Valid after Sclock driving edge in Ext. Clk. mode | – | – | 20 | ns | 35-ns max. for ULP (0.9 V) mode |
| SID171 | $T_{DSO}$ | MISO Valid after Sclock driving edge in Internally Clk. Mode | – | – | $T_{DSO_EXT}$ + 3 × Tscb | ns | Tscb is Serial Comm. Block clock period. |
| SID171B | $T_{DSO}$ | MISO Valid after Sclock driving edge in Internally Clk. Mode with Median filter enabled. | – | – | $T_{DSO_EXT}$ + 4 × Tscb | ns | Tscb is Serial Comm. Block clock period. |
| SID172 | $T_{HSO}$ | Previous MISO data hold time | 5 | – | – | ns | – |
| SID172A | $TSSEL_{SCK1}$ | SSEL Valid to first SCK Valid edge | 65 | – | – | ns | – |
| SID172B | $TSSEL_{SCK2}$ | SSEL Hold after Last SCK Valid edge | 65 | – | – | ns | |

### 6.4.1 LCD specifications

**Table 33 LCD direct drive DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID154 | $I_{LCDLOW}$ | Operating current in low-power mode | – | 5 | – | µA | 16 × 4 small segment display at 50 Hz |
| SID155 | $C_{LCDCAP}$ | LCD capacitance per segment/ common driver | – | 500 | 5000 | pF | – |
| SID156 | $LCD_{OFFSET}$ | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | $I_{LCDOP1}$ | PWM Mode current.<br>3.3-V bias. 8-MHz IMO. 25°C. | – | 0.6 | – | mA | 32 × 4 segments<br>50 Hz |
| SID158 | $I_{LCDOP2}$ | PWM Mode current.<br>3.3-V bias. 8-MHz IMO. 25°C. | – | 0.5 | – | mA | 32 × 4 segments 50 Hz |

**Table 34 LCD direct drive AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID159 | $F_{LCD}$ | LCD frame rate | 10 | 50 | 150 | Hz | – |

## 6.5 Memory

### 6.5.1 Flash

**Table 35 Flash DC specifications[1)]**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID173A | $I_{PE}$ | Erase and program current | – | – | 6 | mA | – |

*1)* It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

**Table 36 Flash AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID174 | $T_{ROWWRITE}$ | Row write time (erase & program) | – | – | 16 | ms | Row = 512 bytes |
| SID175 | $T_{ROWERASE}$ | Row erase time | – | – | 11 | ms | – |
| SID176 | $T_{ROWPROGRAM}$ | Row program time after erase | – | – | 5 | ms | – |
| SID178 | $T_{BULKERASE}$ | Bulk erase time (1024 KB) | – | – | 11 | ms | – |
| SID179 | $T_{SECTORERASE}$ | Sector erase time (256 KB) | – | – | 11 | ms | 512 rows per sector |
| SID178S | $T_{SSERIAE}$ | Subsector erase time | – | – | 11 | ms | 8 rows per subsector |

**(table continues...)**

**Table 36 (continued) Flash AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID179S | $T_{SSWRITE}$ | Subsector write time; 1 erase plus 8 program times | – | – | 51 | ms | – |
| SID180S | $T_{SWRITE}$ | Sector write time; 1 erase plus 512 program times | – | – | 2.6 | seconds | – |
| SID180 | $T_{DEVPROG}$ | Total device write time | – | – | 15 | seconds | – |
| SID181 | $F_{END}$ | Flash Endurance | 100 k | – | – | cycles | – |
| SID182 | $F_{RET1}$ | Flash Retention. $T_A \leq 25°C$, 100 k P/E cycles | 10 | – | – | years | – |
| SID182A | $F_{RET2}$ | Flash Retention. $T_A \leq 85°C$, 10 k P/E cycles | 10 | – | – | years | – |
| SID182B | $F_{RET3}$ | Flash Retention. $T_A \leq 55°C$, 20 k P/E cycles | 20 | – | – | years | – |
| SID256 | $T_{WS100}$ | Number of Wait states at 100 MHz | 3 | – | – | | – |
| SID257 | $T_{WS50}$ | Number of Wait states at 50 MHz | 2 | – | – | | – |

## 6.6 System resources

### 6.6.1 Power-on-reset

**Table 37 Power-on reset (POR) with brown-out detect (BOD) DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID190 | $V_{FALLPPOR}$ | BOD trip voltage in system LP and ULP modes. | 1.54 | – | – | V | Reset guaranteed for $V_{DDD}$ levels below 1.54 V |
| SID192 | $V_{FALLDPSLP}$ | BOD trip voltage in system Deep Sleep mode. | 1.54 | – | – | V | |

**Table 38 POR with BOD AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID192A | $V_{DDRAMP}$ | Maximum power supply ramp rate (any supply) | – | – | 100 | mV/µs | System LP mode |
| SID194A | $V_{DDRAMP_DS}$ | Maximum power supply ramp rate (any supply) in system Deep Sleep mode | – | – | 10 | mV/µs | BOD operation guaranteed |

## 6.6.2 Voltage monitors

**Table 39 Voltage monitors DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID195R | $V_{HVD0}$ | | 1.18 | 1.23 | 1.27 | V | – |
| SID195 | $V_{HVDI1}$ | | 1.38 | 1.43 | 1.47 | V | – |
| SID196 | $V_{HVDI2}$ | | 1.57 | 1.63 | 1.68 | V | – |
| SID197 | $V_{HVDI3}$ | | 1.76 | 1.83 | 1.89 | V | – |
| SID198 | $V_{HVDI4}$ | | 1.95 | 2.03 | 2.1 | V | – |
| SID199 | $V_{HVDI5}$ | | 2.05 | 2.13 | 2.2 | V | – |
| SID200 | $V_{HVDI6}$ | | 2.15 | 2.23 | 2.3 | V | – |
| SID201 | $V_{HVDI7}$ | | 2.24 | 2.33 | 2.41 | V | – |
| SID202 | $V_{HVDI8}$ | | 2.34 | 2.43 | 2.51 | V | – |
| SID203 | $V_{HVDI9}$ | | 2.44 | 2.53 | 2.61 | V | – |
| SID204 | $V_{HVDI10}$ | | 2.53 | 2.63 | 2.72 | V | – |
| SID205 | $V_{HVDI11}$ | | 2.63 | 2.73 | 2.82 | V | – |
| SID206 | $V_{HVDI12}$ | | 2.73 | 2.83 | 2.92 | V | – |
| SID207 | $V_{HVDI13}$ | | 2.82 | 2.93 | 3.03 | V | – |
| SID208 | $V_{HVDI14}$ | | 2.92 | 3.03 | 3.13 | V | – |
| SID209 | $V_{HVDI15}$ | | 3.02 | 3.13 | 3.23 | V | – |
| SID211 | LVI_IDD | Block current | – | 5 | 15 | µA | – |

**Table 40 Voltage monitors AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID212 | $T_{MONTRIP}$ | Voltage monitor trip time | – | – | 170 | ns | – |

## 6.6.3 SWD and trace interface

**Table 41 SWD and trace specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| SID214 | F_SWDCLK2 | 1.7 V ≤ $V_{DDD}$ ≤ 3.6 V | – | – | 25 | MHz | LP mode. $V_{CCD}$ = 1.1 V |
| SID214L | F_SWDCLK2L | 1.7 V ≤ $V_{DDD}$ ≤ 3.6 V | – | – | 12 | MHz | ULP mode. $V_{CCD}$ = 0.9 V |
| SID215 | T_SWDI_SETUP | T = 1/f SWDCLK | 0.25 * T | – | – | ns | – |
| SID216 | T_SWDI_HOLD | T = 1/f SWDCLK | 0.25 * T | – | – | ns | – |
| SID217 | T_SWDO_VALID | T = 1/f SWDCLK | – | – | 0.5 * T | ns | – |

**(table continues...)**

**Table 41 (continued) SWD and trace specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| SID217A | T_SWDO_HOLD | T = 1/f SWDCLK | 1 | – | – | ns | – |
| SID214T | F_TRCLK_LP1 | With Trace Data setup/ hold times of 2/1 ns respectively | – | – | 75 | MHz | LP Mode. $V_{DD}$ = 1.1 V |
| SID215T | F_TRCLK_LP2 | With Trace Data setup/ hold times of 3/2 ns respectively | – | – | 70 | MHz | LP Mode. $V_{DD}$ = 1.1 V |
| SID216T | F_TRCLK_ULP | With Trace Data setup/ hold times of 3/2 ns respectively | – | – | 25 | MHz | ULP Mode. $V_{DD}$ = 0.9 V |

## 6.6.4 Internal Main Oscillator

**Table 42 IMO DC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID218 | $I_{IMO1}$ | IMO operating current at 8 MHz | – | 9 | 15 | µA | – |

**Table 43 IMO AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID223 | $F_{IMOTOL1}$ | Frequency variation centered on 8 MHz | – | – | ±2 | % | – |
| SID227 | $T_{JITR}$ | Cycle-to-Cycle and Period jitter | – | ±250 | – | ps | – |

## 6.6.5 Internal Low-Speed Oscillator

**Table 44 ILO DC specification**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID231 | $I_{ILO2}$ | ILO operating current at 32 kHz | – | 0.3 | 0.7 | µA | – |

**Table 45 ILO AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID234 | $T_{STARTILO1}$ | ILO startup time | – | – | 7 | µs | Startup time to 95% of final frequency |
| SID236 | $T_{LIODUTY}$ | ILO Duty cycle | 45 | 50 | 55 | % | – |
| SID237 | $F_{ILOTRIM1}$ | ILO frequency | 28.8 | 32 | 36.1 | kHz | Factory trimmed |

### 6.6.6 Crystal Oscillator

**Table 46 ECO specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **MHz ECO DC specifications** | | | | | | | |
| SID316 | $I_{DD_MHz}$ | Block operating current with Cload up to 18 pF | – | 800 | 1600 | µA | Max = 35 MHz, Typ = 16 MHz |
| **MHz ECO AC specifications** | | | | | | | |
| SID317 | F_MHz | Crystal frequency range | 16 | – | 35 | MHz | – |
| **kHz ECO DC specifications** | | | | | | | |
| SID318 | $I_{DD_kHz}$ | Block operating current with 32-kHz crystal | – | 0.38 | 1 | µA | – |
| SID321E | ESR32K | Equivalent Series Resistance | – | 80 | – | kΩ | – |
| SID322E | PD32K | Drive level | – | – | 1 | µW | – |
| **kHz ECO AC specifications** | | | | | | | |
| SID319 | F_kHz | 32-kHz frequency | – | 32.768 | – | kHz | – |
| SID320 | Ton_kHz | Startup time | – | – | 500 | ms | – |
| SID320E | $F_{TOL32K}$ | Frequency tolerance | – | 50 | 250 | ppm | – |

### 6.6.7 External clock

**Table 47 External clock specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID305 | $EXTCLK_{FREQ}$ | External Clock input Frequency | 0 | – | 100 | MHz | – |
| SID306 | $EXTCLK_{DUTY}$ | Duty cycle; Measured at $V_{DD/2}$ | 45 | – | 55 | % | – |

### 6.6.8 PLL

**Table 48 PLL specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID304P | PLL_IN | Input frequency to PLL block | 4 | – | 64 | MHz | |
| SID305P | PLL_LOCK | Time to achieve PLL Lock | – | 16 | 35 | µs | – |
| SID306P | PLL_OUT | Output frequency from PLL Block | 10.625 | – | 150 | MHz | – |
| SID307P | PLL_IDD | PLL Current | – | 0.55 | 1.1 | mA | Typ at 100 MHz out. |
| SID308P | PLL_JTR | Period Jitter | – | – | 150 | ps | 100-MHz output frequency |

## 6.6.9 Clock source switching time

**Table 49 Clock source switching time specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID262 | $TCLK_{SWITCH}$ | Clock switching from clk1 to clk2 in clock periods[1)] | – | – | 4 clk1 + 3 clk2 | periods | – |

*1)* As an example, if the clk_path[1] source is changed from the IMO to the FLL (see Figure 4) then clk1 is the IMO and clk2 is the FLL.

## 6.6.10 FLL

**Table 50 Frequency Locked Loop (FLL) specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID450 | FLL_RANGE | Input frequency range. | 0.001 | – | 100 | MHz | Lower limit allows lock to USB SOF signal (1 kHz). Upper limit is for External input. |
| SID451 | FLL_OUT_DIV2 | Output frequency range. $V_{CCD}$ = 1.1 V | 24.00 | – | 100.00 | MHz | Output range of FLL divided-by-2 output |
| SID451A | FLL_OUT_DIV2 | Output frequency range. $V_{CCD}$ = 0.9 V | 24.00 | – | 50.00 | MHz | Output range of FLL divided-by-2 output |
| SID452 | FLL_DUTY_DIV2 | Divided-by-2 output; High or Low | 47.00 | – | 53.00 | % | – |
| SID454 | FLL_WAKEUP | Time from stable input clock to 1% of final value on deep sleep wakeup | – | – | 7.50 | µs | With IMO input, less than 10°C change in temperature while in Deep Sleep, and Fout ≥ 50 MHz. |
| SID455 | FLL_JITTER | Period jitter (1 sigma at 100 MHz) | – | – | 35.00 | ps | 50 ps at 48 MHz, 35 ps at 100 MHz |
| SID456 | FLL_CURRENT | CCO + Logic current | – | – | 5.50 | µA/MHz | – |

## 6.6.11 UDB

**Table 51 UDB AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **Data path performance** | | | | | | | |
| SID249 | $F_{MAX-TIMER}$ | Max frequency of 16-bit timer in a UDB pair | – | – | 100 | MHz | – |

**(table continues...)**

**Table 51 (continued) UDB AC specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID250 | $F_{MAX-ADDER}$ | Max frequency of 16-bit adder in a UDB pair | – | – | 100 | MHz | – |
| SID251 | $F_{MAX_CRC}$ | Max frequency of 16-bit CRC/PRS in a UDB pair | – | – | 100 | MHz | – |
| **PLD performance in UDB** | | | | | | | |
| SID252 | $F_{MAX_PLD}$ | Max frequency of 2-pass PLD function in a UDB pair | – | – | 100 | MHz | – |
| **Clock to output performance** | | | | | | | |
| SID253 | $T_{CLK_OUT_UDB1}$ | Prop. delay for clock in to data out | – | 5 | – | ns | – |
| **UDB port adapter specifications** | | | | | | | |
| *Conditions: 10-pF load, 3-V $V_{DDIO}$ and $V_{DDD}$* | | | | | | | |
| SID263 | $T_{LCLKDO}$ | LCLK to Output delay | – | – | 11 | ns | LCLK is a selected clock; for more information see the reference manual |
| SID264 | $T_{DINLCLK}$ | Input setup time to LCLK rising edge | – | – | 7 | ns | – |
| SID265 | $T_{DINLCLKHLD}$ | Input hold time from LCLK rising edge | 5 | – | – | ns | – |
| SID266 | $T_{LCLKHIZ}$ | LCLK to Output tristated | – | – | 28 | ns | – |
| SID267 | $T_{FLCLK}$ | LCLK frequency | – | – | 33 | MHz | – |
| SID268 | $T_{LCLKDUTY}$ | LCLK duty cycle (percentage high) | 40% | – | 60% | % | – |

## 6.6.12 USB

**Table 52 USB specifications (USB requires LP mode 1.1-V internal supply)**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **USB block specifications** | | | | | | | |
| SID322U | Vusb_3.3 | Device supply for USB operation | 3.15 | – | 3.6 | V | USB Configured |
| SID323U | Vusb_3 | Device supply for USB operation (functional operation only) | 2.85 | – | 3.6 | V | USB Configured |
| SID325U | Iusb_config | Block supply current in Active mode | – | 8 | – | mA | $V_{DDD}$ = 3.3 V |
| SID328 | Iusb_suspend | Block supply current in suspend mode | – | 0.5 | – | mA | $V_{DDD}$ = 3.3 V, Device connected |

**(table continues...)**

**Table 52 (continued) USB specifications (USB requires LP mode 1.1-V internal supply)**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID329 | Iusb_suspend | Block supply current in suspend mode | – | 0.3 | – | mA | $V_{DDD}$ = 3.3 V, Device disconnected |
| SID330U | USB_Drive_Res | USB driver impedance | 28 | – | 44 | Ω | Series resistors are on chip |
| SID331U | USB_Pulldown | USB pull-down resistors in Host mode | 14.25 | – | 24.8 | kΩ | – |
| SID332U | USB_Pullup_Idle | Idle mode range | 900 | – | 1575 | Ω | Bus idle |
| SID333U | USB_Pullup | Active mode | 1425 | – | 3090 | Ω | Upstream device transmitting |

## 6.6.13 QSPI

**Table 53 QSPI Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| **SMIF QSPI specifications. All specs with 15-pF load.** | | | | | | | |
| SID390Q | Fsmifclock | SMIF QSPI output clock frequency | – | – | 80 | MHz | LP mode (1.1 V) |
| SID390QU | Fsmifclocku | SMIF QSPI output clock frequency | – | – | 50 | MHz | ULP mode (0.9 V). Guaranteed by Char. |
| SID397Q | Idd_qspi | Block current in LP mode (1.1 V) | – | – | 1900 | µA | LP mode (1.1 V) |
| SID398Q | Idd_qspi_u | Block current in ULP mode (0.9 V) | – | – | 590 | µA | ULP mode (0.9 V) |
| SID391Q | Tsetup | Input data set-up time with respect to clock capturing edge | 4.5 | – | – | ns | – |
| SID392Q | Tdatahold | Input data hold time with respect to clock capturing edge | 0 | – | – | ns | – |
| SID393Q | Tdataoutvalid | Output data valid time with respect to clock falling edge | – | – | 3.7 | ns | 7.5-ns max for ULP mode (0.9 V) |
| SID394Q | Tholdtime | Output data hold time with respect to clock rising edge | 3 | – | – | ns | – |
| SID395Q | Tseloutvalid | Output Select valid time with respect to clock rising edge | – | – | 7.5 | ns | 15-ns max for ULP mode (0.9 V) |
| SID396Q | Tselouthold | Output Select hold time with respect to clock rising edge | 0.5*Tsclk | – | – | ns | Tsclk = Fsmifclk cycle time |

## 6.6.14 Audio subsystem

**Table 54 Audio subsystem specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| **PDM specifications** | | | | | | | |
| SID400P | PDM_IDD1 | PDM Active current, Stereo operation, 1-MHz clock | – | 175 | – | µA | 16-bit audio at 16 ksps |
| SID401 | PDM_IDD2 | PDM Active current, Stereo operation, 3-MHz clock | – | 600 | – | µA | 24-bit audio at 48 ksps |
| SID402[1)] | PDM_JITTER | RMS Jitter in PDM clock | –200 | – | 200 | ps | – |
| SID403[1)] | PDM_CLK | PDM Clock speed | 0.384 | – | 3.072 | MHz | – |
| SID403A[1)] | PDM_BLK_CLK | PDM Block input clock | 1.024 | – | 49.152 | MHz | – |
| SID403B[1)] | PDM_SETUP | Data input set-up time to PDM_CLK edge | 10 | – | – | ns | – |
| SID403C[1)] | PDM_HOLD | Data input hold time to PDM_CLK edge | 10 | – | – | ns | – |
| SID404[1)] | PDM_OUT | Audio sample rate | 8 | – | 48 | ksps | – |
| SID405[1)] | PDM_WL | Word Length | 16 | – | 24 | bits | – |
| SID406[1)] | PDM_SNR | Signal-to-Noise Ratio (A-weighted) | – | 100 | – | dB | PDM input, 20 Hz to 20 kHz BW |
| SID407[1)] | PDM_DR | Dynamic Range (A-weighted) | – | 100 | – | dB | 20 Hz to 20 kHz BW, –60 dB FS |
| SID408[1)] | PDM_FR | Frequency Response | –0.2 | – | 0.2 | dB | DC to 0.45f. DC Blocking filter off. |
| SID409[1)] | PDM_SB | Stop Band | – | 0.566 | – | f | – |
| SID410[1)] | PDM_SBA | Stop Band Attenuation | – | 60 | – | dB | – |
| SID411[1)] | PDM_GAIN | Adjustable Gain | –12 | – | 10.5 | dB | PDM to PCM, 1.5 dB/step |
| SID412[1)] | PDM_ST | Startup time | – | 48 | – | WS (Word Select) cycles | |
| **I2S Specifications. The same for LP and ULP modes unless stated otherwise.** | | | | | | | |
| SID415 | I2S_IDD | Block current | – | 400 | – | µA | |
| SID413 | I2S_WORD | Length of I2S Word | 8 | – | 32 | bits | – |

**(table continues...)**

**Table 54 (continued) Audio subsystem specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| SID414 | I2S_WS | Word Clock frequency in LP mode | – | – | 192 | kHz | 12.288-MHz bit clock with 32-bit word |
| SID414M | I2S_WS_U | Word Clock frequency in ULP mode | – | – | 48 | kHz | 3.072-MHz bit clock with 32-bit word |
| SID414A | I2S_WS_TDM | Word Clock frequency in TDM mode for LP | – | – | 48 | kHz | Eight 32-bit channels |
| SID414X | I2S_WS_TDM_U | Word Clock frequency in TDM mode for ULP | – | – | 12 | kHz | Eight 32-bit channels |
| **I2S Slave mode** | | | | | | | |
| SID430 | TS_WS | WS Setup Time to the Following Rising Edge of SCK for LP Mode | 5 | – | – | ns | – |
| SID430U | TS_WS | WS Setup Time to the Following Rising Edge of SCK for ULP Mode | 11 | – | – | ns | – |
| SID430A | TH_WS | WS Hold Time to the Following Edge of SCK | TMCLK_SOC[2] + 5 | – | – | ns | – |
| SID432 | TD_SDO | Delay Time of TX_SDO Transition from Edge of TX_SCK for LP mode | – (TMCLK_SOC + 25) | – | TMCLK_SOC + 25 | ns | Associated clock edge depends on selected polarity |
| SID432U | TD_SDO | Delay Time of TX_SDO Transition from Edge of TX_SCK for ULP mode | – (TMCLK_SOC +70) | – | TMCLK_SOC + 70 | ns | Associated clock edge depends on selected polarity |
| SID433 | TS_SDI | RX_SDI Setup Time to the Following Edge of RX_SCK in Lp Mode | 5 | – | – | ns | – |
| SID433U | TS_SDI | RX_SDI Setup Time to the Following Edge of RX_SCK in ULP mode | 11 | – | – | ns | – |
| SID434 | TH_SDI | RX_SDI Hold Time to the Rising Edge of RX_SCK | TMCLK_SOC + 5 | – | – | ns | – |
| SID435 | TSCKCY | TX/RX_SCK Bit Clock Duty Cycle | 45 | – | 55 | % | – |
| **I2S Master mode** | | | | | | | |

**(table continues...)**

**Table 54 (continued) Audio subsystem specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| SID437 | TD_WS | WS Transition Delay from Falling Edge of SCK in LP mode | –10 | – | 20 | ns | – |
| SID437U | TD_WS_U | WS Transition Delay from Falling Edge of SCK in ULP mode | –10 | – | 40 | ns | – |
| SID438 | TD_SDO | SDO Transition Delay from Falling Edge of SCK in LP mode | –10 | – | 20 | ns | – |
| SID438U | TD_SDO | SDO Transition Delay from Falling Edge of SCK in ULP mode | –10 | – | 40 | ns | – |
| SID439 | TS_SDI | SDI Setup Time to the Associated Edge of SCK | 5 | – | – | ns | Associated clock edge depends on selected polarity |
| SID440 | TH_SDI | SDI Hold Time to the Associated Edge of SCK | TMCLK_SOC + 5 | – | – | ns | T is TX/RX_SCK Bit Clock period. Associated clock edge depends on selected polarity. |
| SID443 | TSCKCY | SCK Bit Clock Duty Cycle | 45 | – | 55 | % | – |
| SID445 | FMCLK_SOC | MCLK_SOC Frequency in LP mode | 1.024 | – | 98.304 | MHz | FMCLK_SOC = 8 * Bit-clock |
| SID445U | FMCLK_SOC_U | MCLK_SOC Frequency in ULP mode | 1.024 | – | 24.576 | MHz | FMCLK_SOC_U = 8 * Bit-clock |
| SID446 | TMCLKCY | MCLK_SOC Duty Cycle | 45 | – | 55 | % | – |
| SID447 | TJITTER | MCLK_SOC Input Jitter | –100 | – | 100 | ps | – |

*1)* Guaranteed by design, not production tested.
*2)* TMCLK_SOC is the internal I2S master clock period.

## 6.6.15 Smart I/O

**Table 55 Smart I/O specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID420 | SMIO_BYP | Smart I/O Bypass delay | – | – | 2 | ns | – |
| SID421 | SMIO_LUT | Smart I/O LUT prop delay | – | 8 | – | ns | – |

### 6.6.16 Precision ILO (PILO)

**Table 56 PILO specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID 430R | $I_{PILO}$ | Operating current | – | 1.2 | 4 | µA | – |
| SID431 | F_PILO | PILO nominal frequency | – | 32768 | – | Hz | T = 25°C |
| SID432R | ACC_PILO | PILO accuracy with periodic calibration | –500 | – | 500 | ppm | – |

### 6.6.17 JTAG boundary scan

**Table 57 JTAG boundary scan**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **JTAG boundary scan parameters** | | | | | | |
| **JTAG boundary scan parameters for 1.1 V (LP) mode operation:** | | | | | | |
| SID468 | TCKLOW | TCK LOW | 52 | – | – | ns | – |
| SID469 | TCKHIGH | TCK HIGH | 10 | – | – | ns | – |
| SID470 | TCK_TDO | TCK falling edge to output valid | | – | 40 | ns | – |
| SID471 | TSU_TCK | Input valid to TCK rising edge | 12 | – | – | ns | – |
| SID472 | TCk_THD | Input hold time to TCK rising edge | 10 | – | – | ns | – |
| SID473 | TCK_TDOV | TCK falling edge to output valid (High-Z to Active). | 40 | – | – | ns | – |
| SID474 | TCK_TDOZ | TCK falling edge to output valid (Active to High-Z). | 40 | – | – | ns | – |
| **JTAG boundary scan parameters for 0.9 V (ULP) mode operation:** | | | | | | |
| SID468A | TCKLOW | TCK low | 102 | – | – | ns | – |
| SID469A | TCKHIGH | TCK high | 20 | – | – | ns | – |
| SID470A | TCK_TDO | TCK falling edge to output valid | | – | 80 | ns | – |
| SID471A | TSU_TCK | Input valid to TCK rising edge | 22 | – | – | ns | – |
| SID472A | TCk_THD | Input hold time to TCK rising edge | 20 | – | – | ns | – |
| SID473A | TCK_TDOV | TCK falling edge to output valid (high-Z to active). | 80 | – | – | ns | – |
| SID474A | TCK_TDOZ | TCK falling edge to output valid (active to high-Z). | 80 | – | – | ns | – |

# 7 Ordering information

Table 58 lists the CY8C62x6 and CY8C62x7 part numbers and features. See also the product selector guide.

**Table 58 Marketing part numbers**

| Product[1] | CM4 CPU Speed [LP/ULP] (MHz) | CM0+ CPU Speed [LP/ULP] (MHz) | Flash (KB) | SRAM (KB) | Opamp | No. of UDBs | CAPSENSE™ | CRYPTO | "Secure Boot" | GPIOs | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CY8C6246BZI-D04 | 150/50 | 100/25 | 512 | 128 | – | 0 | – | – | – | 100 | 124-BGA |
| CY8C6246BZI-D04T | | | | | | | | | | | |
| CY8C6247BZI-D44 | 150/50 | 100/25 | 1024 | 288 | – | 0 | Y | Y | Y | 100 | 124-BGA |
| CY8C6247BZI-D44T | | | | | | | | | | | |
| CY8C6247BZI-D34 | 150/50 | 100/25 | 1024 | 288 | 2 | 12 | Y | – | – | 100 | 124-BGA |
| CY8C6247BZI-D34T | | | | | | | | | | | |
| CY8C6247BZI-D54 | 150/50 | 100/25 | 1024 | 288 | 2 | 12 | Y | Y | Y | 100 | 124-BGA |
| CY8C6247BZI-D54T | | | | | | | | | | | |
| CY8C6247FDI-D02T | 150/50 | 100/25 | 1024 | 288 | – | 0 | – | – | – | 62 | 80-WLCSP |
| CY8C6247FDI-D32T | 150/50 | 100/25 | 1024 | 288 | 2 | 12 | Y | – | – | 62 | 80-WLCSP |
| CY8C6247FTI-D52T | 150/50 | 100/25 | 1024 | 288 | 2 | 12 | Y | Y | Y | 62 | Thin 80-WLCSP |
| CY8C6247FDI-D52T | 150/50 | 100/25 | 1024 | 288 | 2 | 12 | Y | Y | Y | 62 | 80-WLCSP |
| CY8C6247BTI-D54 | 150/50 | 100/25 | 1024 | 288 | 2 | 12 | Y | Y | Y | 100 | Thin 124-BGA |
| CY8C6247BTI-D54T | | | | | | | | | | | |
| CY8C6246BTI-D54 | 150/50 | 100/25 | 512 | 128 | 2 | 12 | Y | Y | Y | 100 | Thin 124-BGA |
| CY8C6246BTI-D54T | | | | | | | | | | | |

Base features (available in all the part numbers):

- CPU Subsystem: Arm® Cortex®-M4F (CM4) and Arm® Cortex®-M0+ (CM0+), 2x DMA Controllers
- SCBs: 1x Deep-Sleep SCB (I2C/SPI) , 8x SCB (I2C/SPI/UART)[2]
- Analog:2x Low-Power Comparators, 1x 12-bit DAC, 1x 12-bit SAR ADC
- Digital: 1x Quad-SPI Memory I/F, 32x TCPWMs[2]
- Audio: 1x I2S interface, 2x PDM channels
- Others: 1x USB Full-speed, Segment LCD Drive, 1x SIMO DC-DC Buck Converter

1) The tape and reel field in the part number (part numbers ending with the letter 'T') is only used for ordering purposes. This field is not included in the MPN database used for firmware development.
2) The number of instances of a peripheral, like SCB (I2C/SPI/UART), or like TCPWM, for example, will be limited by the number of GPIOs supported by the package. Please use the ModusToolbox™ software device configuration tools to find the package specific availability of peripherals like SCB and TCPWM.

## 7.1 PSOC™ 6 MPN decoder

**CY XX 6 A B C DD E - FF G H I JJ K L**

| Field | Description | Values | Meaning |
|---|---|---|---|
| CY | Cypress | CY | Cypress - An Infineon Technologies company |
| XX | Firmware | 8C | Standard |
| | | B0 | “Secure Boot” v1 |
| | | S0 | “Standard Secure” - AWS |
| 6 | Architecture | 6 | PSOC™ 6 |
| A | Line | 0 | Value |
| | | 1 | Programmable |
| | | 2 | Performance |
| | | 3 | Connectivity |
| | | 4 | Secured |
| B | Speed | 2 | 100 MHz |
| | | 3 | 150 MHz |
| | | 4 | 150/50 MHz |
| C | Memory size (Flash/SRAM) | 0-3 | Reserved |
| | | 4 | 256K/128K |
| | | 5 | 512K/256K |
| | | 6 | 512K/128K |
| | | 7 | 1024K/288K |
| | | 8 | 1024K/512K |
| | | 9 | Reserved |
| | | A | 2048K/1024K |
| DD | Package | AZ, AX | TQFP |
| | | LQ | QFN |
| | | BZ, BT | BGA |
| | | FM | M-CSP |
| | | FN, FD, FT | WLCSP |
| E | Temperature range | C | Consumer |
| | | I | Industrial |
| | | Q | Extended Industrial |
| FF | Feature code | | Cypress internal |
| | | S2-S6 | |
| | | BL | Integrated Bluetooth® LE |
| G | CPU core | F | Single core |

## 7 Ordering information

| Field | Description | Values | Meaning |
|---|---|---|---|
| | | D | Dual core |
| H | Attributes code | 0-9 | Feature set |
| I | GPIO count | 1 | 31-50 |
| | | 2 | 51-70 |
| | | 3 | 71-90 |
| | | 4 | 91-110 |
| JJ | Engineering sample (optional) | ES | Engineering samples or not |
| K | Die Revision (optional) | | Base |
| | | A1-A9 | Die revision |
| L | Tape/Reel Shipment (optional) | T | Tape and Reel shipment |

# 8 Packaging

This product line is offered in two different dimensions of 124-BGA[4] and two different dimensions of 80-ball WLCSP packages[4].

**Table 59 Package dimensions**

| Spec ID# | Package | Description | Package drawing number |
|---|---|---|---|
| PKG_1 | 124-BGA | 124-BGA, 9 mm × 9 mm × 1 mm height with 0.65-mm pitch | 001-97718 |
| PKG_2 | 80-WLCSP | 80-WLCSP, 3.7 mm × 3.2 mm × 0.43 mm height with 0.35-mm pitch | 002-20310 |
| PKG_3 | Thin 80-WLCSP | Thin 80 -WLCSP, 3.7 mm × 3.3 mm × 0.33 mm height with 0.35-mm pitch | 002-23411 |
| PKG_4 | Thin 124-BGA | Thin 124-BGA, 7 mm × 7 mm × 0.8 mm height with 0.5-mm pitch | 002-38770 |

**Table 60 Package characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | – | –40 | 25 | 85 | °C |
| $T_J$ | Operating junction temperature | – | –40 | – | 100 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ (124-BGA) | – | – | 36.2 | – | °C/W |
| $T_{JC}$ | Package $\theta_{JC}$ (124-BGA) | – | – | 15 | – | °C/W |
| $T_{JA}$ | Package $\theta_{JA}$ (thin 124-BGA) | – | – | 58 | – | °C/W |
| $T_{JC}$ | Package $\theta_{JC}$ (thin 124-BGA) | – | – | 19 | – | °C/W |
| $T_{JA}$ | Package $\theta_{JA}$ (80-WLCSP) | – | – | 20.4 | – | °C/W |
| $T_{JC}$ | Package $\theta_{JC}$ (80-WLCSP) | – | – | 0.2 | – | °C/W |
| $T_{JA}$ | Package $\theta_{JA}$ (Thin 80-WLCSP) | – | – | 20.4 | – | °C/W |
| $T_{JC}$ | Package $\theta_{JC}$ (Thin 80-WLCSP) | – | – | 0.2 | – | °C/W |

**Table 61 Solder reflow peak temperature**

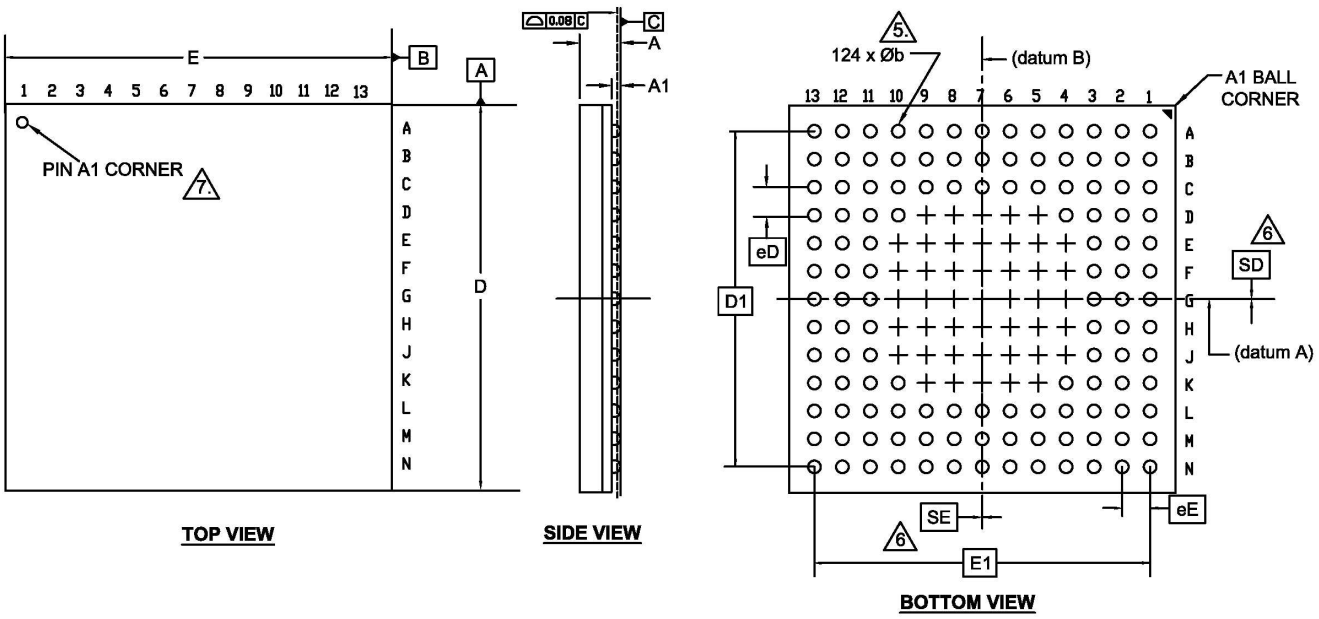
| Package | Maximum peak temperature | Maximum time at peak temperature |
|---|---|---|
| All | 260°C | 30 seconds |

**Table 62 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---|---|
| 124-BGA packages | MSL 3 |
| 80-WLCSP packages | MSL 1 |

[4] The thin 124-BGA package is in the process of qualification; the rest of the packages are production-qualified

## 8 Packaging




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.16 | 0.21 | 0.26 |
| D | 8.90 | 9.00 | 9.10 |
| E | 8.90 | 9.00 | 9.10 |
| D1 | | 7.80 BSC | |
| E1 | | 7.80 BSC | |
| MD | | 13 | |
| ME | | 13 | |
| N | | 124 | |
| Ø b | 0.25 | 0.30 | 0.35 |
| eD | | 0.65 BSC | |
| eE | | 0.65 BSC | |
| SD | | 0 | |
| SE | | 0 | |

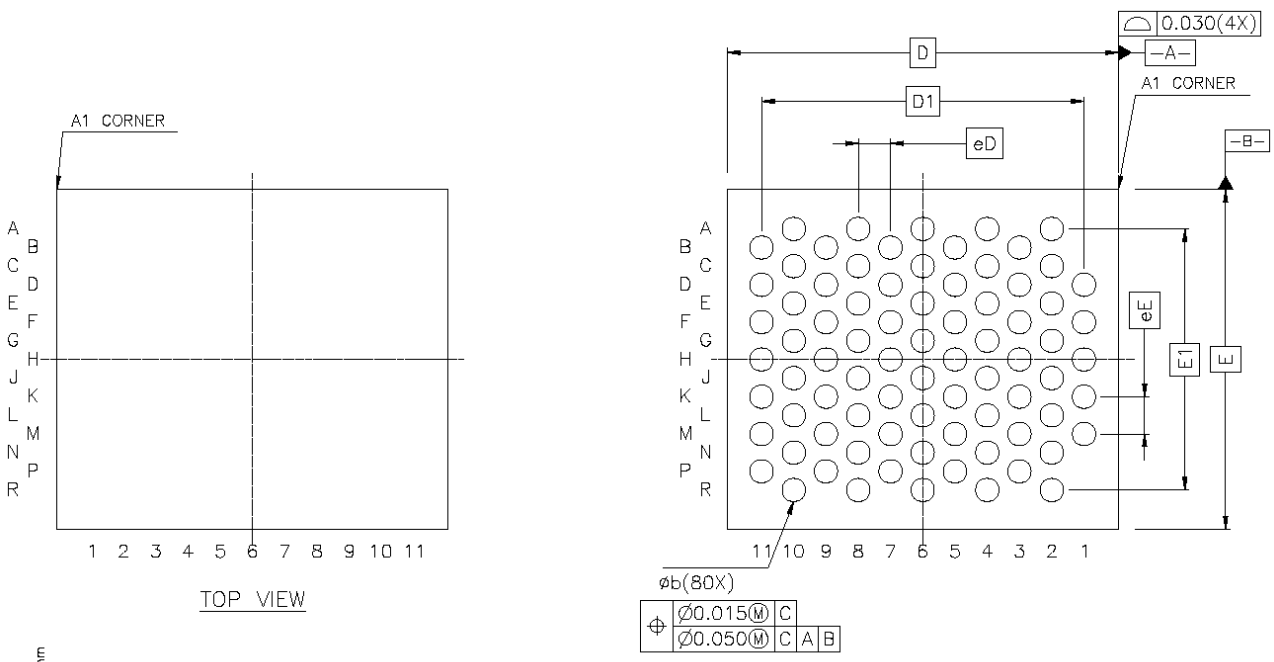
NOTES:

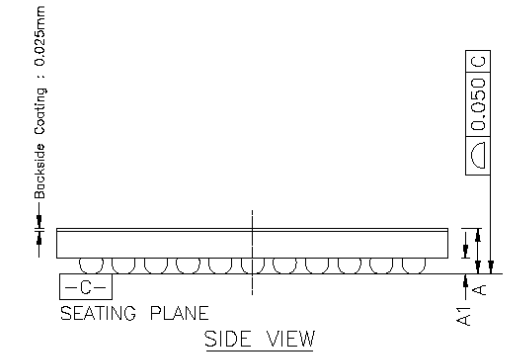
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-280.

001-97718 *B

**Figure 19 124-BGA 9.0 × 9.0 ×1.0 mm (PG-VFBGA-124-800)**

## 8 Packaging




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.387 | 0.427 | 0.467 |
| A1 | 0.122 | — | 0.182 |
| D | 3.676 BSC | | |
| E | 3.190 BSC | | |
| D1 | 3.031 BSC | | |
| E1 | 2.450 BSC | | |
| n | 80 | | |
| Øb | 0.188 | 0.218 | 0.248 |
| eD | 0.303 BSC | | |
| eE | 0.350 BSC | | |

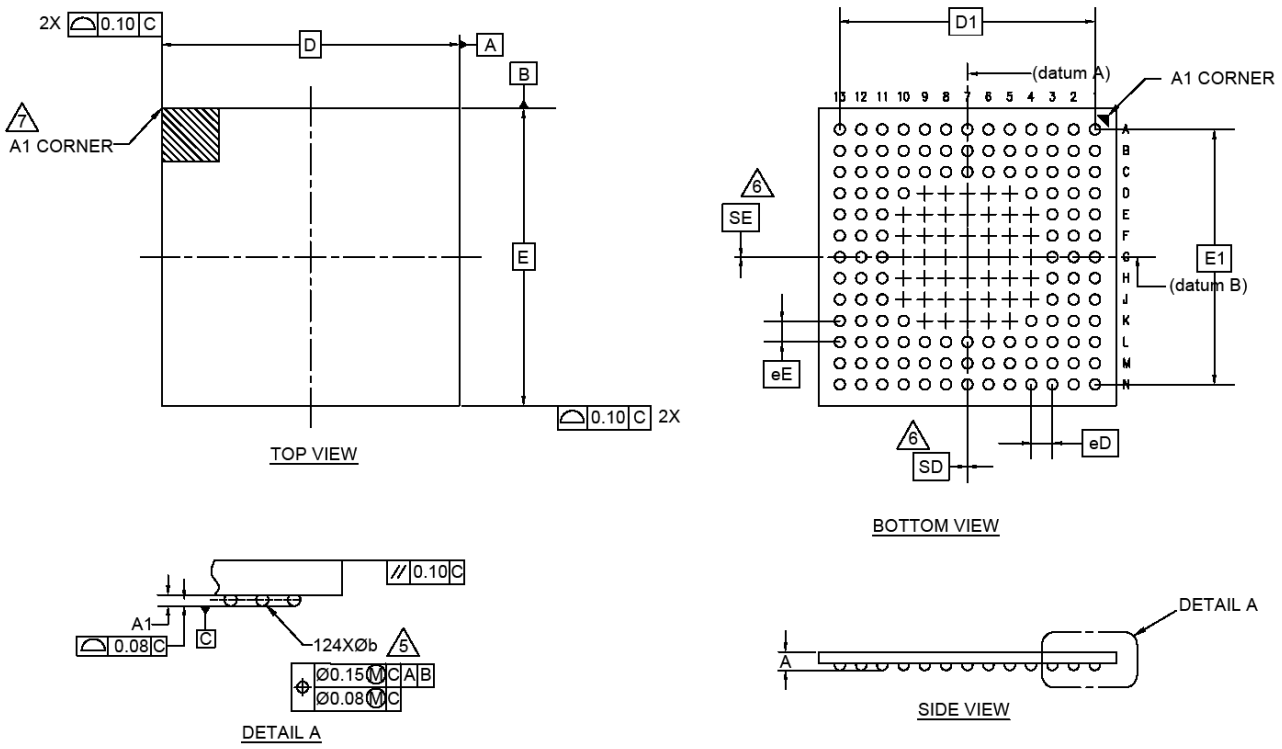
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

002-20310 Rev. *A

**Figure 20 80-ball WLCSP 3.676 × 3.190 × 0.467 mm FN80B, package outline (SG-XFWLB-80)**

## 8 Packaging




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 0.80 |
| A1 | 0.11 | - | - |
| D | 7.00 BSC | | |
| E | 7.00 BSC | | |
| D1 | 6.00 BSC | | |
| E1 | 6.00 BSC | | |
| MD | 13 | | |
| ME | 13 | | |
| N | 124 | | |
| Ø b | 0.20 | 0.25 | 0.30 |
| eD | 0.50 BSC | | |
| eE | 0.50 BSC | | |
| SD | 0.00 | | |
| SE | 0.00 | | |

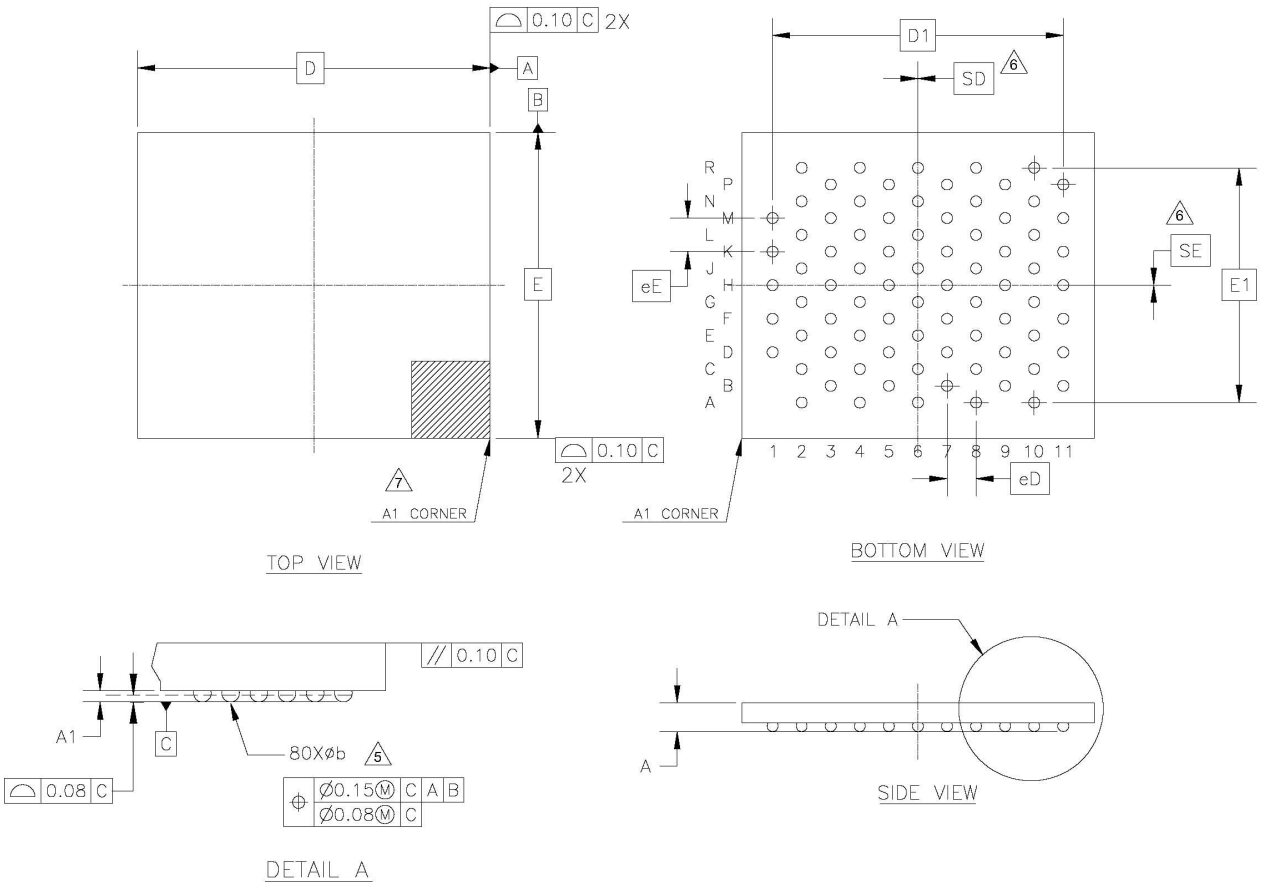
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A

002-38770 Rev. **

**Figure 21 124-ball FBGA 7 × 7 ×0.8 mm BZ124A, package outline (PG-WFBGA-124)**

## 8 Packaging




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 0.33 |
| A1 | 0.081 | - | - |
| D | 3.676 BSC | | |
| E | 3.190 BSC | | |
| D1 | 3.031 BSC | | |
| E1 | 2.450 BSC | | |
| MD | 11 | | |
| ME | 15 | | |
| N | 80 | | |
| Øb | 0.1035 | 0.1150 | 0.1265 |
| eD | 0.303 BSC | | |
| eE | 0.350 BSC | | |
| SD | 0.00 BSC | | |
| SE | 0.00 BSC | | |

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. JEDEC SPECIFICATION NO. REF. : N/A

002-23411 **

**Figure 22 80-ball WLCSP 3.676 × 3.190 × 0.33 mm FL80A, package outline (SG-XFWLB-80)**

# 9 Acronyms

| Acronym | Description |
|---|---|
| 3DES | triple DES (data encryption standard) |
| ADC | analog-to-digital converter |
| AES | advanced encryption standard |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus |
| AMUX | analog multiplexer |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| Arm® | advanced RISC machine, a CPU architecture |
| BGA | ball grid array |
| BOD | brown-out detect |
| CAD | computer aided design |
| CCO | current controlled oscillator |
| CM0+ | Cortex®-M0+, an Arm® CPU |
| CM4 | Cortex®-M4, an Arm® CPU |
| CMAC | cipher-based message authentication code |
| CMOS | complementary metal-oxide-semiconductor, a process technology for IC fabrication |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| CSD | Capacitive Sigma-Delta |
| CSX | Mutual capacitance sensing method. See also CSD |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DAP | debug access port |
| DES | data encryption standard |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DSI | digital system interconnect |
| DU | data unit |
| ECC | elliptic curve cryptography |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| ETM | embedded trace macrocell |

## 9 Acronyms

| Acronym | Description |
|---|---|
| FIFO | first-in, first-out |
| FLL | frequency locked loop |
| FPU | floating-point unit |
| FS | full-speed |
| GND | Ground |
| GPIO | general-purpose input/output, applies to a PSOC™ pin |
| HMAC | Hash-based message authentication code |
| HSIOM | high-speed I/O matrix |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| $I^2C$, or IIC | Inter-Integrated Circuit, a communications protocol |
| $I^2S$ | inter-IC sound |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| IoT | internet of things |
| IPC | inter-processor communication |
| IRQ | interrupt request |
| ISR | interrupt service routine |
| JTAG | Joint Test Action Group |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol |
| LP | low power |
| LS | low-speed |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| M-CSP | molded chip scale package |
| MCU | microcontroller unit |
| MCWDT | multi-counter watchdog timer |
| MISO | master-in slave-out |
| MMIO | memory-mapped input output |

## 9 Acronyms

| Acronym | Description |
|---|---|
| MOSI | master-out slave-in |
| MPU | memory protection unit |
| MSL | moisture sensitivity level |
| Msps | million samples per second |
| MTB | micro trace buffer |
| MUL | multiplier |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NVIC | nested vectored interrupt controller |
| OTP | one-time programmable |
| OVT | overvoltage tolerant |
| PASS | programmable analog subsystem |
| PCB | printed circuit board |
| PCM | pulse code modulation |
| PDM | pulse density modulation |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLL | phase-locked loop |
| PMIC | power management integrated circuit |
| POR | power-on reset |
| PPU | peripheral protection unit |
| PRNG | pseudo random number generator |
| PSOC™ | Programmable system on chip |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| QD | quadrature decoder |
| QSPI | quad serial peripheral interface |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| ROM | read-only memory |
| RSA | Rivest–Shamir–Adleman, a public-key cryptography algorithm |
| RTC | real-time clock |
| RX | receive |
| S/H | sample and hold |

## 9 Acronyms

| Acronym | Description |
|---|---|
| SAR | successive approximation register |
| SARMUX | SAR ADC multiplexer bus |
| SCB | serial communication block |
| SFlash | supervisory flash |
| SHA | secure hash algorithm |
| SINAD | signal to noise and distortion ratio |
| SNR | signal-to-noise ration |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SRAM | static random access memory |
| SROM | supervisory read-only memory |
| SRSS | system resources subsystem |
| SWD | serial wire debug, a test protocol |
| SWJ | serial wire JTAG |
| SWO | single wire output |
| SWV | serial-wire viewer |
| TCPWM | timer, counter, pulse-width modulator |
| TDM | time division multiplexed |
| TQFP | thin quad flat package |
| TRM | technical reference manual |
| TRNG | true random number generator |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| ULP | ultra-low power |
| USB | Universal Serial Bus |
| WCO | watch crystal oscillator |
| WDT | watchdog timer |
| WIC | wakeup interrupt controller |
| WLCSP | wafer level chip scale package |
| XIP | execute-in-place |
| XRES | external reset input pin |

# 10 Document conventions

## 10.1 Units of measure

**Table 63 Units of measure**

| Symbol | Units of measure |
|---|---|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| µA | microampere |
| µF | microfarad |
| µH | microhenry |
| µs | microsecond |
| µV | microvolt |
| µW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |

**(table continues...)**

**Table 63 (continued) Units of measure**

| Symbol | Units of measure |
|---|---|
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

# 11 Errata

This section describes the errata for the CY8C62x6, CY8C62x7 devices in the PSOC™ 62 MCU line. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

For more details, contact Infineon support.

**Table 64 Part numbers affected**

| Part number | Device characteristics |
|---|---|
| CY8C62x6, CY8C62x7 devices | All |

### Qualification status

Product status: In Production – Qual. Report QTP 174005.

### Errata summary

This table defines the errata applicability to CY8C62x6, CY8C62x7 devices in the PSOC™ 62 MCU line.

***Note**: Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.*

| Items | Part number | Silicon revision | Fix status |
|---|---|---|---|
| Table 65 | All | B3 (Major/Minor Die Revision ID: 2/4) with Flash boot revision 1.20.1.45 | Flash boot version 1.20.1.53 resolves the issue |

**Table 65 Boot lock-up**

| | |
|---|---|
| Problem definition | In extremely rare circumstances, on the order of once every 10,000 -100,000+ reset or power cyceles, during boot the device may enter an infinte fault handler loop (never reaches application code). |
| Parameters affected | Device may not transition from boot to application code |
| Trigger condition(s) | Only occurs if TOC2 (table of contents #2) is instantiated in Sflash by user. TOC2 is used for secure lifecycle stage or to alter boot-time defaults in normal lifecycle stage. |
| Scope of impact | Device may not transition from boot to application code |
| Workaround | Reset or power cycle the device |
| Fix status | Flashboot revision 1.20.1.53 resolves the issue. Note that flashboot cannot be field-udapted. Flashboot 1.20.1.53 is deployed beginning with date code 2619 |

# Revision history

| Document revision | Date of release | Description of changes |
|---|---|---|
| *B | 2017-09-27 | External posting: Publish to web.<br>Internal posting: Released to web for PSOC™ 62. |
| *C | 2017-11-03 | Corrected typo in Development Support. |
| *D | 2017-11-29 | Updated Table 5.<br>Updated SID84 description and conditions.<br>Updated Table 13.<br>Updated max value for SID223.<br>Updated min and max values of SID432R.<br>Updated Table 39.<br>Updated Units of Measure. |
| *E | 2018-02-10 | Updated Active CPU power consumption in 32-bit Dual Core CPU Subsystem.<br>Updated Table 5, Table 6, Table 16, Table 21, Table 32, and Table 35.<br>Updated min value for SID4B and SID291.<br>Updated Fixed UART AC specifications.<br>Updated SID190 and removed SID194.<br>Removed SID226.<br>Updated max value for SID234.<br>Updated Units of Measure. |
| *F | 2018-09-08 | Removed Preliminary document status.<br>Corrected units usage throughout the document.<br>Added note explaining Fc for the SID.TCPWM.4 parameter.<br>Updated Features, CPU, Flash, One-Time-Programmable (OTP) eFuse ILO Clock Source, Watchdog Timer (WDT), Serial Communication Blocks (SCB), Ordering Information, Packaging.<br>Added Resource Protection.<br>Removed Errata section.<br>Updated package diagram (spec 001-97718 *A to *B) in Packaging.<br>Updated Figure 2.<br>Added a note in Table 2.<br>Updated Table 5, through Table 8, Table 12, Table 15, Table 18, Table 28, Table 30, Table 36, and Table 38. |
| *G | 2019-09-20 | Updated the title.<br>Updated Ordering Information and Packaging.<br>Added UDB in Acronyms. |
| *H | 2019-12-20 | Updated Features.<br>Updated Blocks and functionality and Functional Description.<br>Updated Pinouts and Power supply considerations. |

## Revision history

| Document revision | Date of release | Description of changes |
|---|---|---|
| *I | 2020-03-31 | Updated Features.<br>Updated Functional Description.<br>Updated Pinouts.<br>Updated PSOC™ 6 MPN Decoder. |
| *J | 2020-06-22 | Updated Development ecosystem, GPIO, and LCD sections.<br>Added External Crystal Oscillators.<br>Updated Errata. |
| *K | 2020-11-09 | Updated Flexible clocking options, Block Diagram, CPUs, Clock system, and SID431.<br>Updated Universal digital blocks (UDBs), UDB Port Adapter Specifications Conditions.<br>Added InterProcessor Communication (IPC).<br>Updated diagram.<br>Updated the XRES bullet in Reset, updated SID15 Description and Conditions, and Power-on reset specifications table.<br>Updated ModusToolbox™ software. Updated Clocking diagram. Updated Power supply considerations<br>Added footnote to TMCLK_SOC specs.<br>Updated Opamp specifications.<br>Updated SID7A conditions, SID7D description, and SID8 conditions.<br>Added spec SID468 - SID474, and SID468A - SID474A.<br>Updated Audio Spec SID408.<br>Updated Ordering information.<br>Integrated ECO erratum into External Crystal Oscillators.<br>Added ECO usage guidelines table. |
| *L | 2021-02-26 | Added Table 12 and Figure.<br>Updated conditions for SID316 and updated description of SID319.<br>Updated conditions for SID316 and updated description of SID319.<br>Changed BLE references to Bluetooth® LE.<br>Updated Security terminology to Infineon standards.<br>Removed the Errata section; incorporated errata into the GPIO, ADC, and CAPSENSE™ sections. |
| *M | 2021-06-30 | Added opamp graphs (Figure 17 and Figure 18).<br>Corrected typo in Figure 12 and Figure 14. |
| *N | 2021-12-14 | Added note regarding unused USB pins in USB Full-Speed device interface, Power supply considerations, and Pinouts.<br>Updated SIDC1 description.<br>Updated Figure and added related footnote.<br>Updated details/conditions for SID7A.<br>Updated SID325U, SID328, and SID329 description. |

## Revision history

| Document revision | Date of release | Description of changes |
|---|---|---|
| *O | 2022-10-31 | Added device identification and revision information in Features.<br>Added spec SID415 and SID304P.<br>Added footnote "Guaranteed by design, not production tested" for specs SID402 - SID412.<br>Updated Clock system and PLL specifications.<br>Updated Protection units. |
| *P | 2023-06-07 | Migrated to Infineon template.<br>Added notes for ModusToolbox™ and PSOC™ Creator in the Development ecosystem section.<br>Updated WLCSP package MPNs in ordering information. |
| *Q | 2023-12-13 | Added thin 124-BGA package information.<br>Updated web hyperlinks. |
| *R | 2026-06-19 | Template update.<br>Updated footnote numbers.<br>PSOC™ 6 MCU resources<br>ModusToolbox™ software<br>CAPSENSE™ subsystem<br>Updated Features<br>Updated USB Full-Speed device/host Interface<br>Added Errata |
| *S | 2026-09-17 | Updated PSOC™ 6 MCU resources<br>Updated Functional description<br>Updated Table 10<br>Updated Power supply considerations<br>Updated Ordering information<br>Updated Table 58 |

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