NA2200

5V Analog Front End with High Gain PGA

FEATURES

- Supply Voltage +2.7V to +5.5V
- Ambient Operating Temperature -40°C to 125°C
- ADC Resolution 16-Bit (No missing codes)
- Data Rate 0.814k to 6.51ksps(1)
- Input mode Differential : 2 inputs
  Single-ended (2) : 4inputs
  Pseudo-differential (3)
- PGA 1V/V to 512V/V
- System Calibration for offset & gain drift
- Built-in Regulator
- Current Consumption Normal Mode 4mA
  Low Power Mode 1.3mA
- Conversion mode Single / Continuous
- Excitation Current Source
  2 systems (0.1mA, 0.25mA, 0.5mA, 1.0mA)
- Interface SPI
- CS (Chip Select)
- Error detection CRC8, Check Sum
- Package SSOP-16-BD

GENERAL DESCRIPTION

NA2200 is a CMOS-based 5V AFE with up to 512 times internal PGA (Programmable Gain Amplifier). Internal 16-bit ΔΣ type Analog to Digital converter (ADC) can perform conversion rates from 0.814ksps to 6.51ksps.
The customer can choose internal Analog to Digital converter's input, among differential input, single-ended input and pseudo-differential input.

NA2200 can set the optimum gain to the pressure sensor, flow sensor by a wide range of gain setting. Various parameters (such as gain, conversion rate, correction) settings can be easily set in the SPI communication from an external MCU.

APPLICATIONS

- Pressure sensors
- Flowmeters
- Current Measurement
- Thermostat
- PLC



SSOP-16-BD
5.0 × 6.4 × 1.15(mm)

(1) Case of single conversion. (Continuous conversion is three times the data rate.)
(2) PGA2 can be used only. (PGA1 cannot be used.) Four channels of VIN1P, VIN1N, VIN2P & VIN2N can be used.
(3) Bias voltage of VIN1P, VIN1N, VIN2P & VIN2N is common to VDD / 2. Input Signal can be used VIN1P and VIN2P only.

■ PRODUCT NAME INFORMATION

NA2200 BD A E2 S

Description of configuration

Suffix	Item	Description
BD	Package code	Indicates the package. Refer to the order information.
A	Version	Product Version. Default is A.
E2	Packing	Refer to the packing specifications.
S	Grade	Standard ; Indicates the quality grade.

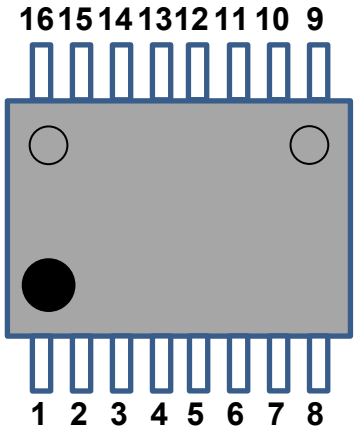
Grade

Grade	Usage	Operating Temperature Range	Test Temperature
S	General-purpose and Consumer application	−40°C to 125°C	25°C

■ ORDER INFORMATION

Product Name	Package	RoHS	Halogen-Free	Terminal Finish	Weight (mg)	Quantity (pcs/reel)
NA2200BDAE2S	SSOP-16-BD	Yes	Yes	Sn-2Bi	68	2,000

■ PIN DESCRIPTION



SSOP-16-BD Pin Configuration

Pin No.	Pin Name	I/O	Description
1	VIN1P	Analog Input	+INPUT 1 for differential mode / INPUT 1 for single-ended mode
2	VIN1N	Analog Input	-INPUT 1 for differential mode / INPUT 2 for single-ended mode
3	VIN2P	Analog Input	+INPUT 2 for differential mode / INPUT 3 for single-ended mode
4	VIN2N	Analog Input	-INPUT 2 for differential mode / INPUT 4 for single-ended mode
5	VREFN	Analog Input	-Reference Voltage Input
6	VREFP	Analog Input	+Reference Voltage Input
7	STBY	Digital Input	Standby Mode
8	VDD	Power Supply	Supply Voltage
9	GND	GND	GND
10	GND	GND	GND
11	REG	Analog Output	Built-in Regulator for Digital Power Supply (Place a decoupling capacitor close to 11pin)
12	CSB	Digital Input	SPI Chip Select
13	SDO / RDYB	Digital Output	SPI serial data output / RDYB output
14	SDI	Digital Input	SPI serial data input
15	SCK	Digital Input	SPI serial clock input
16	NC	GND	Non Connection (*)

(*)It is recommended to be left open or connected to GND.

Please refer to “TYPICAL APPLICATION CIRCUIT“ or “APPLICATION NOTES“ for details.

■ ABSOLUTE MAXIMUM RATINGS

	Symbol	Ratings	Unit
Power Supply Voltage	VDD_{abso}	7.0 (4)	V
Power Dissipation	P_D	900 (5) / 1,300 (6)	mW
Analog Input Voltage	V_{IN}	-0.3 to (VDD+0.3) (7)	V
Operating Temperature Range	T_{opr}	−40 to 125	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C

(4) The difference between the absolute maximum power supply voltage and the operating power supply voltage is small. Please be careful so that the operating power supply voltage does not exceed the absolute maximum supply voltage by spike voltage.
(5) Mounted on glass epoxy board.
(114.3 x 76.2 x 1.57mm: based on EIA/JEDEC standard, 2Layers FR-4.)
(6) Mounted on glass epoxy board.
(114.3 x 76.2 x 1.6mm: based on EIA/JEDEC standard, 4Layers FR-4.)
(7) Input pin is connected to the clamp diode to the power supply pin. When the input signal exceeds the supply rails 0.3V or more (below the GND rail 0.3V or more), the input current must be limited to less than 10mA.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

■ ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Analog Input)

Unless otherwise specified, all limits ensured for T_a = +25°C, VDD = 5.0V, GND = 0V, VREFP = 0.5 x VDD, VREFN = 0V, PGAIN1 = PGAIN2 = 1, VCIN2 = 0.5 x VDD, DR = 0.814ksps or 1.63ksps

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Analog Input 1 (PGA1 = unused, PGA2 = used, PGAIN2 = 1 or 4)						
Differential Input Voltage Range 1	VDIN1		-	±VREF / (PGAIN2)	-	V
Common Mode Input Voltage Range 1	VCIN1		GND	-	VDD	V
Input Impedance 1	ZIN1	FMOD = 1.25MHz PGAIN2 = 1	-	600	-	kΩ
		FMOD = 1.25MHz PGAIN2 = 4	-	300	-	kΩ
Common Mode Rejection Ratio 1	CMRR1	PGAIN2 = 1	70	90	-	dB
Analog Input 2 (PGA1, 2 = used, PGAIN1 = 1 or 2 or 4 or 8 or 16 or 32 or 64 or 128, PGAIN2=1 or 4)						
Differential Input Voltage Range 2	VDIN2	PGAIN1 ≥ 2	-	(±VREF) / (PGAIN1 x PGAIN2)	-	V
Common Mode Input Voltage Range 2	VCIN2		0.1	-	VDD -1.2	V
Input Impedance 2	ZIN2		-	100	-	MΩ
Common Mode Rejection Ratio 2	CMRR2	PGAIN1 = 2 PGAIN2 = 1 CHOP = ON	70	90	-	dB

ELECTRICAL CHARACTERISTICS (Reference Voltage Input)

Unless otherwise specified, all limits ensured for T_a = +25°C, VDD = 5.0V, GND = 0V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Reference Voltage	VREF	VREF = VREFP - VREFN	2.0	-	VDD	V
VREFN Input Voltage Range	VREFN		0	-	VDD -2.5	V
Input Impedance 3	ZIN3	FMOD = 1.25MHz PGAIN2 = 1	-	180	-	kΩ
		FMOD = 1.25MHz PGAIN2 = 4	-	250	-	kΩ

ELECTRICAL CHARACTERISTICS (Internal Regulator)

Unless otherwise specified, all limits ensured for T_a = +25°C, VDD = 5.0V, GND = 0V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output Voltage	REG		2.376	2.4	2.424	V
Temperature Drift	REG_TD	Ta = 25 to 125℃ (REG125–REG25) / REG25 x 10 ^ 6 / (125 -25) (8)	-	-25	-	ppm/℃

(8) REG25 -> Measured value at 25℃. REG125 -> Measured value at 125℃.

ELECTRICAL CHARACTERISTICS (Internal Oscillator)

Unless otherwise specified, all limits ensured for T_a = +25°C, VDD = 5.0V, GND = 0V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OSC Frequency	FOSC		2.25	2.5	2.75	MHz

ELECTRICAL CHARACTERISTICS (Excitation Current Source)

Unless otherwise specified, all limits ensured for T_a = +25°C, VDD = 5.0V, GND = 0V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output Current	IEX	VINxx = 1.2V	-	0.10, 0.25, 0.50, 1.00	-	mA
Absolute Value Deviation	IEX_E	(Measured Value – IEX) / IEX x 100	-	-	±10	%
Matching Error	IEX_ME	IEX1 = 1mA, (IEX2 - IEX1) / IEX1 x 100 (9)	-	-	±1	%
Temperature Drift	IEX_TD	Ta = 25 to 125℃ (IEX125 - IEX25) / IEX125 x 10 ^ 6 / (125 - 25) (10)	-	-300	-	ppm/℃
Temperature Drift Matching Error	IEX_TD_ME	IEX2_TD - IEX1_TD (11)	-	±2	-	ppm/℃

(9) IEX1 -> Measured value of Excitation current source 1.
IEX2 -> Measured value of Excitation current source 2.
(10) IEX25 -> Measured value at 25℃.
IEX125 -> Measured value at 125℃.
(11) IEX1_TD -> Temperature Drift of Excitation current source 1.
IEX2_TD -> Temperature Drift of Excitation current source 2.

ELECTRICAL CHARACTERISTICS (Programmable Gain Amplifier)

Unless otherwise specified, all limits ensured for T_a = +25°C, VDD = 5.0V, GND = 0V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PGA1 Gain	PGAIN1		-	1, 2, 4, 8, 16, 32, 64, 128,	-	V/V
PGA2 Gain	PGAIN2		-	1, 4	-	V/V

ELECTRICAL CHARACTERISTICS (Analog to Digital Convertor)

Unless otherwise specified, all limits ensured for T_a = +25°C, VDD = 5.0V, GND = 0V, VREFP = 0.5 x VDD, VREFN = 0V, PGAIN1 = PGAIN2 = 1, VCIN2 = 0.5 x VDD

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	N	No missing codes(12)	16			Bit
Data Rate	DR	Single Conversion(13) Normal Mode	0.814k, 1.63k, 3.26k, 6.51k			sps
		Single Conversion(13) Low Power Mode	0.203k, 0.407k, 0.814k, 1.63k			
Clock Frequency	FMOD (MDCK)	FMOD = FOSC / 2	1.125	1.25	1.375	MHz
Integral Non Linearity	INL	best-fit-line method(14) VREFP = 5.0V PGAIN1 = 2	-	±30	±60	ppm
Offset Error	OE	PGAIN1 = 128 CHOP = OFF	-	±150	-	µV
		PGAIN1 = 128 CHOP = ON	-	±1	±10	µV
Gain Error	GE	PGAIN1 = 128 PGAIN2 = 1	-	±0.5	±2.0	%
Noise Free Bit(12)(15)(16)	NFB	VDIN2 = 0V VREFP = 5.0V VREFN = 0V DR = 0.814ksps	-	15	-	Bit
		VDIN2 = 0V VREFP = 5.0V VREFN = 0V DR = 1.63ksps	-	14	-	Bit

(12) This parameter is not production tested.
(13) There is no latency by one settling behavior.
(14) Guaranteed by design evaluation and several points test
(15) See table of Effective resolution and Noise Free Bit(NFB) (see page 25 to 26).
(16) NFB represents the ADC output code variations 6.6σ with the differential input shorted.

ELECTRICAL CHARACTERISTICS (Power Supply / Supply Current)

Unless otherwise specified, all limits ensured for T_a = +25°C, VDD = 5.0V, GND = 0V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	VDD		2.7	5.0	5.5	V
Supply Current Normal Mode	IDD	PGA OFF	1.4	2.3	3.3	mA
		PGA ON	2.7	4.0	5.7	mA
Supply Current Low Power Mode	IDD_{LOW}	PGA OFF	0.6	0.9	1.4	mA
		PGA ON	0.85	1.3	1.9	mA
Supply Current Sleep Mode	IDD_{SLEEP}	Sleep Mode	0.14	0.27	0.4	mA
Supply Current Standby Mode	IDD_{STBY}	Standby Mode STBY = VDD Regulator OFF	-	0.001	0.1	µA

ELECTRICAL CHARACTERISTICS (Digital I/Os)

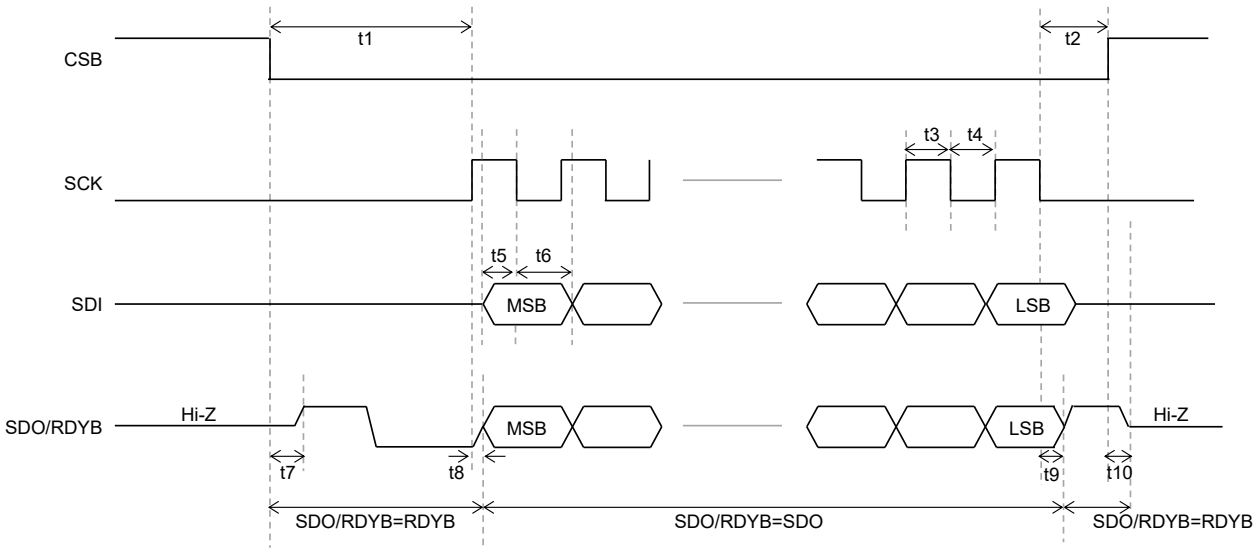
Unless otherwise specified, all limits ensured for T_a = +25°C, VDD = 5.0V, GND = 0V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{ih}		0.7 x VDD	-	-	V
Low-level input voltage	V_{il}		-	-	0.2 x VDD	V
High-level output voltage	V_{oh}	I_{oh} max.= 6mA	0.8 x VDD	-	-	V
Low-level output voltage	V_{ol}	I_{ol} max.= 6mA	-	-	0.4	V

ELECTRICAL CHARACTERISTICS (Serial Peripheral Interface)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
SPI clock frequency	f_{sck}	-	-	10	MHz
Setup time, CSB falling edge to first SCK rising edge	t1	45	-	-	nsec
Hold time, final SCK falling edge to CSB rising edge	t2	45	-	-	nsec
Pulse duration, SCK high	t3	45	-	-	nsec
Pulse duration, SCK low	t4	45	-	-	nsec
Setup time, SDI input data valid before SCK falling edge	t5	10	-	-	nsec
Hold time, SDI input data valid after SCK falling edge	t6	10	-	-	nsec
Setup time, CSB falling edge to SDO / RDYB output data	t7	0	-	30	nsec
Setup time, SCK rising edge to SDO / RDYB output data	t8	0	-	40	nsec
Hold time, SCK falling edge of LSB to SDO / RDYB output data	t9	10	-	50	nsec
Setup time, CSB rising edge to SDO / RDYB changing to HiZ	t10	0	-	30	nsec
Reset time	t_{rstw}	-	-	400	nsec

- The SPI AC timing is shown in the figure below. It is the communication of 10Mbps at the highest speed.
- Capacitance Load of SDO / RDYB terminal is assumed to 40pF



SPI AC timing

■ REGISTER DESCRIPTION

NA2200 has register (list shown below) which can access it through SPI bus.
Registers with different data lengths (1 to 3 bytes) are assigned to 4-Bit register address.

Register Address	Register Name	Data Length [byte]
0x0	CTRL	2-Byte (16-Bit)
0x1	ADCDATA	2-Byte (16-Bit)
0x2	IEXCONF	2-Byte (16-Bit)
0x3	PGACONF	1-Byte (8-Bit)
0x4	CLKCONF	1-Byte (8-Bit)
0x5	Not used	-
0x6	OPTION0	1-Byte (8-Bit)
0x7	Not used	-
0x8	GAIN1	3-Byte (24-Bit)
0x9	GAIN2	3-Byte (24-Bit)
0xA	Not used	-
0xB	Not used	-
0xC	OFFSET1	3-Byte (24-Bit)
0xD	OFFSET2	3-Byte (24-Bit)
0xE	Not used	-
0xF	Not used	-

< View of the register table>

Register Name								
Bit	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Bit Name								
R / W								
Reset								

R / W: Bit of attribute (Read or Write)
- R (Read Only) : Read only
- W (Write Only) : Write only (At the time of read, return "0".)
- RW (Read Write) : Read & Write
- RC (Read / Write 1 to Clear bit) : Read returns the register value.
Writing 1 clears the bit to 0. Writing 0 does not affect the operation.

Reset: Reset value in register
Set to the reset value by SPI reset command and power-on reset.

■ REGISTER DESCRIPTION

CTRL Register

Register Address: 0x0

CTRL								
Bit	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
Bit Name	-	CHSELN			-	CHSELP		
R / W	-	RW			-	RW		
Reset	-	0x4			-	0x4		
Bit	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Bit Name	RDYCNT		RDYB	OV	MODE			
R / W	R		R	R	RW			
Reset	0x0		1	0	0x0			

Bit	Bit Name	Function
[15]	-	-
[14:12]	CHSELN	Analog input channel setting of negative side. Refer the below table: CHSELP / CHSELN Register.
[11]	-	-
[10:8]	CHSELP	Analog input channel setting of positive side. Refer the below table: CHSELP / CHSELN Register.
[7:6]	RDYCNT	Modulo operation counter. 2-Bit modulo operation counter that adds 1 each time the ADCDATA resister is updated.
[5]	RDYB	Data ready flag. When conversion data is updated, this bit is set to “0”. When ADCDATA read, this bit set to “1”. 0: Conversion completion 1: Conversion non-completion
[4]	OV	Overflow flag. When conversion data is overflow, this bit is set to “1”. When ADCDATA read, this bit is set to “0”. 0: Valid 1: Overflow (Invalid)
[3:0]	MODE	Operation mode setting. When this bit is “write”, sets the operation mode of ADC. When this bit is “read”, returns the current configuration state. Refer the below table : MODE Register

Table 1 CHSELP / CHSELN Bit

CHSELP	Positive
0x0	VIN1P
0x1	VIN1N
0x2	VIN2P
0x3	VIN2N
0x4	VREFN
0x5	VREFP
0x6	REG
0x7	GND

CHSELN	Negative
0x0	VIN1P
0x1	VIN1N
0x2	VIN2P
0x3	VIN2N
0x4	VREFN
0x5	VREFP
0x6	REG
0x7	GND

Table 2 MODE Bit

MODE	Operation	Processing
0x0	Idle	Waiting state of conversion operation or calibration
0x1	Sleep	Setting the state of low power consumption which conversion operation or calibration is available. Start-up time is inserted automatically before conversion operation.
0x2	Single conversion	Convert once the input channel that is selected in the CHSELP / N. After the conversion, the operation is “Idle (0x0)” state. Using the value of the “OFFSET1, 2” register.
0x3	Continuous conversion	Convert continuous the input channel that is selected in the CHSELP / N. Until the operation is set to "Idle (0x0)", conversion will continue. Using the value of the “OFFSET1, 2” register.
0x4	Single conversion + CHOP	This is the same as “Single conversion (0x2)”, but the data rate is 1/2. Not using the value of the “OFFSET1, 2” register.
0x5	Continuous conversion + CHOP	This is the same as “Continuous conversion (0x3)”, but the data rate is 1/3. Not using the value of the “OFFSET1, 2” register.
0x6	Single conversion + CHOP + IEX CHOP	This is the same as “Single conversion (0x2)”, but the data rate is 1/2. Not using the value of the “OFFSET1, 2” register. CHOP operation is valid. The connection channel of IEX1 and IEX2 is switched in conjunction with the CHOP operation.
0x7	Continuous conversion + CHOP + IEX CHOP	This is the same as “Continuous conversion (0x3)”, but the data rate is 1/3. Not using the value of the “OFFSET1, 2” register. CHOP operation is valid. The connection channel of IEX1 and IEX2 is switched in conjunction with the CHOP operation.
0x8	Not used(17)	-
0x9	Not used(17)	-
0xA	Not used(17)	-
0xB	Not used(17)	-
0xC	Calibration system offset	Input is selected by CHSELP / N, system offset is calibrated.
0xD	Calibration system gain	Input is selected by CHSELP / N, system gain is calibrated.
0xE	Not used(17)	-
0xF	Boot	Read only. It shows the state from the reset to change to “Idle (0x0)”. After the initial setting, automatically shifts to the "Idle (0x0)".

(17) Please do not absolutely use the “Not used” code. It will be the cause of failure.

ADCDATA Register

Register Address: 0x1

	ADCDATA															
Bit	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Bit Name	ADCDATA															
R / W	R															
Reset	-															

Bit	Bit Name	Function
[15:0]	ADCDATA	Store the converted data of the ADC.(18) Conversion data is expressed as a signed 16-bit. - When the input voltage is negative full-scale, the output is 0x8000 - When the input voltage is zero, the output is 0x0000 - When the input voltage is positive full-scale, the output is 0x7FFF. (in decimal -32768 to +32767)

(18) Relationship of conversion data ADCDATA and the analog input voltage V_{in} is as the following equation.
(It assumed that the offset error and gain error are zero.)

$$ADCDATA = \frac{V_{in}}{2 \times VREF} \times PGAIN1 \times PGAIN2 \times 2^{16} = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 2^{15}$$

IEXCONF Register

Register Address: 0x2

IEXCONF								
Bit	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
Bit Name	IEX2SLP	IEX2C			-	IEX2_EN	IEX2SEL	
R / W	RW	RW			-	RW	RW	
Reset	0	0x0			-	0	0x0	
Bit	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Bit Name	IEX1SLP	IEX1C			-	IEX1_EN	IEX1SEL	
R / W	RW	RW			-	RW	RW	
Reset	0	0x0			-	0	0x0	

Bit	Bit Name	Function
[15]	IEX2SLP	Condition setting of IEX2 at sleep mode by AUTOSLP bit = "1" of OPTION0 register. 0: IEX2 current depends on IEX2C 1: IEX2 OFF
[14:12]	IEX2C	Current setting of IEX2. 0x0: 0.10mA 0x1: 0.25mA 0x2: 0.50mA 0x3: 1.00mA 0x4 to 0x7: Not used(17).
[11]	-	-
[10]	IEX2_EN	Setting ON / OFF of IEX2. 0: IEX2 OFF (Open) 1: IEX2 ON
[9:8]	IEX2SEL	Connection setting of IEX2. 0x0: VIN1P 0x1: VIN1N 0x2: VIN2P 0x3: VIN2N

(17) Please do not absolutely use the "Not used" code. It will be the cause of failure.

Bit	Bit Name	Function
[7]	IEX1SLP	Condition setting of IEX1 at sleep mode by AUTOSLP bit = “1” of OPTION0 register. 0: IEX1 current depends on IEX1C 1: IEX1 OFF
[6:4]	IEX1C	Current setting of IEX1. 0x0: 0.10mA 0x1: 0.25mA 0x2: 0.50mA 0x3: 1.00mA 0x4 to 0x7: Not used(17).
[3]	-	-
[2]	IEX1_EN	Setting ON / OFF of IEX1. 0: IEX1 OFF (Open) 1: IEX1 ON
[1:0]	IEX1SEL	Connection setting of IEX1. 0x0: VIN1P 0x1: VIN1N 0x2: VIN2P 0x3: VIN2N

(17) Please do not absolutely use the “Not used” code. It will be the cause of failure.

PGACONF Register

Register Address: 0x3

PGACONF								
Bit	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Bit Name	-	-	PGA2GAIN	-	PGA1EN	PGA1GAIN		
R / W	-	-	RW	-	RW	RW		
Reset	-	-	0	-	0	0x0		

Bit	Bit Name	Function
[7:6]	-	-
[5]	PGA2GAIN	Gain setting of PGA2. 0: x1 1: x4
[4]	-	-
[3]	PGA1EN	Setting ON / OFF of PGA1. 0: PGA1 OFF 1: PGA1 ON
[2:0]	PGA1GAIN	Gain setting of PGA1. 0x0: x1 0x1: x2 0x2: x4 0x3: x8 0x4: x16 0x5: x32 0x6: x64 0x7: x128

CLKCONF Register

Register Address: 0x4

CLKCONF								
Bit	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Bit Name	-	-	CLKDIV		-	OSR		
R / W	-	-	RW		-	RW		
Reset	-	-	0x0		-	0x3		

Bit	Bit Name	Function
[7:6]	-	-
[5:4]	CLKDIV(19)	Setting of the ADC operating clock frequency (FMOD). FOSC is the operating clock of the internal OSC. 0x0: FOSC / 2 0x1: FOSC / 4 0x2: FOSC / 8 0x3: FOSC/ 16
[3]	-	-
[2:0]	OSR	Setting of the oversampling ratio of the digital filter 0x0: 64 0x1: 128 0x2: 256 0x3: 512 0x4 to 0x7: Not used(17)

(17) Please do not absolutely use the “Not used” code. It will be the cause of failure.
(19) Data rate is derived by the following equation. It will be the data rate of a single conversion.

$$DR = F_{OSC} \times \frac{1}{OSR} \times \frac{1}{2^{(CLKDIV+1)}} \times \frac{1}{3}$$

If FOSC is 2.5MHz of (TYP.), Conversion data rate will be set in the table below.

OSR	Date Rate [sps]			
	CLKDIV=0 (Recommendation)	CLKDIV=1(*)	CLKDIV=2(*)	CLKDIV=3(*)
512	0.814k	0.407k	0.204k	0.102k
256	1.63k	0.814k	0.407k	0.204k
128	3.26k	1.63k	0.814k	0.407k
64	6.51k	3.26k	1.63k	0.814k

(*) This parameter is not production tested.

OPTION0 Register

Register Address: 0x6

OPTION0								
Bit	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Bit Name	CHIPID		LPW_EN	REF_INT_EN	CEMODE		CE	AUTOSLP
R / W	R		RW	RW	RW		RC	RW
Reset	0x2		0	0	0x0		0	0

Bit	Bit Name	Function
[7:6]	CHIPID	Used to identify the chip.
[5]	LPW_EN	Low power setting. ADC operating clock frequency (FMOD) becomes FMOD = FOSC / 8 regardless of CLKDIV setting. 0: Normal Mode 1: Low Power Mode
[4]	REF_INT_EN	ADC reference voltage setting. 0: External reference voltage VREFP / VREFN 1: Internal reference voltage REF / GND
[3:2]	CEMODE	SPI communication error mode setting. 0: Communication Error function OFF 1: Use prohibition 2: CRC8 3: Check Sum
[1]	CE	The communication error can be detected if CEMODE is set to 2 (CRC8) or 3 (Check Sum). 0: No communication error 1: Communication error (Sticky bit)
[0]	AUTOSLP	When MODE is Idle (0x0), set to ON / OFF of analog block 0: ON (Wait) 1: OFF (Power down) When the customer change AUTOSLP from 1to 0, conversion start is necessary to start-up time of the analog block.

GAIN1 / GAIN2 Register

Register Address: 0x8, 0x9

	GAIN1 / GAIN2																							
Bit	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Bit Name	GAIN																							
R / W	RW																							
Reset	0x00								0x00								0x00							

Bit	Bit Name	Function
[23:0]	GAIN	Gain coefficient derived in gain calibration or the external writing gain coefficient. 18-bit unsigned coefficient, GAIN [23:18] is always "0". The customer can do the external writing gain coefficient, when internal clock is active only. In case of writing gain coefficient, please set to "0" AUTOSLP bit of OPTION0 register.

OFFSET1 / OFFSET2 Register

Register Address: 0xC, 0xD

	OFFSET1 / OFFSET2																							
Bit	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Bit Name	OFFSET																							
R / W	RW																							
Reset	0x00								0x00								0x00							

Bit	Bit Name	Function
[23:0]	OFFSET	Offset coefficient derived in offset calibration or the external writing offset coefficient. 20-bit signed coefficient, OFFSET [23:20] is sign-extended value. (20) The customer can do the external writing offset coefficient, when internal clock is active only. In case of writing offset coefficient, please set to "0" AUTOSLP bit of OPTION0 register.

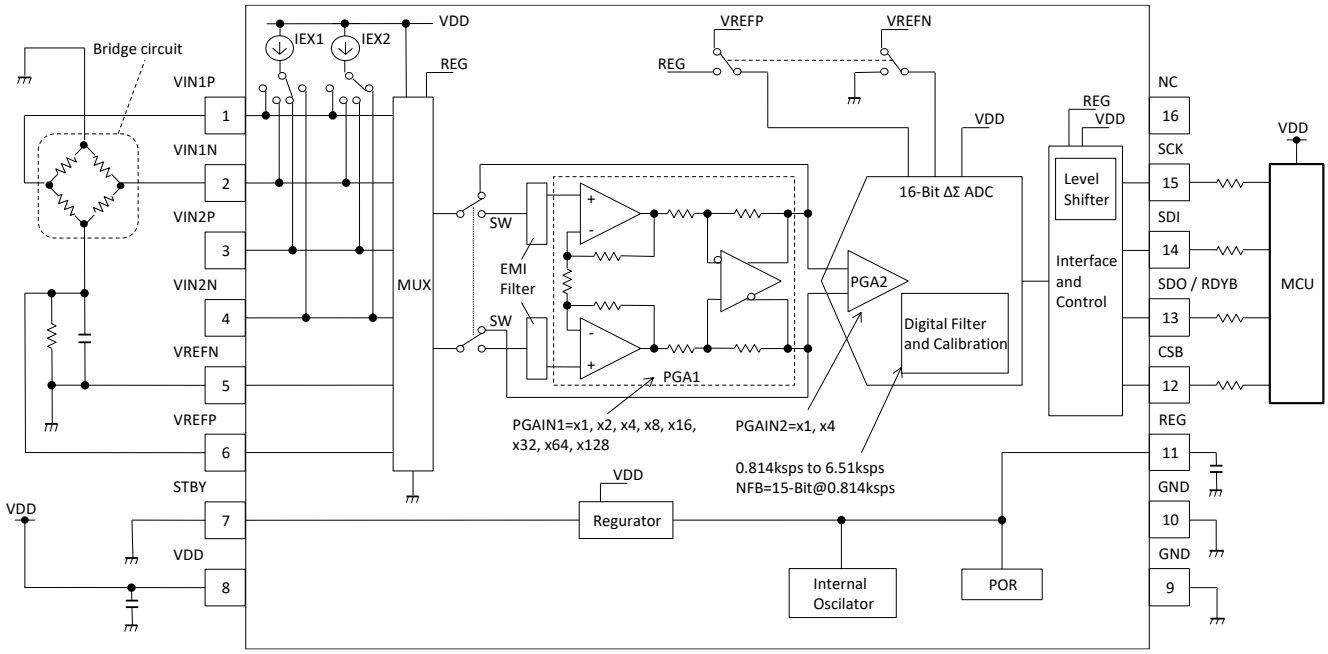
(20) Sign - extended: If the sign is (-) fill the 1 in the free space. If the sign is (+) fill the "0" in the free space
- In the case of -4 in decimal 8- bit is “11111100”.
  16-bit sign extension is “11111111 11111100”.
- In the case of +4 in decimal 8-bit is “00000100”
  16-bit sign extension is “00000000 00000100”

The GAINn and OFFSETn registers are used for the coefficients used in gain and offset calibration.
“n” is determined by the setting value on the positive input side, CTRL Register 0x0 CHSELP[10:8].
Refer the below table: Data Calibration Coefficient Correspondence Table 3.

Table 3 Data Calibration Coefficient Correspondence Table

CHSELP Set Value	Positive	Gain n Register	OFFSET n Register
0x0	VIN1P	GAIN1	OFFSET1
0x1	VIN1N	GAIN1	OFFSET1
0x2	VIN2P	GAIN2	OFFSET2
0x3	VIN2N	GAIN2	OFFSET2
0x4	VREFN	GAIN1	OFFSET1
0x5	VREFP	GAIN1	OFFSET1
0x6	REG	GAIN1	OFFSET1
0x7	GND	GAIN1	OFFSET1

■ TYPICAL APPLICATION CIRCUIT



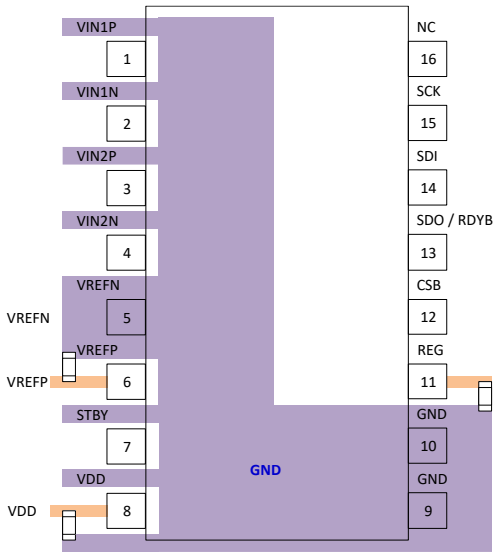
NA2200 Typical Application Circuit

Notes on External Parts

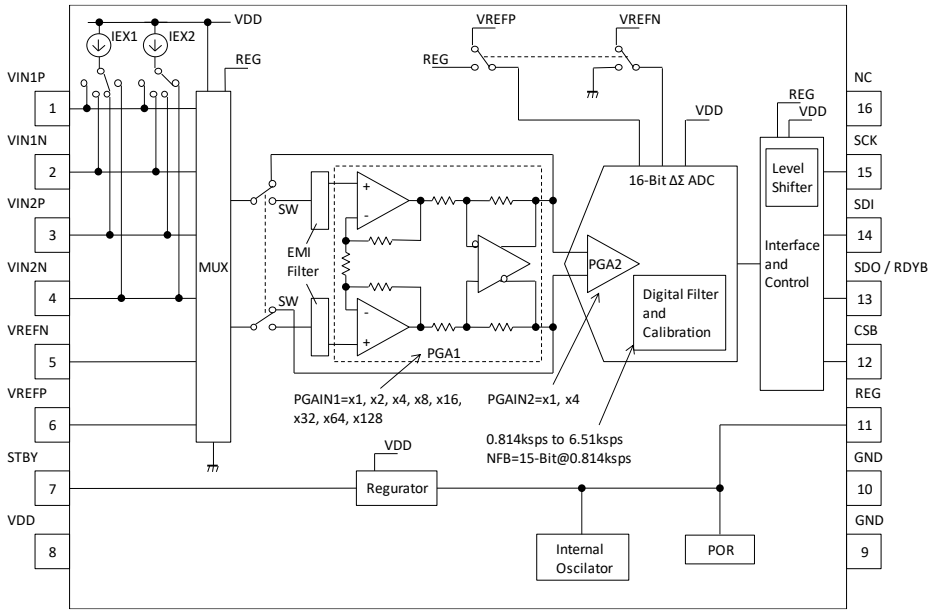
Place a decoupling capacitor 0.1µF close to 11pin (REG). A decoupling capacitor should be connected to ground for stability.
The regulator is optimized for NA2200 operation, so do not connect any components other than the decoupling capacitor to 11pin(REG).

It is recommended that 5pin (VREFN) is connected to ground.

The printed circuit board (PCB) layout pattern example of NA2200 is shown below.



■ BLOCK DIAGRAM



NA2200 Block Diagram

■ OPERATING DESCRIPTION

The NA2200 uses a PGA (Programmable Gain Amplifier) to amplify analog signals obtained from sensors and other devices connected to the VIN1P / VIN1N / VIN2P / VIN2N input terminals. Combination of PGA1 / PGA2 can amplify signals up to 512 times. The amplified signal is converted to digital data by a 16-Bit ΔΣ ADC, and after signal processing such as offset calibration and gain calibration, the digital signal is output to the MCU via SPI communication. A built-in level shifter outputs digital signals at the VDD level, so it can be connected to a 5V MCU. It supports up to 2 inputs in differential mode and up to 4 inputs in single-ended mode.

It has two excitation current sources and can used for temperature controller applications using resistance temperature detectors.

The reference voltage source for the ADC can be set to either an external reference voltage VREFP / VREFN input externally or an internal reference voltage REG using an internal regulator.

In addition to Normal Mode, Low Power Mode (conversion speed 1/4 and current consumption 1/4 compared to Normal Mode), Sleep Mode (OFF except bias and REG circuit), and Standby Mode (all circuit OFF, current consumption 0.1μA or less) can be selected.

■ APPLICATION NOTES

■ TERMINAL DESCRIPTION

● 1pin (VIN1P), 2pin (VIN1N), 3pin (VIN2P), 4pin (VIN2N), Analog Input terminals, Excitation Current Source Output terminals

Analog input terminals for inputting signals from external sources such as sensors.
It supports up to 2 inputs in differential mode and up to 4 inputs in single-ended mode.
CHSELP and CHSELN in CTRL register 0x0 select the analog input channel for data conversion (built-in multiplexer function).
NA2200 has two excitation current sources to provide a constant current to the sensors. IEXCONF register 0x2 selects the analog input channel to which the excitation current source is connected and the current value can be set.

● 5pin (VREFN), 6pin (VREFP), Reference Voltage Input terminals

Reference voltage input terminals. Negative input / positive input are supported.

● 7pin (STBY), Standby terminal

Standby terminal. NA2200 is in Standby Mode when STBY = VDD.

● 8pin (VDD), Power Supply terminal

Power supply terminal. The applied DC voltage range is 2.7V to 5.5V.

● 9pin (GND), 10pin (GND), Ground terminals

Ground terminals of NA2200.

● 11pin (REG), Built-in regulator output terminal for digital power supply

NA2200 has a built-in regulator for digital power supply. 11pin (REG) is the output terminal.
A decoupling capacitor should be connected to ground for stability. Place a decoupling capacitor close to 11pin (REG).
The regulator is optimized for NA2200 operation, so do not connect any components other than the decoupling capacitor.

● 12pin (CSB), SPI chip select terminal

NA2200 serial interface chip select terminal. It is a digital input terminal.
When the CSB terminal is high level, SCK and SDI are disabled and communication is not possible.
When the CSB terminal is low level, SCK and SDI are enable and communication is possible.
After the CSB terminal changes from high to low level, the state of the SPI slave interface is reset and the command byte must be resent.

● **13pin (SDO/RDYB), SPI serial data output / RDYB terminal**

NA2200 serial interface data output / RDYB terminal. It is a digital output terminal.
When reading, data from the SDO/RDYB terminal is communicated MSB first.
SDO/RDYB is synchronized to the rising edge of SCK.
The RDYB bit outputs “1” or “0” depending on whether the ADC is converting or not. (1: conversion in progress or 0: conversion completed)

● **14pin (SDI), SPI serial data input terminal**

NA2200 serial interface data input terminal. It is a digital input terminal.
When writing, data to the SDI terminal is communicated MSB first.
SDI is captured on the falling edge of SCK.

● **15pin (SCK), SPI serial clock input terminal**

NA2200 serial interface clock input terminal. It is a digital input terminal.

● **16pin (NC), Non connection**

Non connection terminal. Ground the terminal.

■ Power up sequence

When the power supply pin VDD reaches a voltage at which the circuit can operate, the internal reset is released by the built-in power-on reset circuit and initialization begins.
After the reset is released, the startup sequence of the NA2200 is completed after a waiting period of about 600µsec .
(The waiting time of about 600µsec does not include the power-on time.)
After the startup sequence is completed, the device transitions to the idle state and is ready for AD conversion operation.

■ Effective resolution, Noise Free Bit (NFB)

Data Rate (DR) is speed at the time of single conversion (1 settling).
Output code variation σ is the effective resolution in the VIN1P and VIN1N (or VIN2P and VIN2N) connected to VDD/2, 6.6σ is the NFB.

< Condition >
- FMOD=1.25MHz
- VDD=5.0V, GND=0V
- VREFP=5.0V, VREFN=0V
- Differential input
- CHOP OFF
- T_a=+25°C

(1) Normal Mode & External REF

DR vs. Effective resolution (Unit: bit)

OSR	DR [sps]	PGA OFF	PGA ON									
			x1	x2	x4	x8	X16	x32	x64	x128	x256	x512
512	0.814k	16	16	16	16	16	16	16	16	16	16	16
256	1.63k	16	16	16	16	16	16	16	16	16	16	16
128	3.26k	16	16	16	16	16	16	16	16	16	16	15
64	6.51k	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5	12.5

DR vs. NFB (Unit: bit)

OSR	DR [sps]	PGA OFF	PGA ON									
			x1	x2	x4	x8	x16	x32	x64	x128	x256	x512
512	0.814k	16	16	16	16	16	16	16	16	16	14.5	14
256	1.63k	16	16	16	16	16	16	16	16	16	14.5	14
128	3.26k	14	14	14	14	14	14	14	14	14	13	12.5
64	6.51k	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	10

(2) Low Power Mode & External REF

DR vs. Effective resolution (Unit: bit)

OSR	DR [sps]	PGA OFF	PGA ON									
			x1	x2	x4	x8	X16	x32	x64	x128	x256	x512
512	0.203k	16	16	16	16	16	16	16	16	16	16	16
256	0.407k	16	16	16	16	16	16	16	16	16	16	16
128	0.814k	16	16	16	16	16	16	16	16	16	14	14
64	1.63k	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5	12.5	12.5

DR vs. NFB (Unit: bit)

OSR	DR [sps]	PGA OFF	PGA ON									
			x1	x2	x4	x8	x16	x32	x64	x128	x256	x512
512	0.203k	16	16	16	16	16	16	16	16	16	14.5	14.5
256	0.407k	16	16	16	16	16	16	16	16	16	14	14
128	0.814k	14	14	14	14	14	14	14	14	14	11.5	11.5
64	1.63k	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	10	10

(3) Normal Mode & Internal REF

DR vs. Effective resolution (Unit: bit)

OSR	DR [sps]	PGA OFF	PGA ON									
			x1	x2	x4	x8	X16	x32	x64	x128	x256	x512
512	0.814k	16	16	16	16	16	16	16	16	16	16	16
256	1.63k	16	16	16	16	16	16	16	16	16	16	15.5
128	3.26k	16	16	16	16	16	16	16	16	16	15	15
64	6.51k	14	14	14	14	14	14	14	14	14	12	12

DR vs. NFB (Unit: bit)

OSR	DR [sps]	PGA OFF	PGA ON									
			x1	x2	x4	x8	x16	x32	x64	x128	x256	x512
512	0.814k	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14	13.5	13
256	1.63k	14	14	14	14	14	14	14	14	14	13	13
128	3.26k	13	13	13	13	13	13	13	13	13	12	12
64	6.51k	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	9.5	9.5

(4) Low Power Mode & Internal REF

DR vs. Effective resolution (Unit: bit)

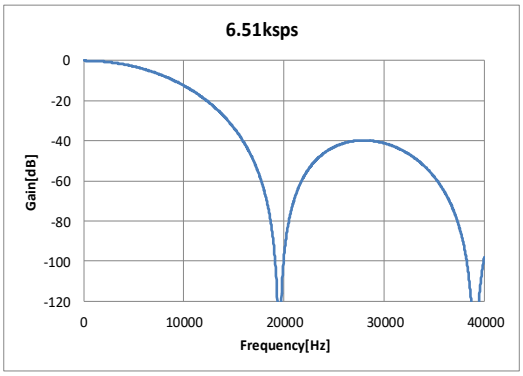
OSR	DR [sps]	PGA OFF	PGA ON									
			x1	x2	x4	x8	X16	x32	x64	x128	x256	x512
512	0.203k	16	16	16	16	16	16	16	16	16	16	16
256	0.407k	16	16	16	16	16	16	16	16	16	16	16
128	0.814k	16	16	16	16	16	16	16	16	16	15	15
64	1.63k	14	14	14	14	14	14	14	14	14	13.5	12.5

DR vs. NFB (Unit: bit)

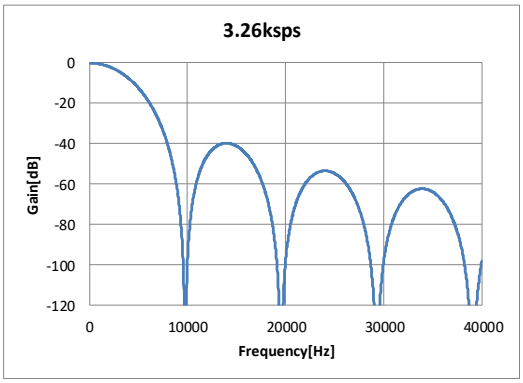
OSR	DR [sps]	PGA OFF	PGA ON									
			x1	x2	x4	x8	x16	x32	x64	x128	x256	x512
512	0.203k	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14	13.5	13.5
256	0.407k	14	14	14	14	14	14	14	14	14	13.5	13
128	0.814k	13	13	13	13	13	13	13	13	13	12.5	12
64	1.63k	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11	10

■ Digital filter frequency characteristic

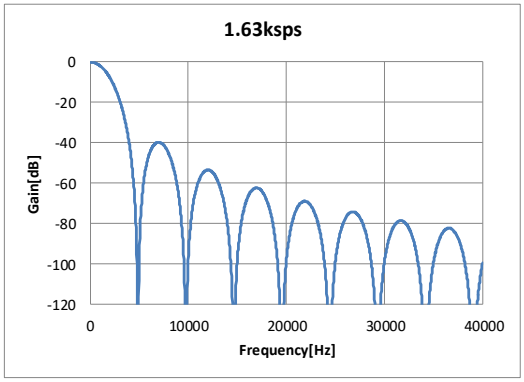
The output of the ΔΣ modulator is converted to a digital value of high resolution by a digital filter (third-order Sinc filter).
Frequency characteristics will change depending on the data rate.
When the conversion data rate (DR) is 6.51ksps, 3.26ksps, 1.63ksps, 0.814ksps, frequency characteristics of the digital filter is shown below. Characteristic is the case of FMOD=1.25MHz.



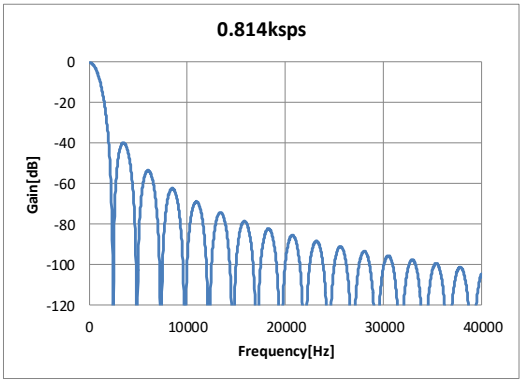
DR=6.51ksps



DR=3.26ksps



DR=1.63ksps



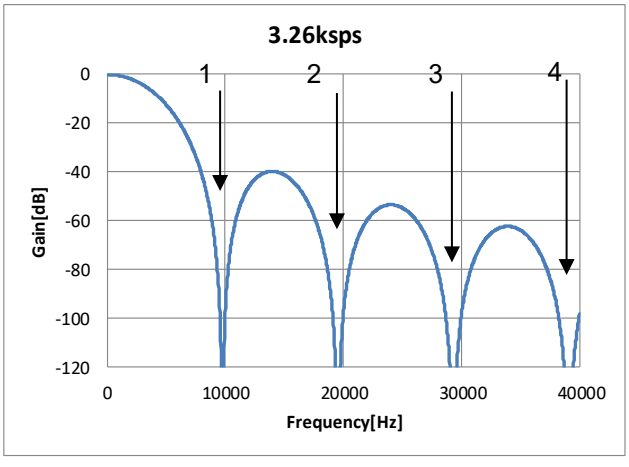
DR=0.814ksps

It has a first notch in the frequency of the data rate x 3.
Or later, it has a notch to the integer multiple of the position.(21)

(e.x.) In the case 3.26ksps (Figure of right)
Position of the notch
1. 9.8kHz （3.26kHz x 3 x 1）
2. 19.6kHz（3.26kHz x 3 x 2）
3. 29.3kHz（3.26kHz x 3 x 3）
4. 39.1kHz（3.26kHz x 3 x 4）

.
.

(N) 3.26kHz x 3 x N (N is an integer)



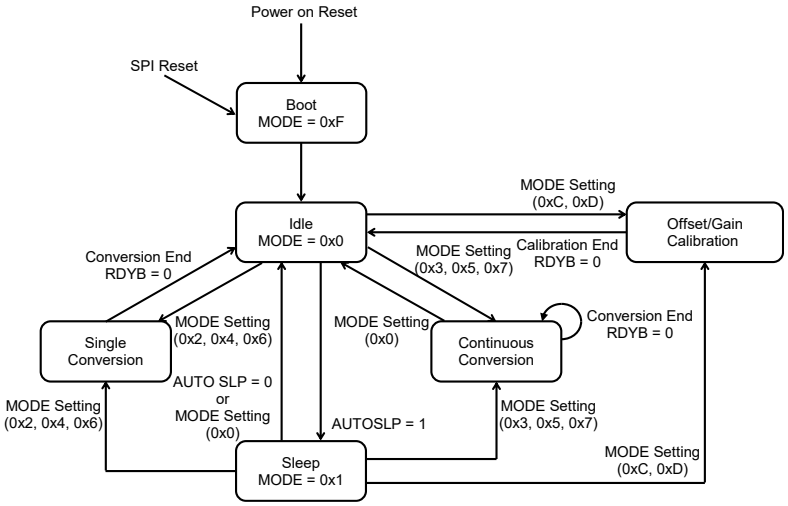
DR=3.26ksps

(21) Position of the notch varies in proportion to the frequency of the FMOD
FMOD is ±10% variation. Position of the notch is likely to vary ±10% from the above figure.

■ Conversion Control

Set the conversion operation by MODE bit of CTRL register.

MODE	OPERATION
0x0	Idle
0x1	Sleep
0x2	Single conversion
0x3	Continuous conversion
0x4	Single conversion + CHOP
0x5	Continuous conversion + CHOP
0x6	Single conversion + CHOP + IEX CHOP
0x7	Continuous conversion + CHOP + IEX CHOP
0x8, 0x9 0xA, 0xB	Not used
0xC	Calibration system offset
0xD	Calibration system gain
0xE	Not used
0xF	Boot



< Definition of time >

(1) ADC conversion time of basic : T_{adc} (sec)

$$T_{adc} = OSR / FMOD$$

OSR : Over Sampling Rate
FMOD: Clock Frequency of ADC

(2) Calculation time for data correction (after ADC conversion) : T_{cal} (sec)

$$T_{cal} = 40 / FOSC$$

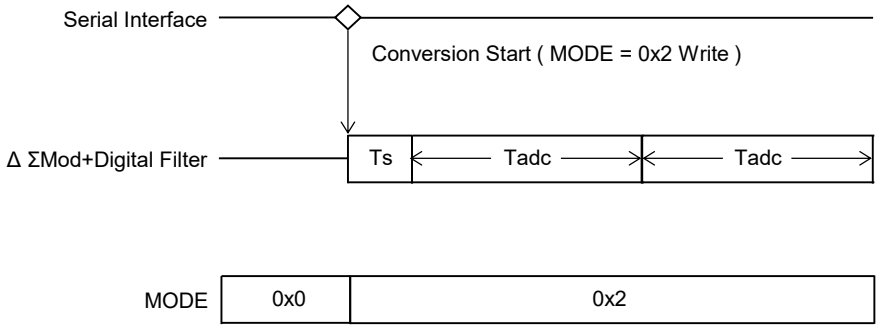
FOSC : Clock Frequency of Internal Oscillator

(3) Calculation time for gain coefficient (after gain calibration) : T_{div} (sec)

$$T_{div} = 70 / FOSC$$

(4) Setup time : T_s

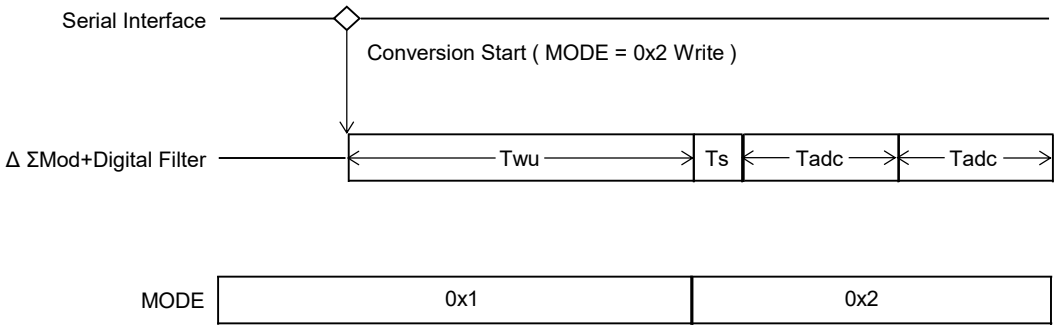
When the analog block is ON (AUTOSLP bit of OPTION 0 register = "0"), setting the MODE bit in CTRL register to operation mode starts operation after T_s (about 10µsec). The case where the MODE bit is switched from "Idle (0x0)" to "single conversion (0x2)" is shown below.



Setup time AUTOSLP=0

(5) Startup wait time : T_{wu}

Waiting time of T_{wu} (about 70µsec) is required when changing the analog block from OFF to ON (AUTOSLP bit from "1" to "0"). The figure below shows the case where the MODE bit is switched from "sleep (0x1)" to "single conversion (0x2)".

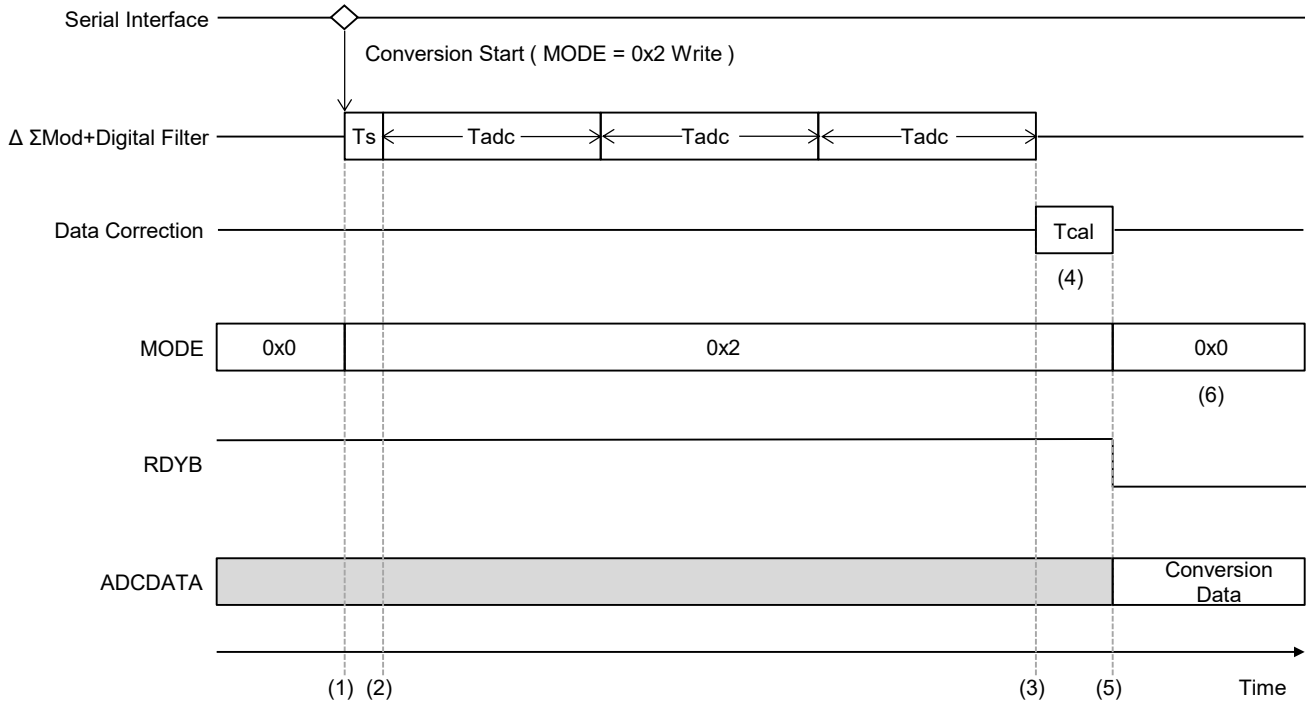


Startup wait time AUTOSLP=1

Single conversion operation (MODE = 0x2)

It is the basic conversion of NA2200.
Even if the input signal is switched by the multiplexer (external), waiting time for converted data is unnecessary.
(1 settling, zero latency)

When the conversion cycle is long, the recommended usage is that converting once and power-down the remaining period. So, the consumption current of NA2200 can be reduced. It is the optimum conversion method for "switching input signals with multiplexer" and "low power consumption".



Single conversion timing

STEP	DETAILS
(1)	Set to single conversion. (MODE bit in CTRL register = "0x2")
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion completed with conversion time (3 x T_{adc}). The conversion data is the result of the convolution integration of 3 x T_{adc}. (ΔΣ Mod + Digital Filter)
(4)	Data is corrected with calculation time (T_{cal}).
(5)	Conversion data stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	Shift to Idle state. (MODE bit= ”0x0”)

In NA2200, the data rate is specified by the following formula. (Single conversion)

$$DR = F_{OSC} \times \frac{1}{OSR} \times \frac{1}{2^{(CLKDIV+1)}} \times \frac{1}{3}$$

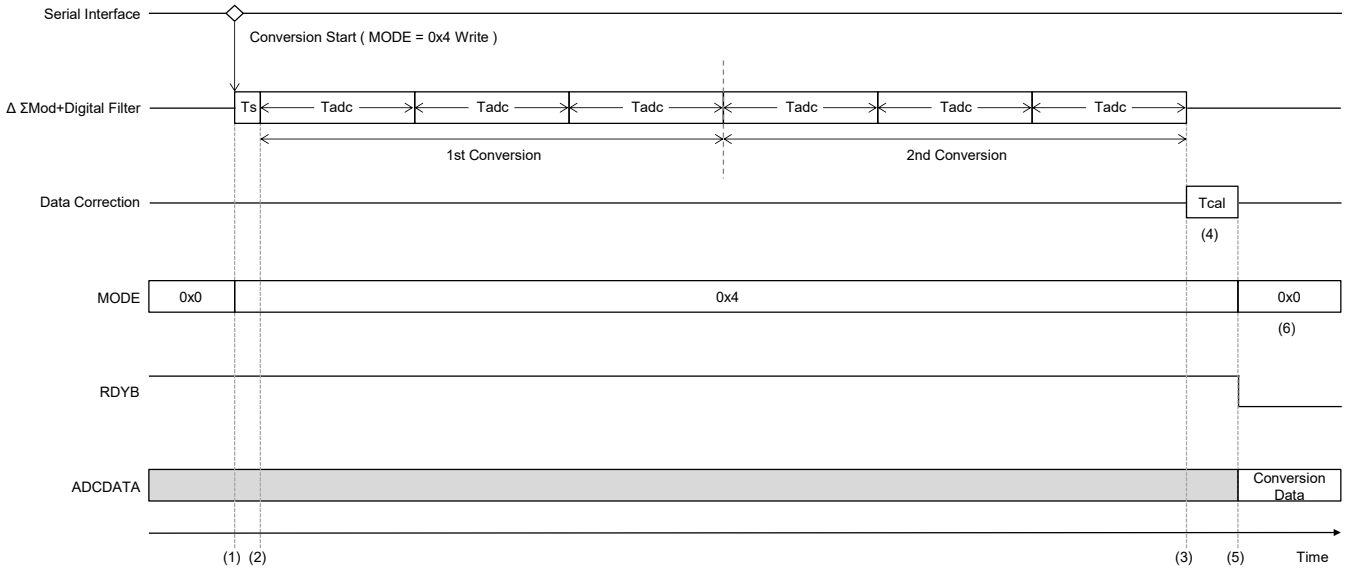
The conversion data rate (DR) is DR_all when T_s and T_{cal} are considered. (In the table below, CLKDIV=0)

OSR	DR [sps]	3xT_{adc}(=1/DR) [sec]	3xT_{adc}+T_s+T_{cal} [sec]	DR_all (=1/(3xT_{adc}+T_s+T_{cal})) [sps]
512	0.814k	1.23m	1.26m	0.794k
256	1.63k	0.614m	0.640m	1.56k
128	3.26k	0.307m	0.333m	3.00k
64	6.51k	0.154m	0.180m	5.56k

“Single conversion + CHOP” operation (MODE = 0x4)

Single conversion performs single conversion twice. By change VINxP and VINxN at the second conversion, the NA2200 offset can be removed in real time. The change of VINxP and VINxN is done automatically by the internal switch.

With single conversion, it is the optimum conversion method for "when you want to calibrate the offset in real time". Though, the data rate is half of single conversion.



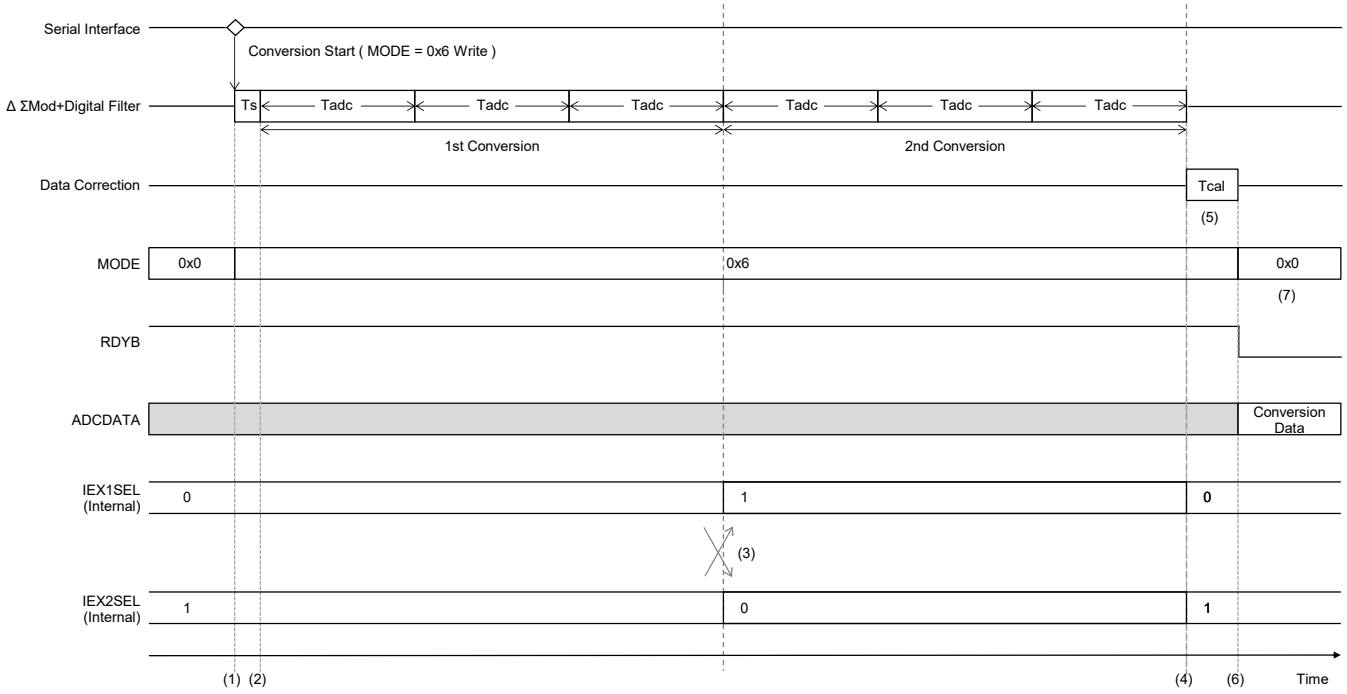
Single conversion + CHOP timing

STEP	DETAILS
(1)	Set to single conversion + CHOP. (MODE bit in CTRL register = "0x4")
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion completed in conversion time (6 x T_{adc}). The conversion data is the result of the convolution integration of 6 x T_{adc}. (1st & 2nd conversion of "ΔΣ Mod + Digital Filter".)
(4)	Data is corrected in calculation time (T_{cal}).
(5)	Conversion data stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	Shift to Idle state. (MODE bit= ”0x0”)

“Single conversion + CHOP + IEX CHOP” operation (MODE = 0x6)

Single conversion performs single conversion twice. By change VINxP and VINxN at the second conversion, the NA2200 offset can be removed in real time. The change of VINxP and VINxN is done automatically by the internal switch.
The excitation current setting is automatically switched in conjunction with the CHOP operation.

With single conversion, it is the optimum conversion method for "when you want to measure 3-wire RTD with high accuracy". Though, the data rate is half of single conversion.



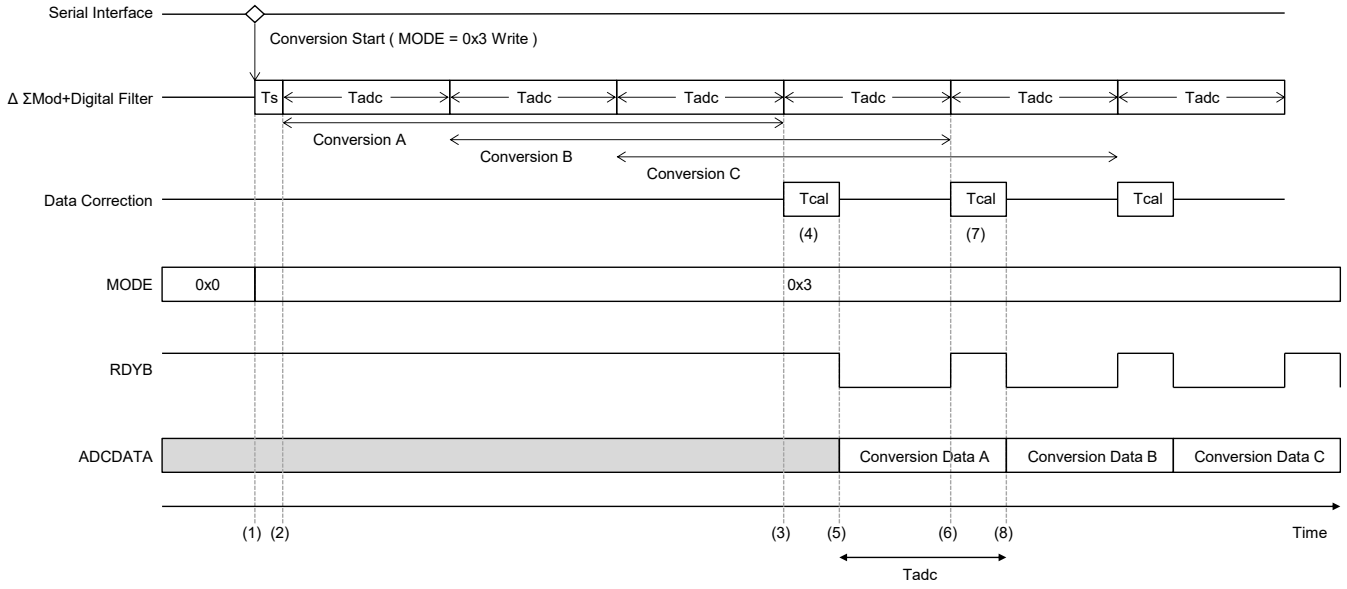
Single conversion + CHOP + IEX CHOP timing

STEP	DETAILS
(1)	Set to single conversion + CHOP + IEX CHOP. (MODE bit in CTRL register = "0x6")
(2)	After the set-up time (T_s), start the conversion.
(3)	The setting IEX1SEL / IEX2SEL of the excitation current source is switched in conjunction with the CHOP operation that switches the input polarity in the second conversion.
(4)	Conversion completed in conversion time (6 x T_{adc}). The conversion data is the result of the convolution integration of 6 x T_{adc}. (1st & 2nd conversion of "ΔΣ Mod + Digital Filter".)
(5)	Data is corrected in calculation time (T_{cal}).
(6)	Conversion data stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(7)	Shift to Idle state. (MODE bit= ”0x0”)

Continuous conversion operation (MODE = 0x3)

When input signals are switched by the multiplexer, the same waiting time as the first conversion (conversion A) is required. When input signal is not switched by multiplexer, wait time after the second conversion (conversion B) is unnecessary.

It is the optimum conversion method for "when input is not switched by multiplexer" and "when you want to maximize data rate". The data rate is three times that of single conversion.



Continuous conversion timing

STEP	DETAILS
(1)	Set to continuous conversion. (MODE bit in CTRL register = "0x3")
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion A (1st) completed in conversion time (3 x T_{adc}). The conversion data A is the result of the convolution integration of conversion A ("3 x T_{adc}" of ΔΣ Mod + Digital Filter")
(4)	Data is corrected in calculation time (T_{cal})
(5)	Conversion data A (1st) stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	After completion of conversion B (2nd), RDYB bit changes from "0" to "1". The conversion data B is the result of the convolution integration of conversion B ("3 x T_{adc}" of ΔΣ Mod + Digital Filter)
(7)	Data is corrected in calculation time (T_{cal}).
(8)	Conversion data B (2nd) stored (overwrite) in ADCDATA register. At that time, RDYB bit changes from "1" to "0".

Repeat steps (5) to (8) until the operation mode is set to idle (MODE bit is set to "0x0").

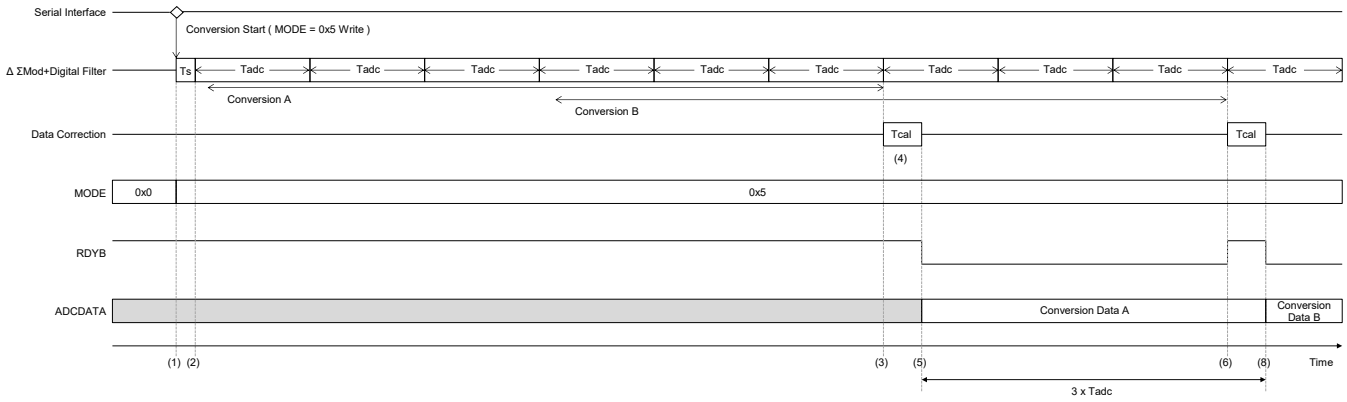
“Continuous conversion + CHOP” operation (MODE = 0x5)

By changing VINxP and VINxN every "3 x T_{adc}", the NA2200 offset can be removed in real time. The change of VINxP and VINxN is done automatically by the internal switch.

When input signals are switched by the multiplexer, the same waiting time as the first conversion (conversion A) is required. When input signal is not switched by multiplexer, wait time after the second conversion (conversion B) is unnecessary.

As with “single conversion + CHOP” operation, offset of whole chip can be calibrated in real time.

It is the optimal conversion method for "when you want to calibrate offsets in real time" with continuous conversion. Though, the data rate is 1/3 of continuous conversion. (Same data rate as single conversion)



Continuous conversion + CHOP timing

STEP	DETAILS
(1)	Set to continuous conversion + CHOP. (MODE bit in CTRL register = "0x5")
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion A (1st) completed in conversion time (6 x T_{adc}). The conversion data A is the result of the convolution integration of conversion A (“6 x T_{adc}” of ΔΣ Mod + Digital Filter”)
(4)	Data is corrected in calculation time (T_{cal}).
(5)	Conversion data A (1st) stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	After completion of conversion B (2nd), RDYB bit changes from "0" to "1". The conversion data B is the result of the convolution integration of conversion B (“6 x T_{adc}” of ΔΣ Mod + Digital Filter)
(7)	Data is corrected in calculation time (T_{cal}).
(8)	Conversion data B (2nd) stored (overwrite) in ADCDATA register. At that time, RDYB bit changes from "1" to "0".

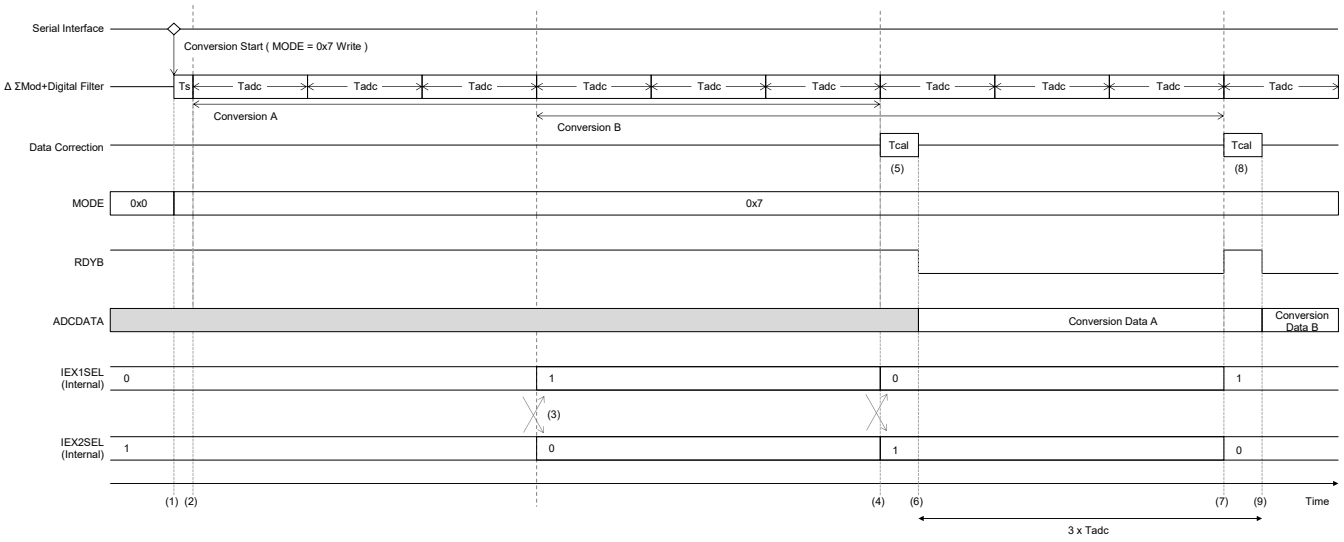
Repeat steps (5) to (8) until the operation mode is set to idle (MODE bit is set to "0x0").

“Continuous conversion + CHOP + IEX CHOP” operation (MODE = 0x7)

By changing VINxP and VINxN every "3 x T_{adc}", the NA2200 offset can be removed in real time. The change of VINxP and VINxN is done automatically by the internal switch.
The excitation current setting is automatically switched in conjunction with the CHOP operation.

When input signals are switched by the multiplexer, the same waiting time as the first conversion (conversion A) is required. When input signal is not switched by multiplexer, wait time after the second conversion (conversion B) is unnecessary.

As with “single conversion + CHOP” operation, offset of whole chip can be calibrated in real time.



Continuous conversion + CHOP +IEX CHOP timing

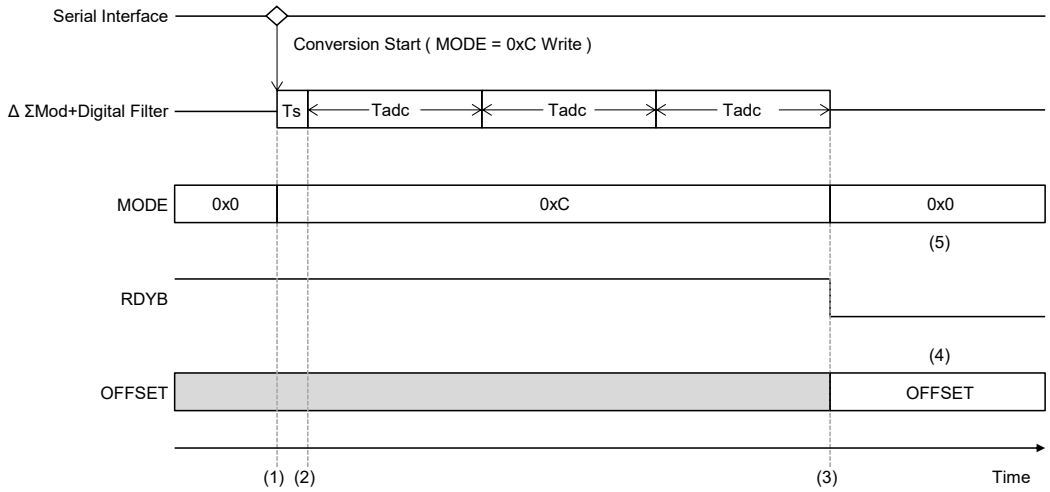
STEP	DETAILS
(1)	Set to continuous conversion + CHOP + IEX CHOP. (MODE bit in CTRL register = "0x7")
(2)	After the set-up time (T_s), start the conversion.
(3)	The setting IEX1SEL / IEX2SEL of the excitation current source is switched in conjunction with the CHOP operation that switches the input polarity in the conversion time (3 x T_{adc}).
(4)	Conversion A (1st) completed in conversion time (6 x T_{adc}). The conversion data A is the result of the convolution integration of conversion A (“6 x T_{adc}” of ΔΣ Mod + Digital Filter”)
(5)	Data is corrected in calculation time (T_{cal}).
(6)	Conversion data A (1st) stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(7)	After completion of conversion B (2nd), RDYB bit changes from "0" to "1". The conversion data B is the result of the convolution integration of conversion B (“6 x T_{adc}” of ΔΣ Mod + Digital Filter) The setting IEX1SEL / IEX2SEL of the excitation current source is switched.
(8)	Data is corrected in calculation time (T_{cal}).
(9)	Conversion data B (2nd) stored (overwrite) in ADCDATA register. At that time, RDYB bit changes from "1" to "0".

Repeat steps (6) to (9) until the operation mode is set to idle (MODE bit is set to "0x0").

With continuous conversion, it is the optimum conversion method for "when you want to measure 3-wire RTD with high accuracy".
Though, the data rate is 1/3 of continuous conversion. (Same data rate as single conversion)

Offset calibration operation (MODE = 0xC)

Timing is almost the same as single conversion operation.
Calculate the offset amount and save it in the OFFSET register (OFFSET1, OFFSET2).



Offset calibration timing

STEP	DETAILS
(1)	Set to offset calibration. (MODE bit in CTRL register = “0xC”)
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion is complete in conversion time (3 xT_{adc}).
(4)	Conversion data stored in OFFSET register (OFFSET1, OFFSET2). At that time, RDYB bit changes from "1" to "0".
(5)	Shift to Idle state. (MODE bit= ”0x0”)

For offset calibration, use the CHSELP / CHSELN bits in the CTRL register to select the input channel.
In addition, select the REF_INT_EN bit in the OPTION0 register.

When the offset calibration command is executed, the following processing is automatically performed.

- Using the input channel selected by the CHSELP / CHSELN bit, AD conversion is performed with the reference voltage source of the ADC selected by the REF_INT_EN bit of the OPTION0 register, and the offset is calculated.
- Store calculated offset in OFFSET registers.

The example of internal ADC offset calibration.

(1) REF_INT_EN = 0 (ADC reference voltage = external reference VREFP / VREFN used)

When setting the following PGA gains and input channels, and the offset calibration command is executed, the offset calibration is performed.

- Set PGA1 to OFF (PGA1EN = 0x0) and set the PGA2 gain to “x1” (PGA2GAIN = 0x0).
- Applying VREFN internally to the positive and negative inputs of the ADC. (CHSELP = 0x4, CHSELN = 0x4)
- Calculate the offset.
- Store calculated offset in OFFSET registers.

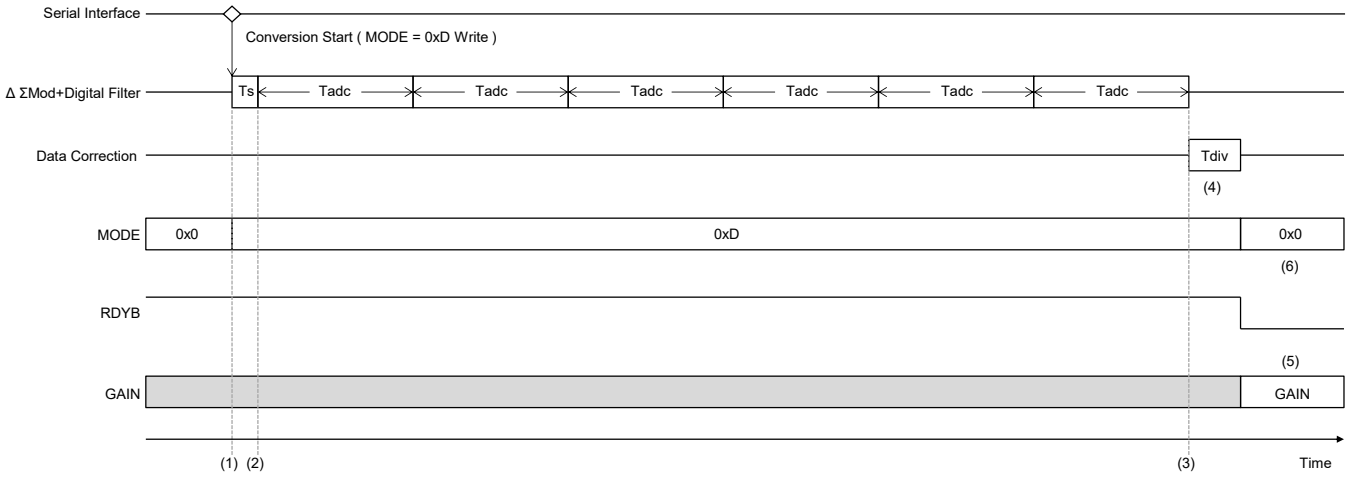
(2) REF_INT_EN = 1 (ADC reference voltage = internal reference REG / GMD used)

When setting the following PGA gains and input channels, and the offset calibration command is executed, the offset calibration is performed.

- Set PGA1 to OFF (PGA1EN = 0x0) and set the PGA2 gain to “x1” (PGA2GAIN = 0x0).
- Applying GND internally to the positive and negative inputs of the ADC. (CHSELP = 0x7, CHSELN = 0x7)
- Calculate the offset.
- Store calculated offset in OFFSET registers.

Gain calibration operation (MODE = 0xD)

Timing is almost the same as “single conversion + CHOP” operation.
Calculate the gain factor and save it in the GAIN register (GAIN1, GAIN2).



Gain calibration timing

STEP	DETAILS
(1)	Set to gain calibration. (MODE bit in CTRL register = “0xD”)
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion is complete in conversion time (6 xT_{adc}).
(4)	The slope (gain) coefficient is calculated in the gain coefficient calculation time (T_{div}).
(5)	The GAIN registers (GAIN 1, GAIN 2) are updated. At that time, RDYB bit changes from "1" to "0".
(6)	Shift to Idle state. (MODE bit= ”0x0”)

For gain calibration, use the CHSELP / CHSELN bits in the CTRL register to select the input channel.
In addition, select the REF_INT_EN bit in the OPTION0 register.

When the gain calibration command is executed, the following processing is automatically performed.

- Using the input channel selected by the CHSELP / CHSELN bit, AD conversion is performed with the reference voltage source of the ADC selected by the REF_INT_EN bit of the OPTION0 register, and the gain coefficient is calculated.
- Store calculated gain coefficient in GAIN registers.

The example of internal ADC gain calibration.

(3) REF_INT_EN = 0 (ADC reference voltage = external reference VREFP / VREFN used)

When setting the following PGA gains and input channels, and the gain calibration command is executed, the gain calibration is performed.

- Set PGA1 to OFF (PGA1EN = 0x0) and set the PGA2 gain to “x1” (PGA2GAIN = 0x0).
- Applying VREF internally to the positive and negative inputs of the ADC.
  (CHSELP = 0x5(VREFP), CHSELN = 0x4(VREFN))
- Calculate the gain coefficient.
- Store calculated gain coefficient in GAIN registers.

(4) REF_INT_EN = 1 (ADC reference voltage = internal reference REG / GMD used)

When setting the following PGA gains and input channels, and the gain calibration command is executed, the gain calibration is performed.

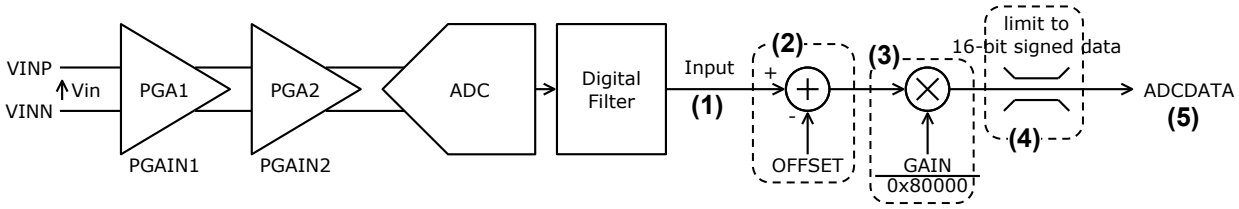
- Set PGA1 to OFF (PGA1EN = 0x0) and set the PGA2 gain to “x1” (PGA2GAIN = 0x0).
- Applying REG and GND internally to the positive and negative inputs of the ADC.
  (CHSELP = 0x6(REG), CHSELN = 0x7(GND))
- Calculate the gain coefficient.
- Store calculated gain coefficient in GAIN registers.

■ Data calibration flow / Combination of conversion operation and calibration operation

"Data calibration flow" and "Combination of conversion operation and calibration operation" are explained.

Single conversion or Continuous conversion

The figure below is a calibration flow block diagram of "single conversion" or "continuous conversion".
The offset calibration uses the value of the OFFSET register (OFFSET1, OFFSET2).
The gain calibration uses the values of the GAIN register (GAIN1, GAIN2).



STEP	DETAILS
(1)	"Input" is the following value for the input voltage V_{in}. The full scale of the digital filter is eight times signed 16 bits (262144 = 32768 x 8). $Input = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 262144$
(2)	Subtract "OFFSET" calculated by offset calibration operation from "Input".
(3)	Multiply the result of step (2) by "GAIN" calculated by the gain calibration operation. In order to convert to signed 16-bit full scale, 1 / (0x80000) = 1 / (32768 x 8) is also multiplied.
(4)	Confirm whether "-32768 ≤ (3) result ≤ +32768" is satisfied. If it is not satisfied, set the OV bit of the CTRL register to "1". If it is satisfied, set the OV bit of the CTRL register to "0".
(5)	Store the calculation result in the ADCDATA register. If "OV=1" in step (4), the ADCDATA register is the minimum value (-32768) or the maximum value (+32767). $ADCDATA = (Input - OFFSET) \times \frac{GAIN}{0x80000} = \left(\frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 262144 - OFFSET \right) \times \frac{GAIN}{0x80000}$

(Example) When applying PGAIN1 = PGAIN2 = 1, OFFSET = 0, GAIN = 0x10000, VREF = 3.3V, V_{in} = 1V,
--> ADCDATA code is "9930".(22)

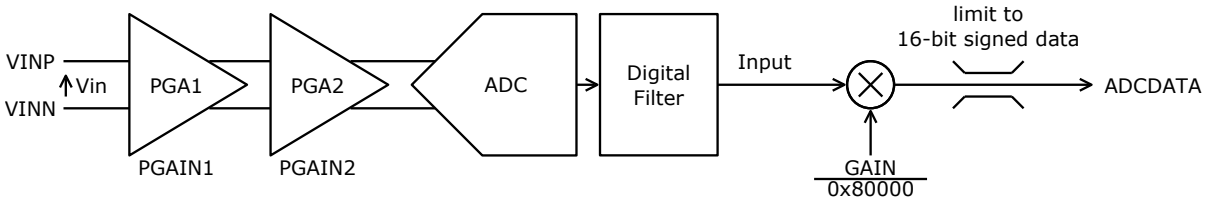
$$ADCDATA = \left(\frac{1V}{3.3V} \times 1 \times 1 \times 262144 - 0 \right) \times \frac{0x10000}{0x80000} = 9930$$

(22) When thinking of NA2200 as a black box, it is intuitively understood that it is correct.

$$ADCDATA = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 2^{15} = \frac{1V}{3.3V} \times 1 \times 1 \times 32768 = 9930$$

“Single conversion + CHOP” or “Continuous conversion + CHOP”

The figure below is a block diagram of the calibration flow of "single conversion + CHOP" or "continuous conversion + CHOP".
Since offset is removed by CHOP operation, the offset register value is not used for offset calibration.
Otherwise, it is the same operation as "1. Single conversion or Continuous conversion" on the previous page.



“Single conversion + CHOP + IEX CHOP” or “Continuous conversion + CHOP + IEX CHOP”

“Single conversion + CHOP + IEX CHOP” or “Continuous conversion + CHOP + IEX CHOP” replaces the excitation current source in conjunction with CHOP operation
Otherwise, it is the same operation as "2. Single conversion + CHOP or Continuous conversion + CHOP".

■ SPI Interface

The interface is 4-wire SPI communication of CSB, SCK, SDI, SDO / RDYB. In case, CSB fixed to GND, NA2200 can use as 3-wire SPI communication device.

When CSB is “1”, SCK and SDI are invalid. SDO / RDYB becomes high impedance.
After CSB changes from “1” to “0”, SPI communication always starts with a command byte.
When CSB is “0”, SCK and SDI become valid and these can communicate.

SDI is captured on the falling edge of SCK and SDO / RDYB is synchronized with the rising edge of SCK.
Bits are transferred in order from the MSB.

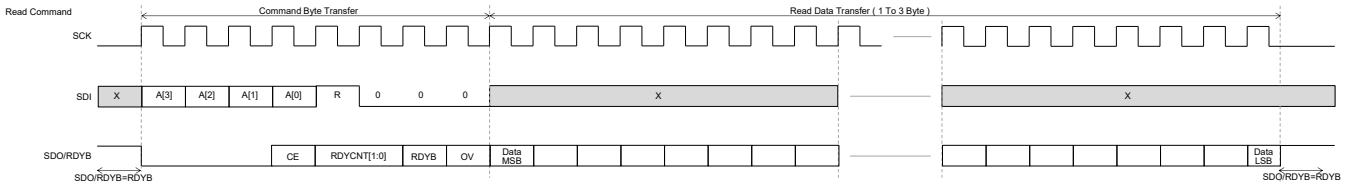
SPI communication is performed as follows.

Step	Details
(1)	Command byte transfer
(2)	Read or write data transfer (1 byte or 2 byte or 3 byte data transfer)

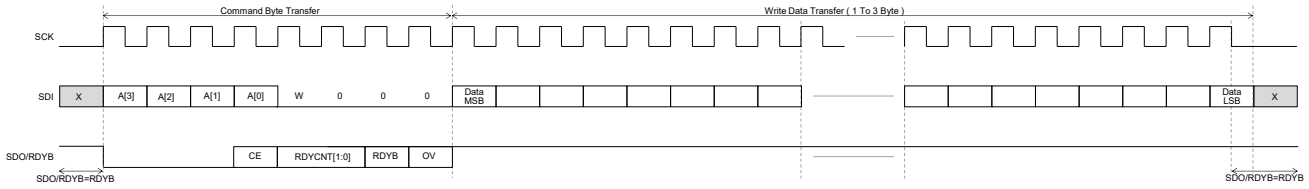
When the data transfer is completed, it waits for the command byte.
When SPI communication is not in progress, the RDYB bit value of the CTRL register is output from SDO / RDYB.
RDYB bit outputs "1" or "0" depending on the ADC operation state. (1: Conversion in progress, 0: Conversion end)

The above state is supplied from the NA2200 to the master device (microcomputer and others).
Therefore, the master device can confirm the conversion end without monitoring the NA2200 periodically.

< Reading >

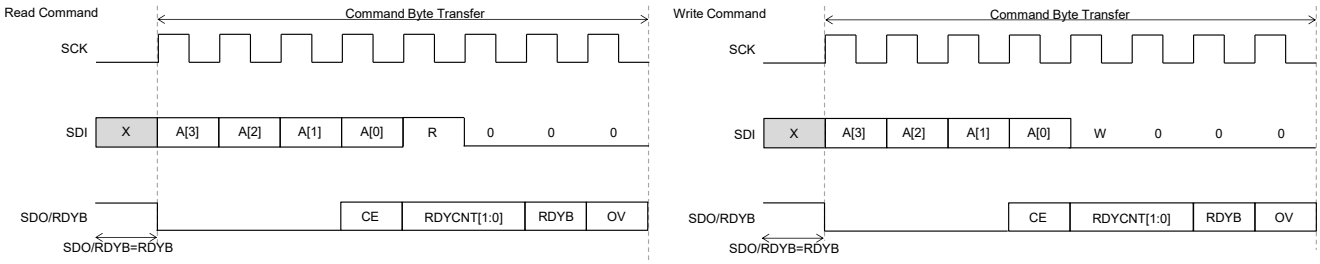


< Writing >



SPI communication format

SPI command byte



Reading **Writing**

Read command (Byte)

BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	CE	RDYCNT		RDYB	OV
R / W	-	-	-	R	R		R	R
VALUE	0	0	0	-	-		-	-

BIT	BIT NAME	FUNCTION
[7:5]	-	-
[4]	CE	Returns the same value as the CE bit of the OPTION0 register
[3:2]	RDYCNT	Returns the same value as the RDYCNT bit of the CTRL register
[1]	RDYB	Returns the same value as the RDYB bit of the CTRL register
[0]	OV	Returns the same value as the OV bit of the CTRL register

Write command (Byte)

BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	A				RW	ZERO		
R / W	W				W	W		
VALUE	-				-	0		

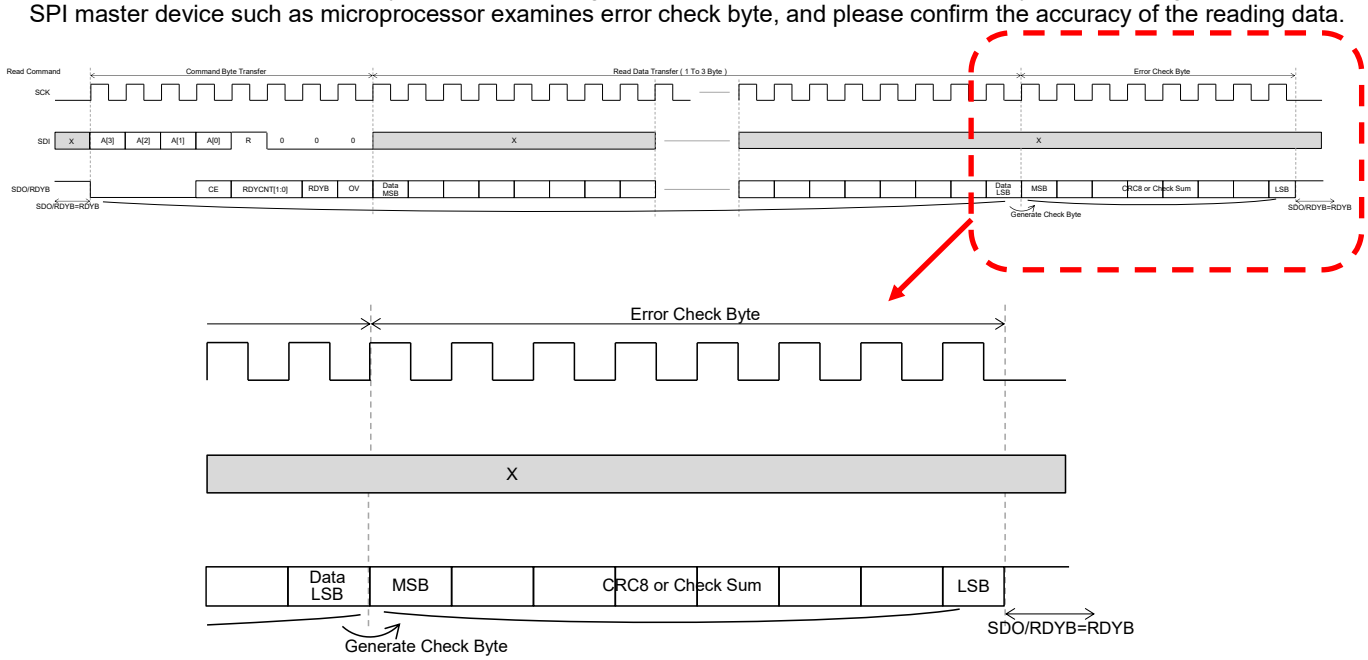
BIT	BIT NAME	FUNCTION
[7:4]	A	Specify the register address to be accessed.
[3]	RW	Specify the direction of communication. (Write or Read) 0: Write 1: Read
[2:0]	ZERO	Always write "0"

SPI communication error detection

SPI communication error detection is valid, in case CEMODE bit of the OPTION0 register (Register address: 0x6) sets to CRC8 mode or Check Sum mode.
When the communication error detection is enable, one byte of Error check byte is added after read or write data transfer.

Read mode

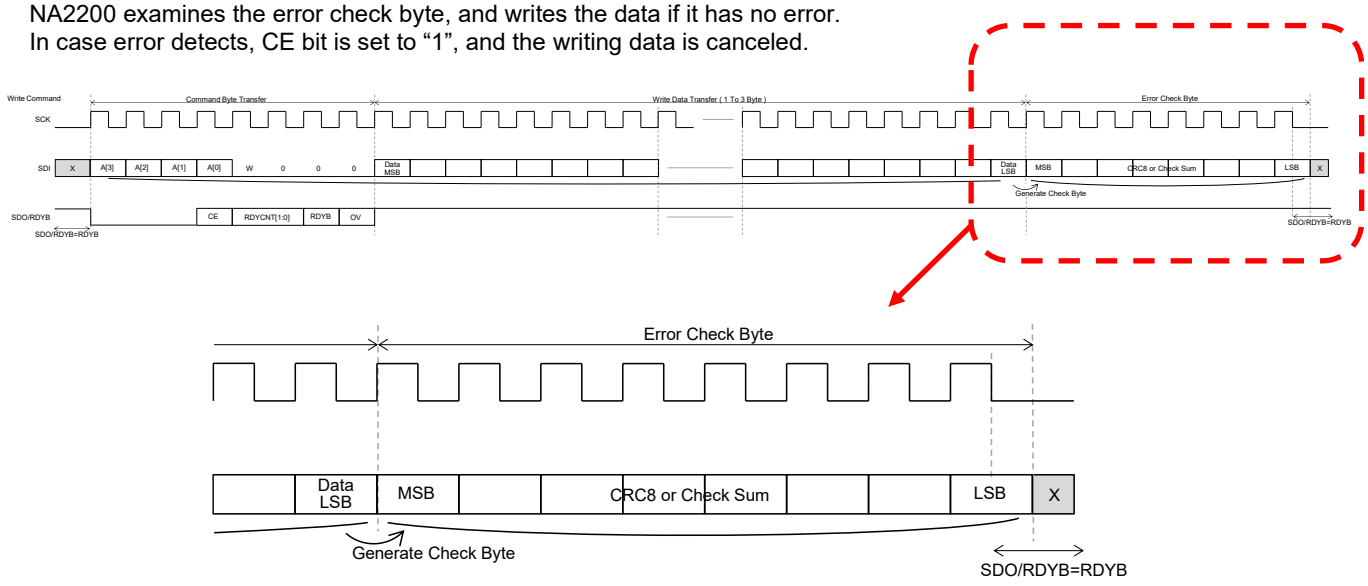
NA2200 outputs the error check byte, after calculating CRC8 or Check Sum from command byte and reading data.
SPI master device such as microprocessor examines error check byte, and please confirm the accuracy of the reading data.



SPI communication format with error check byte: Reading

Write mode

Write the data by adding CRC8 or Check Sum to the command byte and the writing data bytes.
NA2200 examines the error check byte, and writes the data if it has no error.
In case error detects, CE bit is set to “1”, and the writing data is canceled.



SPI communication format with error check byte: Writing

CRC8 mode

Generally, CRC has a stronger error check function than Check Sum, though it has a large MCU source because of a complex calculation.

Error check byte with CRC8 mode is CRC-8-ATM (x^8+x^2+x+1).
Initial value is 0xFF.
In case data has 3 bytes, calculating as follow.

Step	Description
(1)	It takes Ex-OR of “MSB byte of data” and ”Initial value: 0xFF”. (MSB: Most Significant Bit, XOR: Exclusive OR)
(2)	If MSB of the result (1) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (1) is “0”, shift the data 1 bit to the left.
(3)	If MSB of the result (2) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (2) is “0”, shift the data 1 bit to the left.
(4)	Repeat the step (3) six times. (from (2) to (4), shift the data 1 bit to the left eight times)
(5)	It takes XOR of “the result (4)” and ”middle byte of data”.
(6)	If MSB of the result (5) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (5) is “0”, shift the data 1 bit to the left.
(7)	If MSB of the result (6) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (6) is “0”, shift the data 1 bit to the left.
(8)	Repeat the step (7) six times. (from (6) to (8), shift the data 1 bit to the left eight times)
(9)	It takes XOR of “the result (8)” and ”LSB byte of data”. (LSB: Least Significant Bit)
(10)	If MSB of the result (9) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (9) is “0”, shift the data 1 bit to the left.
(11)	If MSB of the result (10) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (10) is “0”, shift the data 1 bit to the left.
(12)	Repeat the step (11) six times. (from (9) to (11), shift the data 1 bit to the left eight times) The calculation of CRC8 is finished.

The calculation method is shown as below.
The below is considered as the calculation method when the writing data is “0x201012”.
(Register Address is set to “0x2”, and writing data is set to “0x1012” in the IEXCONF register.)

Writing data: 00100000 00010000 00010010 (0x201012)
Initial value: 11111111 (0xFF)

Step (1)

MSB of Writing data	00100000	(0x20)
Initial value	11111111	(0xFF)
XOR	11011111	

Step (2)

If MSB of result (1) is “1”, shifts it 1bit to the left	10111110	(1st time)
Polynomial	00000111	
XOR	10111001	

Step (3)

If MSB of result (2) is “1”, shifts it 1bit to the left	01110010	(2nd time)
Polynomial	00000111	
XOR	01110101	

Step (4): Repeat step (3) 6 times.

Shift 1bit to the left	11101010	(3rd time)
If MSB of the above data is “1”, shifts it 1 bit to the left	11010100	(4th time)
Polynomial	00000111	
XOR	11010011	
If MSB of the above data is “1”, shifts it 1 bit to the left	10100110	(5th time)
Polynomial	00000111	
XOR	10100001	
If MSB of the above data is “1”, shifts it 1 bit to the left	01000010	(6th time)
Polynomial	00000111	
XOR	01000101	
Shift 1bit to the left	10001010	(7th time)
If MSB of the above data is “1”, shifts it 1 bit to the left	00010100	(8th time)
Polynomial	00000111	
XOR	00010011	(0x13)

Step (5)

The result (4)	00010011	(0x13)
Middle byte of writing data	00010000	(0x10)
XOR	00000011	

Step (6)

Shift 1bit to the left	00000110	(1st time)

Step (7)

Shift 1bit to the left	00001100	(2nd time)

Step (8): Repeat step (7) 6 times.

Shift 1bit to the left	00011000	(3rd time)		
Shift 1bit to the left	00110000	(4th time)		
Shift 1bit to the left	01100000	(5th time)		
Shift 1bit to the left	11000000	(6th time)		
If MSB of the data is “1”, shifts it 1 bit to the left			10000000	(7th time)
Polynomial	00000111			
XOR	10000111			
If MSB of the data is “1”, shifts it 1 bit to the left			00001110	(8th time)
Polynomial	00000111			
XOR	00001001	(0x09)		

Step (9)

The result (8)	00001001	(0x09)
LSB byte of writing data	00010010	(0x12)
XOR	00011011	

Step (10)

Shift 1bit to the left	00110110	(1st time)

Step (11)

Shift 1bit to the left	01101100	(2nd time)

Step (12): Repeat step (11) 6 times.

Shift 1bit to the left	11011000	(3rd time)		
If MSB of the data is “1”, shifts it 1 bit to the left			10110000	(4th time)
Polynomial	00000111			
XOR	10110111			
If MSB of the data is “1”, shifts it 1 bit to the left			01101110	(5th time)
Polynomial	00000111			
XOR	01101001			
Shift 1bit to the left	11010010			(6th time)
If MSB of the data is “1”, shifts it 1 bit to the left			10100100	(7th time)
Polynomial	00000111			
XOR	10100011			
If MSB of the data is “1”, shifts it 1 bit to the left			01000110	(8th time)
Polynomial	00000111			
XOR	01000001	(0x41)		

The calculation result is “0x41”.
You need add error check byte 0x41 (01000001) with CRC8 mode, if writing data is “0x201012”.

The calculation result is changed because of initial data.
Initial data is 1 byte (8bits), so there are 256 calculation results.

In fact, CPU program calculates error check byte with CRC8.
Initial value is changed as below, error check byte changes.

- Initial value: 0x00 → error check byte: 0x6A
- Initial value: 0x80 → error check byte: 0x61

```
#include <stdio.h>
unsigned char crc8_gen( const unsigned char *buffer, size_t size){
   const unsigned char polynomial = 0x07; /* x^8 + x^2 + x + 1 */
   unsigned char crc = 0xFF; /* CRC initial value = 0xFF */
   unsigned char data;
   int bit_count;
   size_t i=0;

   for ( ; i < size; i++) {
      data = crc ^ *buffer++;
      for ( bit_count = 0; bit_count < 8; bit_count++ ){
         if ( ( data & 0x80 ) != 0 ) {
            data <<= 1;
            data ^= polynomial;
         } else {
            data <<= 1;
         }
      }
      crc =data;
   }
   return crc;
}

int main () {
   unsigned char buffer[3];
   unsigned char crc8;

  /* Example:
        Write 0x1012 to IEXCONF Register.
        Command 0x201012
  */
  buffer[0] = 0x20; /* Command Byte ( Address=2, Write) */
  buffer[1] = 0x10; /* Write Data MS Byte */
  buffer[2] = 0x12; /* Write Data LS Byte */

  crc8 =crc8_gen( buffer, 3 );
  printf( "CRC8 = 0x%02X¥n", crc8 );
  /* Result : CRC8 = 0x41 */

  return 0;
}
```

Check Sum mode

The error check byte added in Check Sum mode is calculated by the following procedure.
In case data is 3 byte, calculating as below.

Step	Description
(1)	Adding MSB byte, Middle byte and LSB byte of the data. Overflow is ignored. MSB: Most Significant Bit, LSB: Least Significant Bit)
(2)	The bits of result (1) inverted (1's complement) is error check byte.

The calculation method is shown as below.
The below is considered as the calculation method when the writing data is "0x201012".
(Register Address is set to "0x2", and writing data is set to "0x1012" in the IEXCONF register.)

Writing data: 00100000 00010000 00010010 (0x201012)

Step (1)

MSB byte	00100000	(0x20)
Middle byte	00010000	(0x10)
LSB byte	00010010	(0x12)
Addition result	01000010	(0x42)

Step (2)

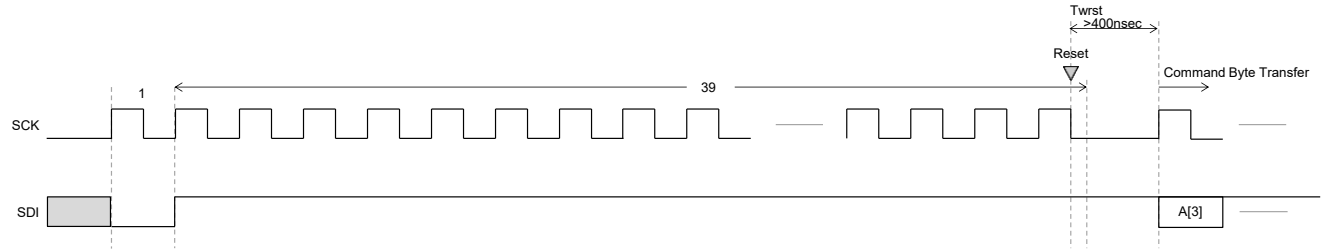
The result of step (1)	01000010	(0x42)
1' complement	10111101	(0xBD)

The calculation result is "0xBD".
You need add error check byte (0xBD) with Check Sum mode, if writing data is "0x201012".

SPI reset command

Transferring SDI=1 continuously for 39 bits after SDI=0 resets the chip.
In normal operation, since there is "0" in the ZERO [1: 0] bits of the SPI command byte, SDI=1 never becomes 39 consecutive bits.

Wait at least 400nsec after reset and transfer the command byte of operation start. 400nsec is the minimum required for internal startup time.

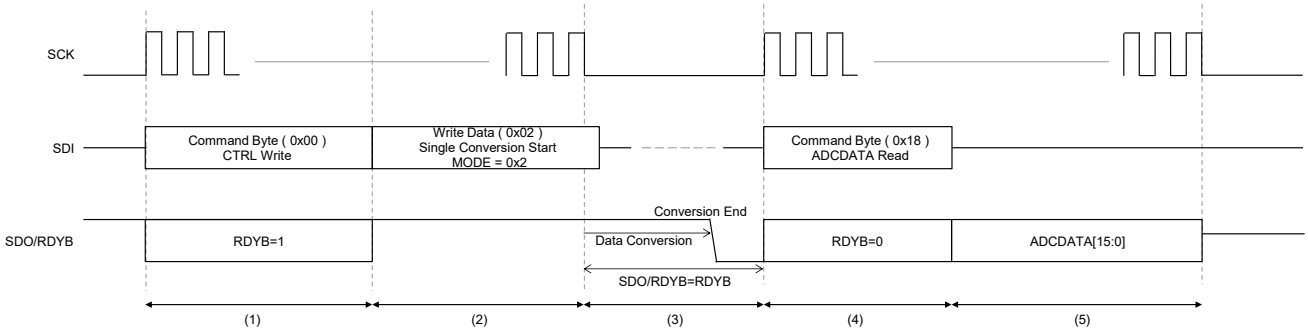


SPI reset command

SPI communication example

< Single conversion >

This is an example of communication with the PGA gain setting implemented. (Processing in the shortest time)



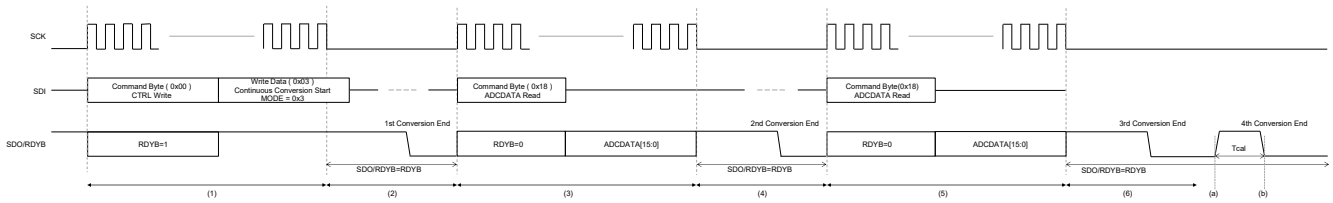
Single conversion example

STEP	DETAILS
(1)	Specify the address "0x0" of the CTRL register.
(2)	Specify single conversion "0x2" (= MODE).
(3)	Performs single conversion. (Conversion time + setup time + data correction time (= 1 / DR + T_s + T_{cal}))
(4)	Specify the ADCDATA register (0x1).
(5)	Read the conversion data (ADCDATA register).

The table below shows the time when CLKDIV = 0 and the operation clock of SPI is 5 Mbps.
It is understood that the time of SPI communication << conversion time.

OSR	Conversion time (1/DR+T_s+T_{cal}) [µsec]	SPI communication time ((1)+(2)+(4)+(5)) [µsec]
512	1255	8 (= 1/(5[Mbit/s]) x 5[byte] x 8[bit/byte])
256	640	
128	333	
64	180	

< Continuous conversion >



Continuous conversion example

STEP	DETAILS
(1)	Specify the address "0x0" of the CTRL register and specify continuous conversion "0x3" (= MODE).
(2)	Perform continuous conversion (first time). After conversion, SDO / RDYB changes from "1" to "0".
(3)	Specify the address "0x1" of the ADCDATA register. SDO / RDYB changes from "0" to "1" when conversion data (ADCDATA register) is read.
(4)	Perform continuous conversion (second time). After conversion, SDO / RDYB changes from "1" to "0".
(5)	Specify the address "0x1" of the ADCDATA register. SDO / RDYB changes from "0" to "1" when conversion data (ADCDATA register) is read.
(6)	Perform continuous conversion (third time). After conversion, SDO / RDYB changes from "1" to "0".
(7)	:

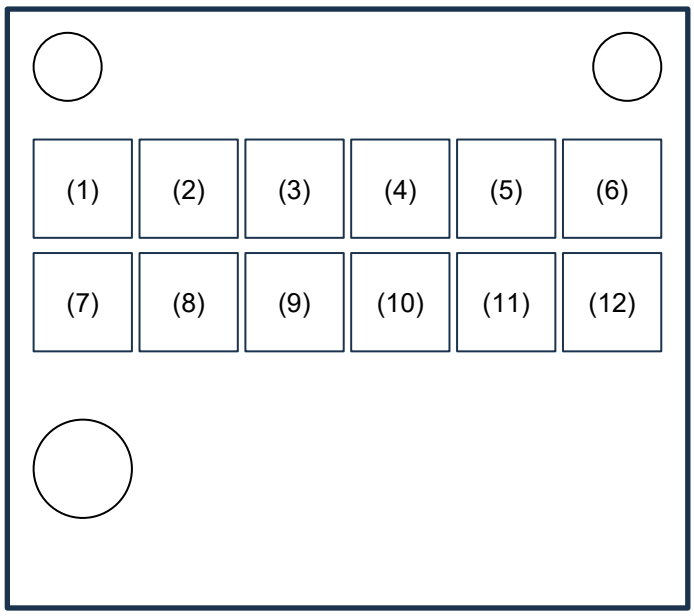
SDO / RDYB is kept "0" when reading the third conversion result is not performed.
If reading is not performed, it operates as follows.

(a) SDO / RDYB changes from "0" to "1" when the fourth AD conversion before data correction ends.
(b) After the data correction time (T_{cal}), SDO / RDYB changes from "1" to "0".

At the point (a) above, the third conversion data is discarded.
If conversion data (ADCDATA register) is not read before the next (a) comes, the fourth data is also discarded. In order to read data safely, it is necessary to read the conversion data before (a) comes.

■ MARKING SPECIFICATION (SSOP-16-BD)

(1)(2)(3)(4)(5)(6)(7) Product Code Refer to *Part Marking List*
(8) to (12) Control Number



1Pin

Part Marking List（SSOP-16-BD）

Product Name	(1)	(2)	(3)	(4)	(5)	(6)	(7)
NA2200BDAE2S	A	2	2	0	0	A	S

NOTICE

There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

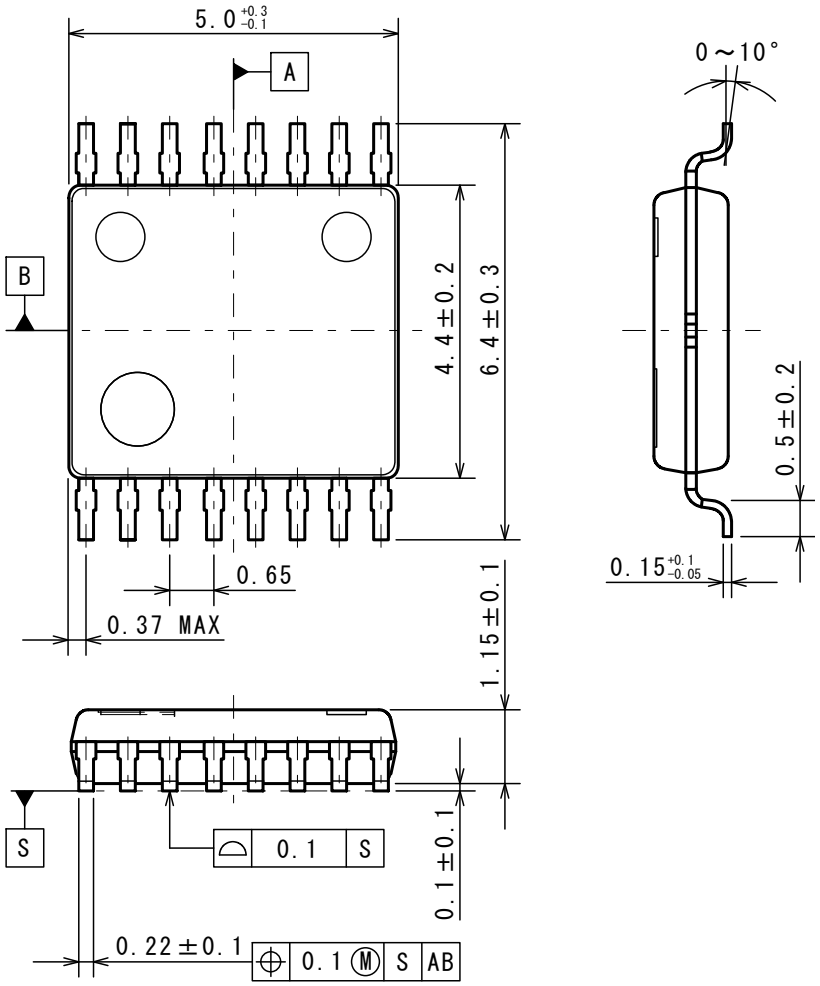
Nisshinbo Micro Devices Inc.

SSOP-16-BD

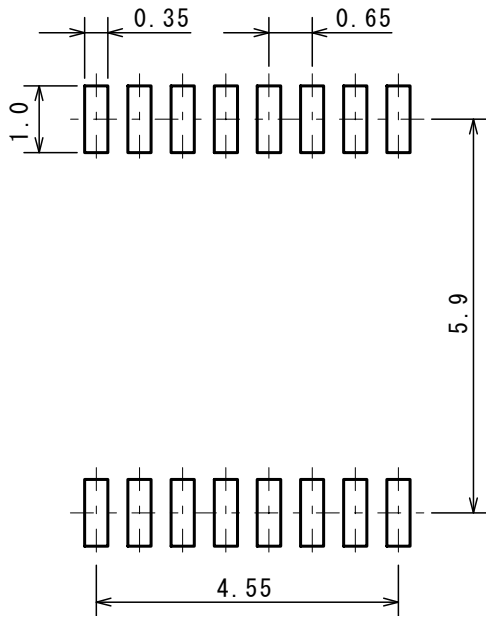
PI-SSOP-16-BD-E-A

■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS



Nisshinbo Micro Devices Inc.

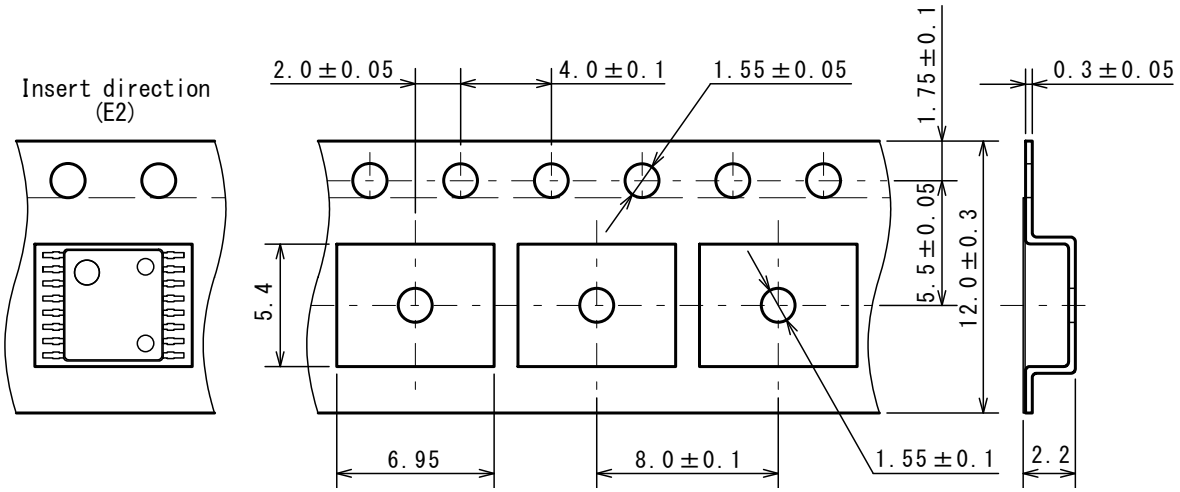
SSOP-16-BD

PI-SSOP-16-BD-E-A

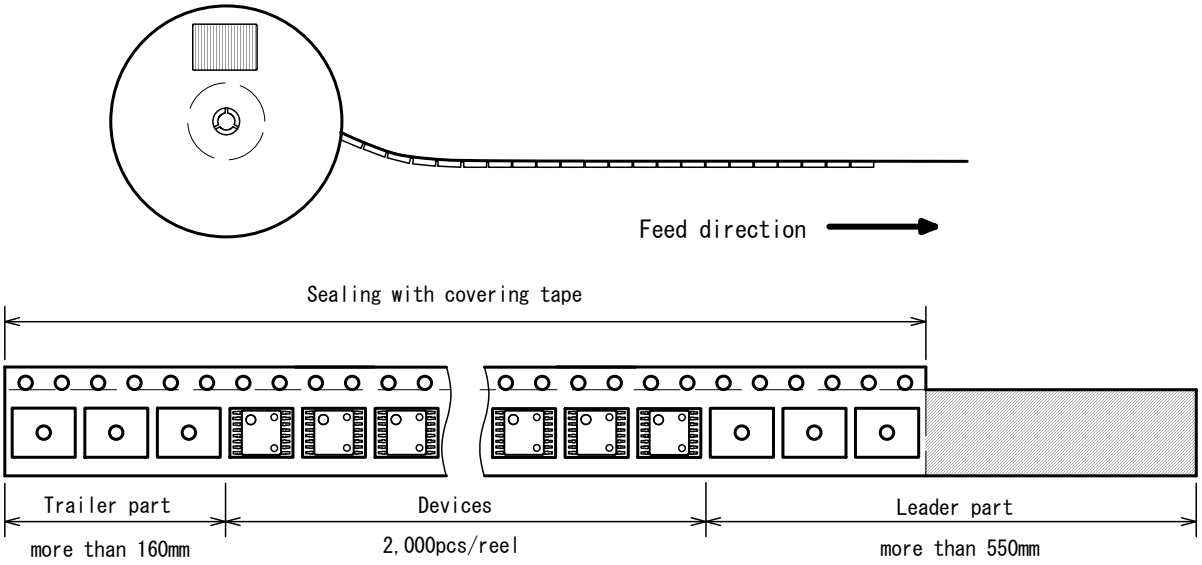
■ PACKING SPEC

UNIT: mm

(1) Taping dimensions / Insert direction



(2) Taping state

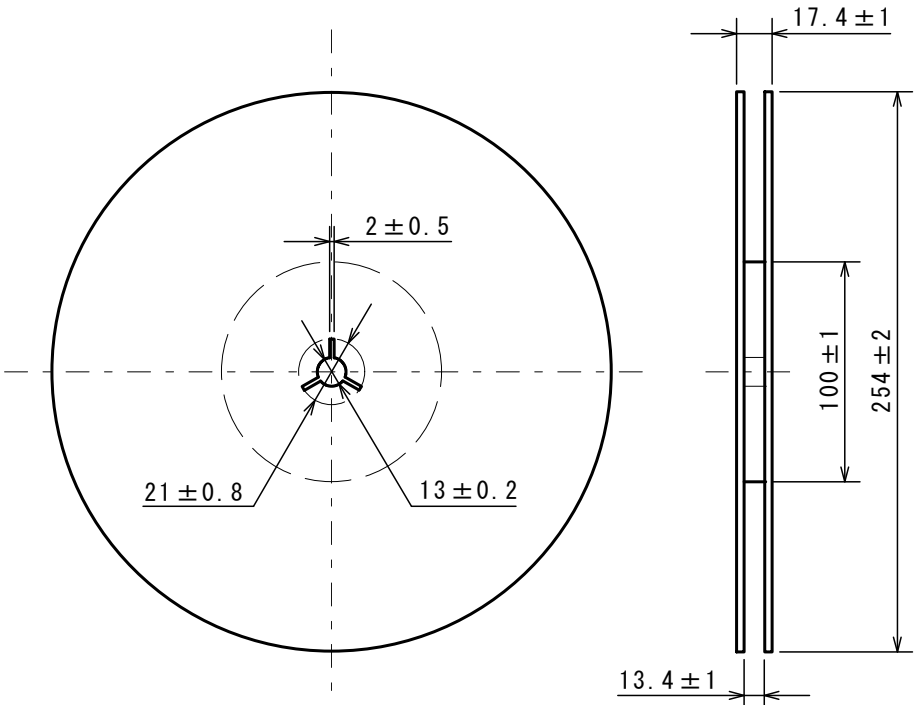


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SSOP-16-BD

PI-SSOP-16-BD-E-A

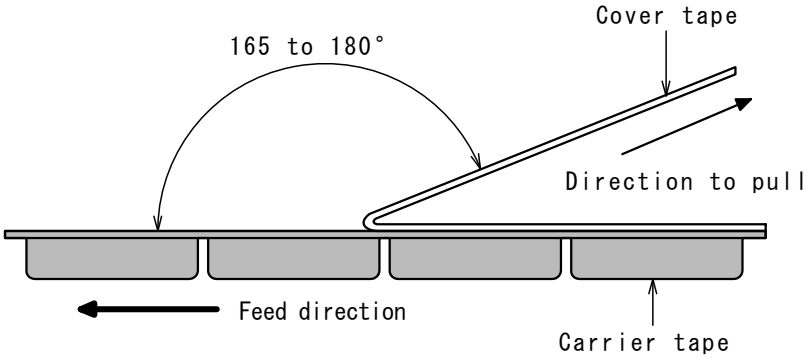
(3) Reel dimensions



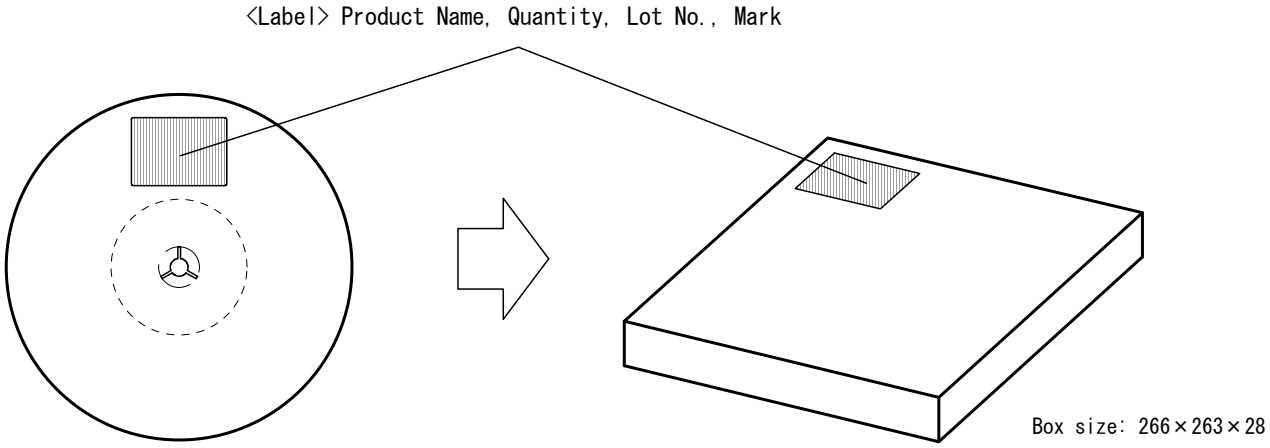
(4) Peeling strength

Peeling strength of cover tape

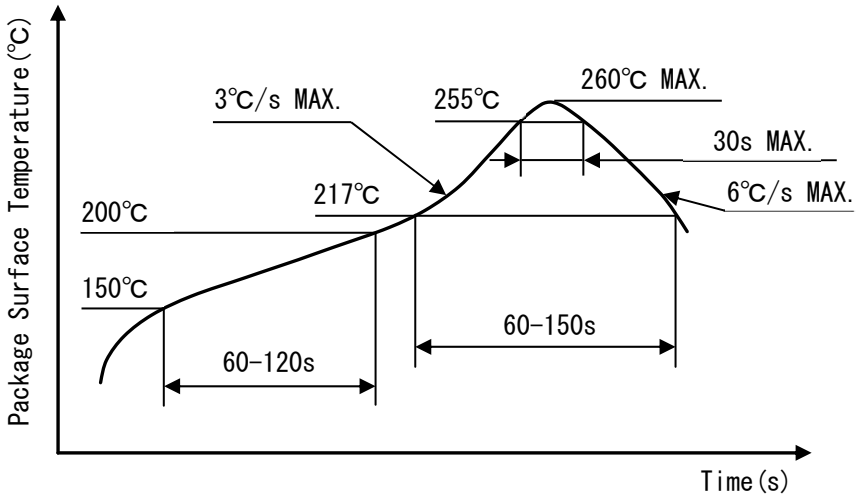
・Peeling angle	165 to 180° degrees to the taped surface.
・Peeling speed	300mm/min
・Peeling strength	0.1 to 1.3N



(5) Packing state



■ **HEAT-RESISTANCE PROFILES**



Reflow profile

■ REVISION HISTORY

Date	Revision	Changes
May 23, 2024	Ver. 1.0	Initial release Datasheet
2025/06/25	Ver. 1.1	Analog to Digital Converter -> Analog to Digital Converter(ADC) Package height correction Added note about NC terminals Order information: Quantity/reel -> Quantity

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    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
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