Quad Sine-Wave Clock Buffer With LDO

Check for Samples: CDC3S04

FEATURES

- **1:4 Low-Jitter Clock Buffer**
- **Single-Ended Sine-Wave Clock Input and Outputs**
- **Ultralow Phase Noise and Standby Current**
- **Individual Clock Request Inputs for Each Output**
- **On-Chip Low-Dropout Output (LDO) for Low-Noise TCXO Supply**
- **Serial I^2C Interface (Compatible With High-Speed Mode, 3.4 Mbit/s)**
- **1.8-V Device Power Supply**
- **Wide Temperature Range, –40°C to 85°C**
- **ESD Protection: 2 KV HBM, 750 V CDM, and 100 V MM**
- **Small 20-Pin Chip-Scale Package: 0.4-mm Pitch WCSP (1.6 mm × 2 mm)**

APPLICATIONS

- **Cellular Phones**
- **Smart Phones**
- **Mobile Handsets**
- **Portable Systems**
- **Wireless Modems Including GPS, WLAN, W-BT, D-TV, DVB-H, FM Radio, WiMAX, and System Clock**

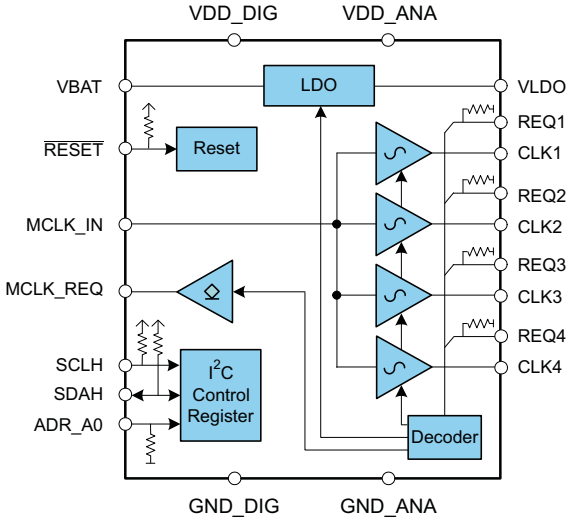
DESCRIPTION

The CDC3S04 is a four-channel low-power low-jitter sine-wave clock buffer. It can be used to buffer a single master clock to multiple peripherals. The four sine-wave outputs (CLK1–CLK4) are designed for minimal channel-to-channel skew and ultralow additive output jitter.

Each output has its own clock request inputs which enables the dedicated clock output. These clock requests are active-high (can also be changed to be active-low via I^2C), and an output signal is generated that can be sent back to the master clock to request the clock (MCLK_REQ). MCKL_REQ is an open-source output and supports the wired-OR function (default mode). It needs an external pulldown resistor. MCKL_REQ can be changed to wired-AND or push-pull functionality via I^2C.

The CDC3S04 also provides an I^2C interface (Hs-mode) that can be used to enable or disable the outputs, select the polarity of the REQ inputs, and allow control of internal decoding.

The CDC3S04 features an on-chip high-performance LDO that accepts voltages from 2.3 V to 5.5 V and outputs a 1.8-V supply. This 1.8-V supply can be used to power an external 1.8-V TCXO. It can be enabled or disabled for power saving at the TCXO.



WCSP

	1	2	3	4
A	REQ2	CLK2	REQ1	CLK1
B	MCLK_ IN	RESET	VDD_ ANA	GND_ ANA
C	REQ4	CLK4	REQ3	CLK3
D	VDD_ DIG	GND_ DIG	MCLK_ REQ	ADR_ A0
E	VLDO	VBAT	SDAH	SCLH

Top View
(Solder Ball Underneath)

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

A low signal at the $\overline{\text{RESET}}$ input switches the outputs CLK1 and CLK4 into the default state. In this configuration, CLK1 and CLK4 are ON (see Table 1); the remaining device function is not affected. Also, the $\overline{\text{RESET}}$ input provides a glitch filter which rejects spikes of typical 300 ns on the $\overline{\text{RESET}}$ line to preserve false reset. A complete device reset to the default condition can be initiated by a power-up cycle of V_{DD_DIG}.

The CDC3S04 operates from two 1.8-V supplies. There is a core supply (VDD_DIG/GND_DIG) for the core logic and a low-noise analog supply (VDD_ANA/GND_ANA) for the sine-wave outputs. The CDC3S04 is designed for sequence-less power up. Both supply voltages may be applied in any order.

The CDC3S04 is offered in a 0.4-mm pitch WCSP package (1.6 mm × 2 mm) and is optimized for low standby current (0.5 µA). It is characterized for operation from –40°C to 85°C.

DEVICE INFORMATION

PIN FUNCTIONS

NAME	BALL NO.	TYPE	FUNCTION
ADR_A0	D4	Input	Selectable address bit A0 of slave-address register; internal 500-kΩ pulldown resistor
CLK1	A4	Output	Clock output 1
CLK2	A2	Output	Clock output 2
CLK3	C4	Output	Clock output 3
CLK4	C2	Output	Clock output 4
GND_ANA	B4	Ground	Ground for sine-wave buffer
GND_DIG	D2	Ground	Ground for core logic
MCLK_IN	B1	Input	Master clock input
MCLK_REQ	D3	Output	Clock request to the master clock source; active-high; open-source output for wired-OR connection (default condition). Can be changed to push-pull output or wired-AND output via I^2C.
REQ1	A3	Input	Clock request from peripheral 1; internal 500-kΩ pulldown resistor
REQ2	A1	Input	Clock request from peripheral 2; internal 500-kΩ pulldown resistor
REQ3	C3	Input	Clock request from peripheral 3; internal 500-kΩ pulldown resistor
REQ4	C1	Input	Clock request from peripheral 4; internal 500-kΩ pulldown resistor
$\overline{\text{RESET}}$	B2	Input	Peripheral reset signal provided by application processor. The signal is active-low and switches CLK1 and CLK4 outputs to ON (see Table 1). On-chip LDO is enabled. Internal 1-MΩ pullup resistor and 300-ns (typ) glitch filter.
SCLH	E4	Input	I^2C clock input – Hs-mode. Internal 1-MΩ pullup resistor
SDAH	E3	Input/output	I^2C data input/output – Hs-mode. Internal 1-MΩ pullup resistor
VBAT	E2	Power	Supply pin to internal LDO
VDD_ANA	B3	Power	1.8-V power supply for sine-wave buffer
VDD_DIG	D1	Power	1.8-V power supply for core logic. Power up of VDD_DIG resets the whole device to the default condition.
VLDO	E1	Output	1.8-V supply for external TCXO; LDO is enabled if $\overline{\text{RESET}}$ (default mode) or REQx is active. LDO is not enabled if only VBAT is on.

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FUNCTION SELECTION TABLES

Table 1. Reset and Request (REQx) Conditions for Clock Outputs(1)

$\overline{\text{RESET}}$(2)	PRIORITY BIT(3)	CLK1	CLK2	CLK3	CLK4
0	0	On	Controlled by REQ2	Controlled by REQ3	On
	1		Controlled by REQ2INT	Controlled by REQ3INT	
1	0	Controlled by REQ1	Controlled by REQ2	Controlled by REQ3	Controlled by REQ4
	1	Controlled by REQ1INT	Controlled by REQ2INT	Controlled by REQ3INT	Controlled by REQ4INT

(1) Shaded cells show the default setting after power up.
(2) $\overline{\text{RESET}}$ resets REQ1PRIO/REQ4PRIO and REQ1INT/REQ4INT bits to their default values (CLK1/4 is ON) but does not change the remaining internal SW bits. During $\overline{\text{RESET}}$, any I^2C operation is blocked until $\overline{\text{RESET}}$ is deactivated. A minimum pulse duration of 500 ns must be applied to activate $\overline{\text{RESET}}$ (the internal glitch-filter suppresses spikes of typical 300 ns).
(3) Priority bit defines if the external control pins (HW controlled) or the SW bits (SW controlled) have priority. It can be set in the configuration register, Byte 2, Bits 0–3.

Table 2. Request Signal Condition for Clock Outputs(1)

REQ-Signals(2)	REQx (REQ1/2/3/4)	CLKx (CLK1/2/3/4)	MCLK_REQ	LDO(3)
Active-low	0	Clock	High	On
	1	Disabled to high	Low (if all REQx are high)	Off (if all REQx are high)
Active-high	0	Disabled to high(4)	Low (if all REQx are low)	Off (if all REQx are low)
	1	Clock(4)	High	On

(1) Shaded cells show the default setting after power up.
(2) Polarity of REQ1, REQ2, REQ3, and REQ4 are register-configurable via I^2C (see Table 3, Byte 0, Bits 0–3). Default setting is active-high.
(3) The LDO is controlled by an on-chip decoder, but can also be SW controlled (see Table 3, Byte 2, Bits 4–5).
(4) CLK1 and CLK4 are ON after device power up (default condition). CLK2 and CLK3 are controlled by external REQ2 and REQ3, respectively.

POWER GROUPS

NAME	DESCRIPTION
VBAT	Supply pin for LDO provided by main battery. LDO is not working if only VBAT is on.
VLDO	1.8-V low-drop output voltage for external TCXO. LDO is enabled if VBAT and VDD_DIG are on and REQx or $\overline{\text{RESET}}$ is active (see Table 2).
VDD_DIG	1.8-V power supply for core logic and I^2C logic. VDD_DIG must be supplied for correct device operation. Power up of VDD_DIG resets the whole device to the default condition.
VDD_ANA	1.8-V power supply for sine-wave buffers. For correct sine-wave buffer function, all three power supplies (VBAT, V_{DD_DIG} and V_{DD_ANA}) must be on. But, V_{DD_ANA} can be switched on and off at any time. If off, the sine-wave outputs are switched to high-impedance.

POWER-UP SEQUENCE

The CDC3S04 is designed for sequence-less power up. VBAT, V_{DD_DIG}, and V_{DD_ANA} may be applied in any order. Recommended power-on sequence is VBAT first, followed by V_{DD_DIG} and V_{DD_ANA}. Recommended power-off sequence is in reverse order.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_{DD_ANA} V_{DD_DIG}	Supply voltage range	–0.5 to 2.5	V
V_{BAT}	Battery supply voltage range	–0.5 to 6.5	V
V_I	Input voltage range (2) (3)	–0.5 to V_{DD} + 0.5	V
V_O	Output voltage range (2) (3)	–0.5 to V_{DD} + 0.5	V
V_{LDO}	Output voltage range	–0.5 to V_{BAT} + 0.5	V
	Input current (V_I < 0, V_I > V_{DD})	±20	mA
I_O	Continuous output current	±20	mA
I_{LDO}	Continuous output current	±20	mA
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The input V_I and output V_O positive voltages are limited to the absolute maximum rating for V_{DD} = 2.5 V.

THERMAL CHARACTERISTICS for 20-pin WCSP (YFF) (1)

PARAMETER		AIRFLOW (lfm)	20-PIN WCSP	UNIT
T_{JA}	Thermal resistance, junction-to-ambient	0	71	°C/W
		200	62	
		400	59	
T_{JC}	Thermal resistance, junction-to- case	–	17.5	°C/W
T_{JB}	Thermal resistance, junction-to-board	–	20.5	°C/W
T_J	Maximum junction temperature	–	125	°C

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD_ANA}	Device supply voltage	1.65	1.8	1.95	V
V_{DD_DIG}	Device supply voltage	1.65	1.8	1.95	V
V_{IH}	Input voltage ADR_A0, REQx, $\overline{RESET}$	0.65 V_{DD_DIG}			V
V_{IL}				0.35 V_{DD_DIG}	V
V_{IS}	Sine-wave input voltage – MCLK_IN; ac-coupled amplitude	0.5		1.2	V_{PP}
C_L	Sine-wave output load (1)		10	30	pF
C_{OUT}	LDO output capacitance (stabilize the internal control loop)	0.8	2.2		µF
T_A	Operating free-air temperature	–40		85	°C

(1) 10 pF is the typical load-driving capability. The drive capability can be optimized for 30 pF by the I^2C register (Byte 3, Bits 7–4).

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OVERALL PARAMETER							
I_{DD_ANA}	Analog supply current(1) (seeFigure 8 through Figure 12)	V_{BAT} = 5.5 V; V_{DD_ANA} = 1.95 V; LDO is on; V_{IS} = 1 V_{PP}; f_{MCLK_IN} = 38.4 MHz; R_L = 10 kΩ; C_L = 10 pF(2)	Off (no REQ)		0.1	0.2	mA
			Per output		2	2.6	
I_{DD_DIG}	Digital supply current (see Figure 8 through Figure 12)	V_{BAT} = 5.5 V; V_{DD_DIG} = 1.95 V; V_{DD_ANA} = off; LDO = off; V_{IS} = 1 Vpp; f_{MCLK_IN} = 38.4 MHz; C_L= 10 pF; R_L= 10 kΩ				0.1	mA
I_{SB}	Standby current	V_{BAT} = 5.5 V; V_{DD_DIG}/V_{DD_ANA} = 1.95 V; All outputs disabled (no input clock; LDO off; no REQ; $\overline{RESET}$ is inactive; I^2C is in idle mode); includes 1-MΩ pullup at I^2C and $\overline{RESET}$			0.5	10	µA
f_{MCLK_IN}	Input frequency	Sine wave		0.01	38.4	52	MHz
V_{OH}	MCLK_REQ high-level output voltage	Wired-OR output; I_{OH} = –2 mA; V_{DD_DIG} = 1.65 V (See Figure 3.)		V_{DD_DIG} – 0.45			V
		Push-pull output; V_{DD_DIG} = 1.65 V, I_{OH} = –2 mA		V_{DD_DIG} – 0.45			
V_{OL}	MCLK_REQ low-level output voltage	Wired-AND output; I_{OL} = 2 mA V_{DD_DIG} = 1.65 V				0.45	V
		Push-pull output; V_{DD_DIG} = 1.65 V, I_{OL} = 2 mA				0.45	
V_{IK}	LVCMOS input voltage	V_{DD_DIG} = 1.65 V; I_I = –18 mA				–1.2	V
I_{IH}	Input current ADR_A0, REQx (500-kΩ pulldown)	V_I = V_{DD_DIG}; V_{DD_DIG} = 1.95 V				6	µA
	Input current $\overline{RESET}$ (1-MΩ pullup)					2	
I_{IL}	Input current ADR_A0, REQx (500-kΩ pulldown)	V_I = 0 V; V_{DD_DIG} = 1.95 V				–2	µA
	Input current $\overline{RESET}$ (1-MΩ pullup)					–3	
C_I	Input capacitance ADR_A0, REQx, $\overline{RESET}$	V_I = 0 V or V_{DD_DIG}			3		pF
SDAH/SCLH PARAMETER (Hs-Mode)							
V_{IK}	SCLH/SDAH input clamp voltage	V_{DD_DIG} = 1.65 V; I_I = –18 mA				–1.2	V
I_I	SCLH/SDAH input current	0.1 V_{DD_DIG} < V_I < 0.9 V_{DD_DIG}				10	µA
V_{IH}	SDA/SCL input high voltage			0.7 V_{DD_DIG}			V
V_{IL}	SDAH/SCLH input low voltage					0.3 V_{DD_DIG}	V
V_{hys}	Hysteresis of Schmitt-trigger inputs			0.1 V_{DD_DIG}			V
V_{OL}	SDAH low-level output voltage	I_{OL} = 3 mA, V_{DD_DIG} = 1.65 V				0.2 V_{DD_DIG}	V
C_I	SCLH input capacitance	V_I = 0 V or V_I = V_{DD_DIG}(3)			3	5	pF
	SDAH input capacitance	V_I = 0 V or V_I = V_{DD_DIG}(3)			8	10	

(1) The total current consumption when no output is active is calculated by I_{DD_ANA}(off) + I_{DD_DIG}.
(2) For C_L = 30 pF, the typical current for one output is 2.2 mA (see Figure 8).
(3) The I^2C standard specifies a maximum C_I of 10 pF.

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ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SINE-WAVE PARAMETER (MCLK_IN is sine-wave signal, C_L = 10 pF)							
f_{OUT}	Output frequency					52	MHz
V_{OS}	Output gain level (see Figure 17)	MCLK_IN-to-CLKx; 10 kΩ, 10 pF; ac-coupled; f_{MCLK_IN} > 1 MHz	0.5 ≤ V_{IS} ≤ 1.2 V_{PP}	–1	–0.3	0	dB
	Output voltage		V_{IS} = 0.5 V_{PP}	445	490	500	mV_{PP}
$t_{jitadd(rms)}$	Additive rms jitter(4)	10 Hz to 10 MHz; f_{OUT} = 38.4 MHz			0.3	0.6	ps_{RMS}
		10 kHz to 10 MHz; f_{OUT} = 38.4 MHz			0.1	0.2	
pn_{add}	Additive phase noise at f_{OUT} = 38.4 MHz(5)	At offset = 1 kHz			–142	–135	dBc/Hz
		At offset = 10 kHz			–152	–145	
		At offset = 100 kHz			–157	–150	
R_{IN}	Input resistance	At dc level		12	15		kΩ
C_{IN}	Input capacitance	f_{MCLK_IN} = 38.4 MHz			5	7	pF
ELECTRICAL CHARACTERISTIC of LDO (C_{OUT} = 0.8 to 2.7 µF)(6)							
V_{BAT}	Input voltage range			2.3		5.5	V
V_{LDO}	LDO output voltage(7)	2.3 V < V_{BAT} < 5.5 V, I_{LOAD} = 5 mA		1.72	1.8	1.9	V
ΔV_{LDO}	Maximum line regulation	2.3 V < V_{BAT} ≤ 5.5 V, I_{LOAD} = 5 mA			0.5%		
	Maximum load regulation	0 < I_{LOAD} < 5 mA, V_{BAT} = 2.3 V or 5.5 V; T_J = 25°C			0.5%		
I_{LOAD}	Load current	C_{OUT} = 0.8 µF to 2.7 µF		0	5		mA
I_{LCL}	LDO output current limit	V_{LDO} = 0.9 × $V_{LDO(TYP)}$		10		60	mA
I_{LGND}	LDO ground pin current(8)	V_{BAT} = 3.6 V; 0 < I_{LOAD} < 5 mA			50	150	µA
I_{LSHDN}	LDO shutdown current	2.3 V < V_{BAT} < 5.5 V				0.2	µA
PSRR	Power-supply rejection ratio (ripple rejection) (see Figure 20)	V_{BAT} = 2.3 V (for min) V_{BAT} = 2.5 V (for typ) V_{LDO} = 1.8 V I_{LOAD} = 5 mA V_{ripple} = 0.1 Vpp	100 Hz	60	68		dB
			1 kHz	55	62		
			10 kHz	45	52		
			100 kHz	33	40		
			1 MHz	37	46		
			10 MHz	60	67		
V_N	Output noise voltage (see Figure 21)	BW = 10 Hz to 100 kHz; V_{LDO} = 1.8 V; I_{LOAD}= 5 mA				30	μV_{RMS}

(4) Additive rms jitter is the integrated rms jitter that the device adds to the signal chain. It is calculated by $t_{jitadd(rms)} = \sqrt{(t_{jitout(rms)}^2 - t_{jitin(rms)}^2)}$. Specified with the supply ripple noise of 30 µV(rms) from 10 Hz to 100 kHz.

(5) Additive phase noise is the amount of phase noise that the device adds to the signal chain. It is calculated by L_{add} (dB) = 10 log ($10^{0.1\ Lout} - 10^{0.1\ Lin}$).

(6) Minimum C_{OUT} should be 100 nF to allow for stable LDO operation.

(7) LDO output voltage includes maximum line and load regulation.

(8) LDO ground pin current does not change over V_{BAT}.

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TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted) V_{LDO} = 1.8 V; C_L = 10 pF; R_L = 10 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TIMING PARAMETER						
t_{PD}	Propagation delay time	MCLK_IN-to-CLKx; f_{MCLK_IN} = 38.4 MHz			3	ns
t_{LH}	Propagation delay time, low-to-high	REQx-to-MCLK_REQ (wired-OR, C_L= 15 pF, R_L= 10 kΩ);			15	ns
t_{CLK}(2)	CLKx on-time – REQ-to-CLKx	f_{MCLK_IN} = 38.4 MHz; V_{VDD_ANA} is on; V_{IS} = 1 V; V_{OS} = –1 dB (see Figure 5 and Figure 6)		0.3	0.4	µs
	CLKx on-time – $\overline{\text{RESET}}$-to-CLKx(3)			0.6	0.8	µs
	CLKx off-time – REQ-to-CLKx				25	ns
	CLKx on-time – V_{DD_ANA} to-CLKx	f_{MCLK_IN} = 38.4 MHz ; V_{IS} = 1 V; V_{OS} = –1 dB; measurement starts when V_{DD_ANA} is 90% of 1.7 V (see Figure 7)		20	50	µs
t_{SP}	Pulse duration of spikes that must be suppressed by the input filter for $\overline{\text{RESET}}$ (3)				100	ns
$t_{sk(o)}$	Output skew(4)	f_{MCLK_IN} = 38.4 MHz; CLK1-to-CLK4		25	50	ps
t_{LDO}	LDO on-time(5) – REQ-to-LDO; – $\overline{\text{RESET}}$-to-LDO	V_{LDO} = 1.7 V, I_{LDO} = 5 mA, 2.3 V < V_{BAT} < 5.5 V; C_{OUT} = 2.7 µF		100	300	µs

(1) All typical values are at nominal V_{DD_ANA} and V_{DD_DIG}.
(2) CLK on-time is measured with valid input signal (V_{IS} = 1 Vpp). In case a TXCO is used, the LDO and TCXO are already on.
(3) Pulses above 500 ns are interpreted as a valid reset signal. Total time from $\overline{\text{RESET}}$-to-CLKx is the sum of t_{SP} + $t_{CLK_/RESET}$.
(4) Output skew is calculated as the greater of the difference between the fastest and the slowest t_{PLH} or the difference between the fastest and the slowest t_{PHL}.
(5) LDO off-time depends on the discharge time of the R-C components (seeFigure 4).

PARAMETER		MIN	MAX	UNIT
SDAH/SCLH TIMING REQUIREMENTS, Hs-Mode (C_{BUS} = 100 pF for each I^2C line; see Figure 24 and Figure 25)				
f_{SCLH}	SCLH clock frequency	0	3.4	MHz
$t_{su(START)}$	START setup time (SCLH high before SDAH low)	160		ns
$t_{h(START)}$	START hold time (SCLH low after SDAH low)	160		ns
t_{LOW}	Low period of the SCLH clock	160		ns
t_{HIGH}	High period of the SCLH clock	60		ns
$t_{h(SDAH)}$	SDAH hold time (SDAH valid after SCLH low)	0(1)	70	ns
$t_{su(SDAH)}$	SDAH setup time	10		ns
t_r	SCLH rise time	10	40	ns
	SDAH rise time	10	80	
t_f	SCLH fall time	10	40	ns
	SDAH fall time	10	80	
$t_{su(STOP)}$	STOP setup time	160		ns
t_{SP}	Pulse duration of spikes that must be suppressed by the input filter for SDAH and SCLH	0	10	ns

(1) A device must internally provide a data hold time to bridge the undefined period between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

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PARAMETER MEASUREMENT INFORMATION

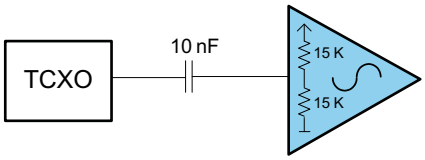


Figure 1. Input Circuit

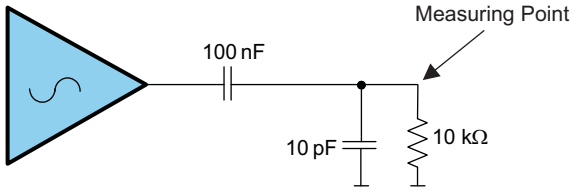


Figure 2. Output Circuit

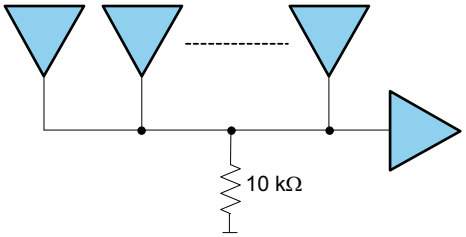
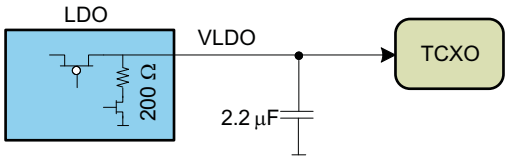


Figure 3. Wired OR



i.e. time constant(RxC) is 440 µs for 63% discharge.

Figure 4. LDO Output Circuit

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TYPICAL CHARACTERISTICS

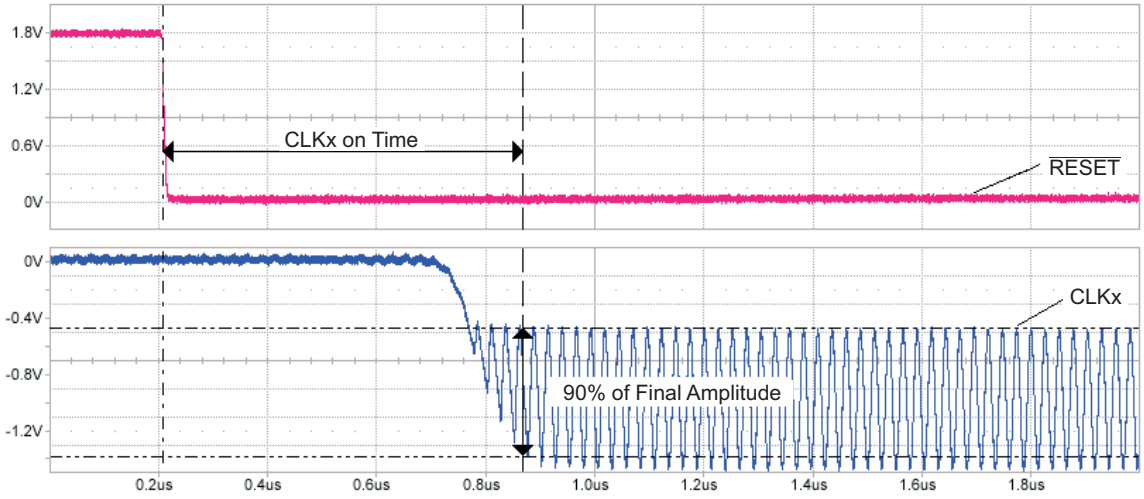

Figure 5. CLKx On-Time From $\overline{\text{RESET}}$ Off-to-On

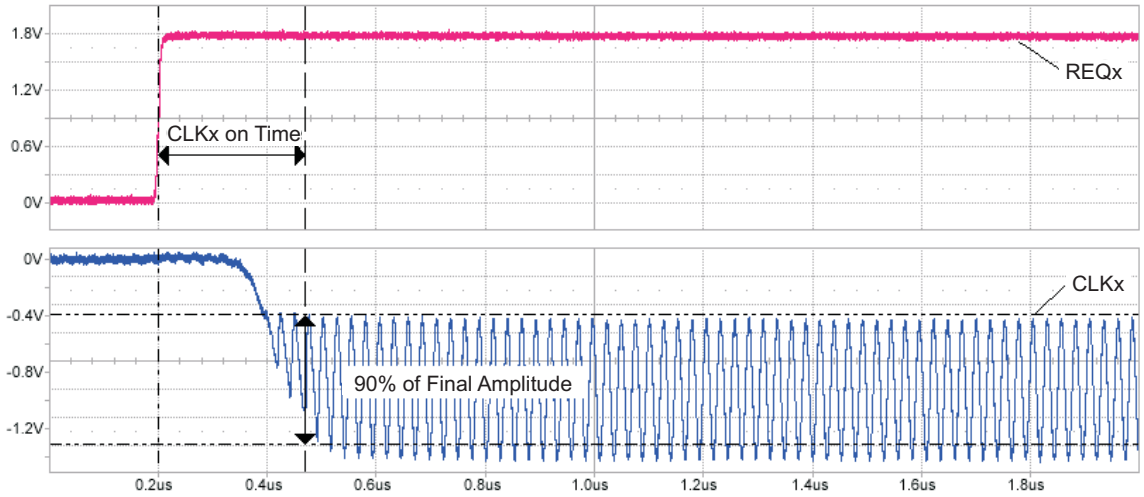

Figure 6. CLKx On-Time From REQ Off-to-On

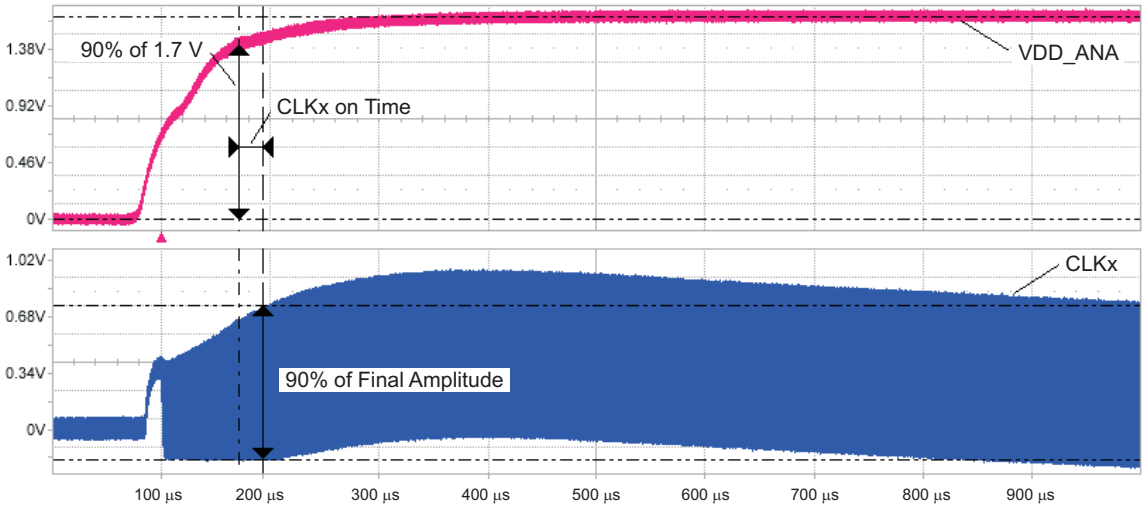

Figure 7. CLKx On-Time From V_{DD_ANA} Off-to-On

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT (IDD_ANA, IDD_DIG)
vs
OUTPUT LOAD (CL) AT 38.4 MHz INPUT CLOCK

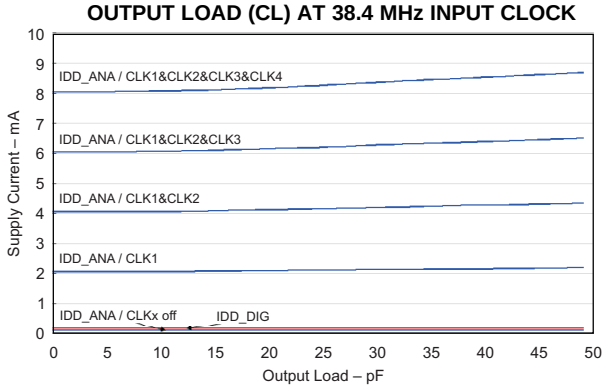

Figure 8.

SUPPLY CURRENT (IDD_ANA, IDD_DIG)
vs
OUTPUT LOAD (CL) AT 26 MHz INPUT CLOCK

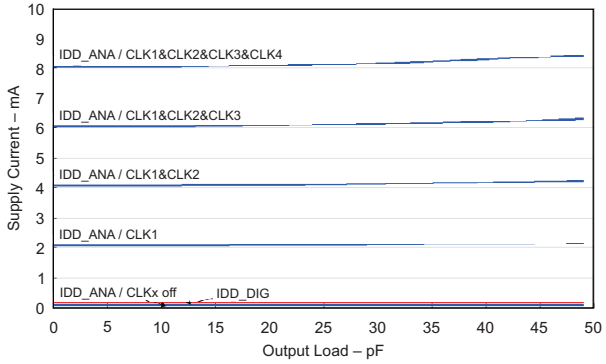

Figure 9.

SUPPLY CURRENT (IDD_ANA, IDD_DIG)
vs
INPUT FREQUENCY (MCLK_IN)

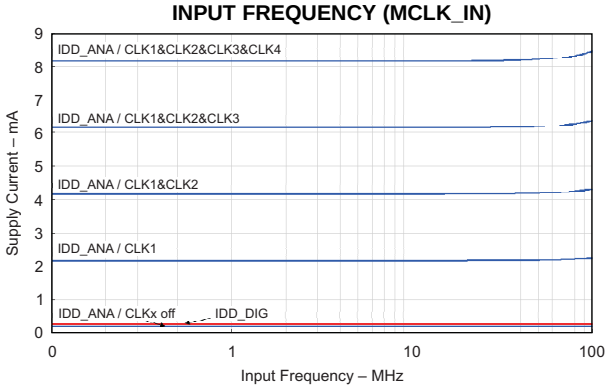

Figure 10.

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TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT (IDD_ANA, IDD_DIG)
vs
INPUT VOLTAGE LEVEL AT 38.4 MHz INPUT CLOCK

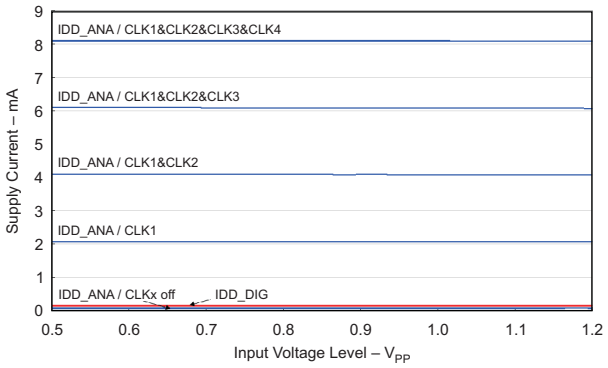

Figure 11.

SUPPLY CURRENT (IDD_ANA, IDD_DIG)
vs
INPUT VOLTAGE LEVEL AT 26 MHz INPUT CLOCK

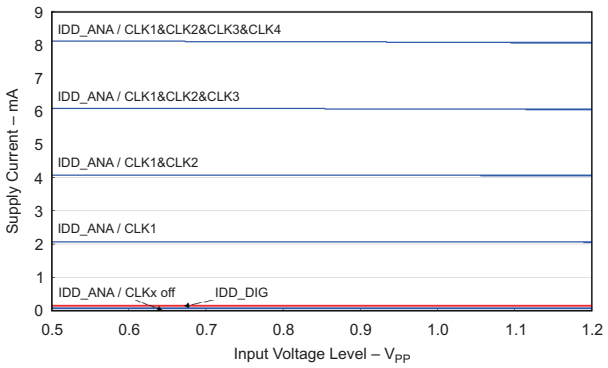

Figure 12.

TCXO INPUT CLOCK
vs
OUTPUT CLOCK AT 38.4 MHz

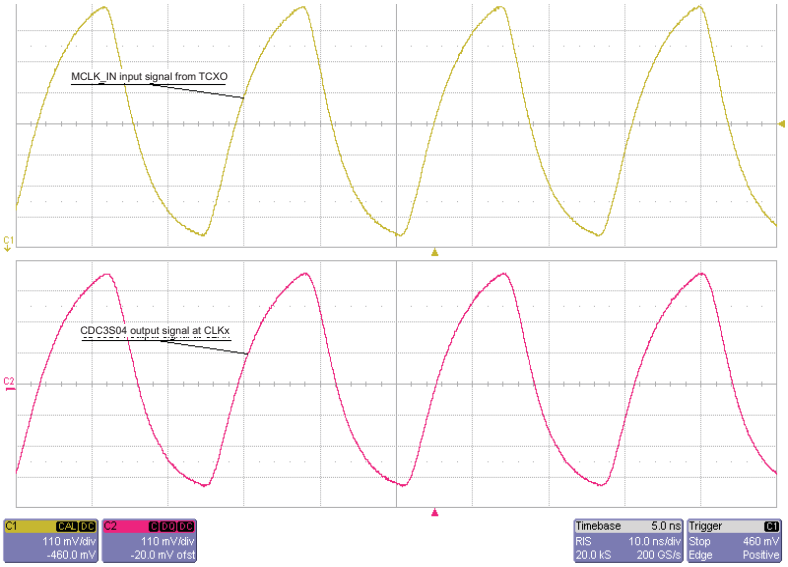

Figure 13.

TYPICAL CHARACTERISTICS (continued)

TCXO INPUT CLOCK
vs
OUTPUT CLOCK AT 26 MHz

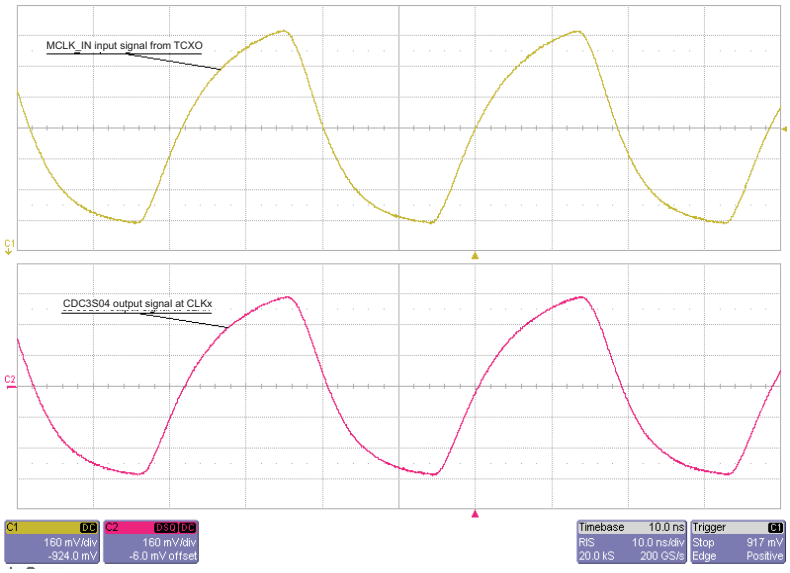

Figure 14.

SINE WAVE INPUT CLOCK
vs
OUTPUT CLOCK AT 38.4 MHz

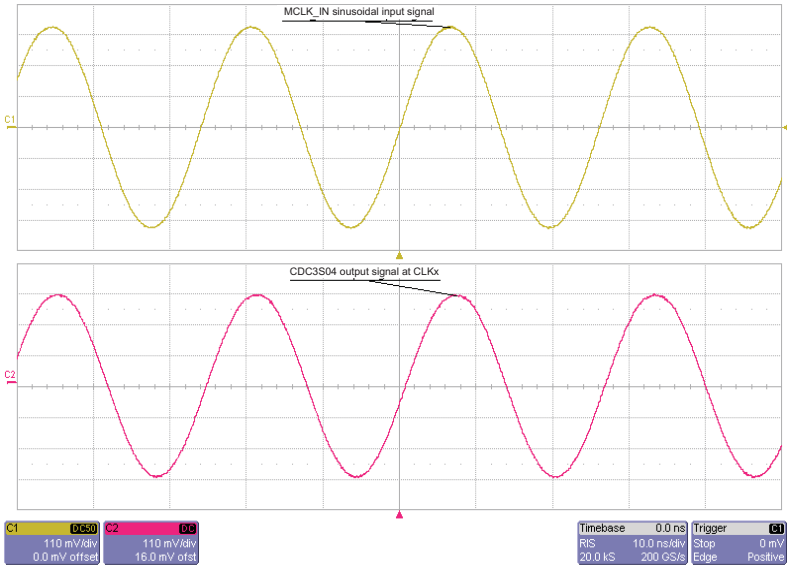

Figure 15.

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TYPICAL CHARACTERISTICS (continued)

SINE WAVE INPUT CLOCK
vs
OUTPUT CLOCK AT 26 MHz

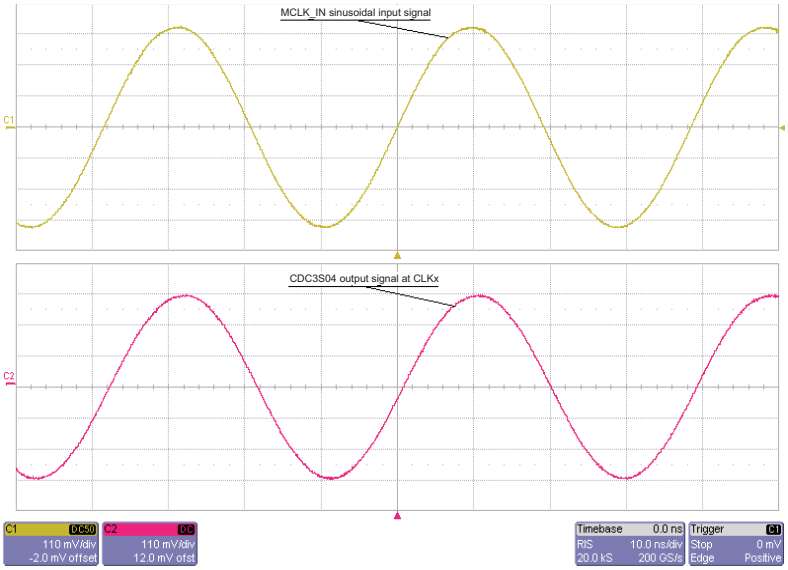

Figure 16.

OUTPUT GAIN
vs
INPUT FREQUENCY (MCLK_IN)

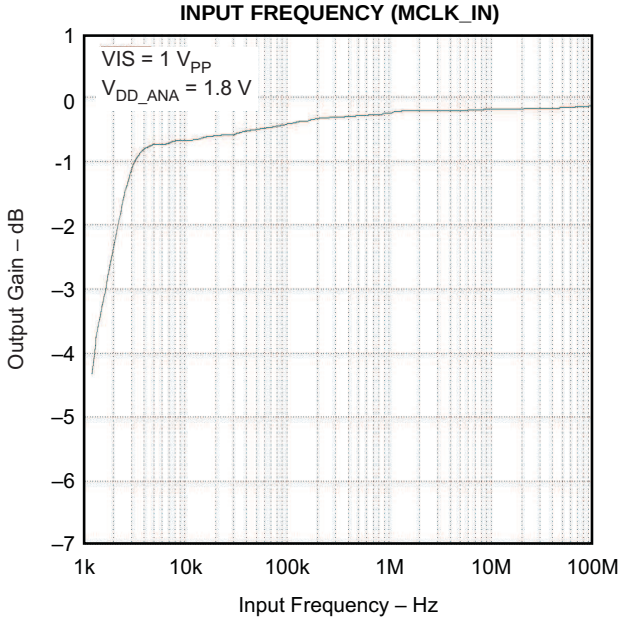

Figure 17.

TYPICAL CHARACTERISTICS (continued)

INPUT
vs
OUTPUT PHASE-NOISE PERFORMANCE WITH 38.4-MHz TCXO

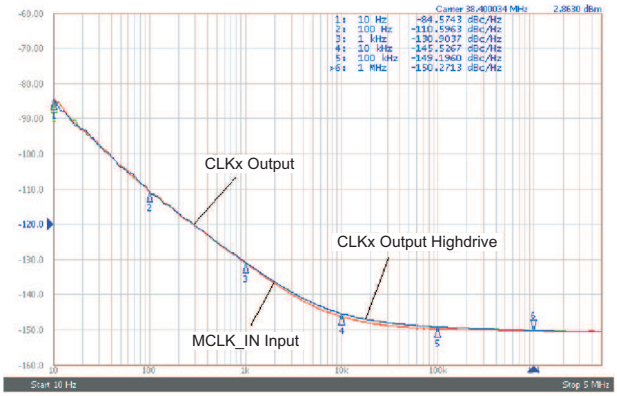

Figure 18.

INPUT
vs
OUTPUT PHASE-NOISE PERFORMANCE WITH 26-MHz TCXO

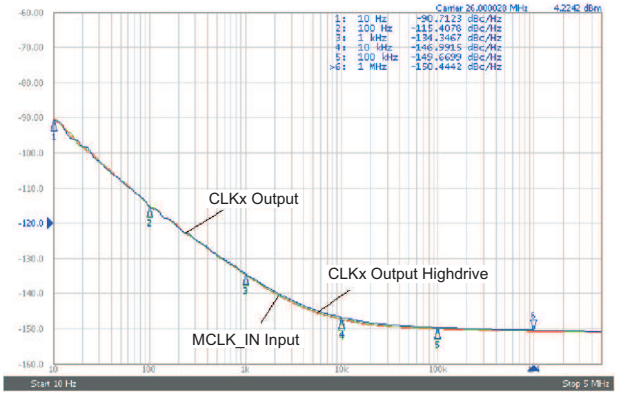

Figure 19.

LDO POWER SUPPLY REJECTION
vs
FREQUENCY (PSRR)

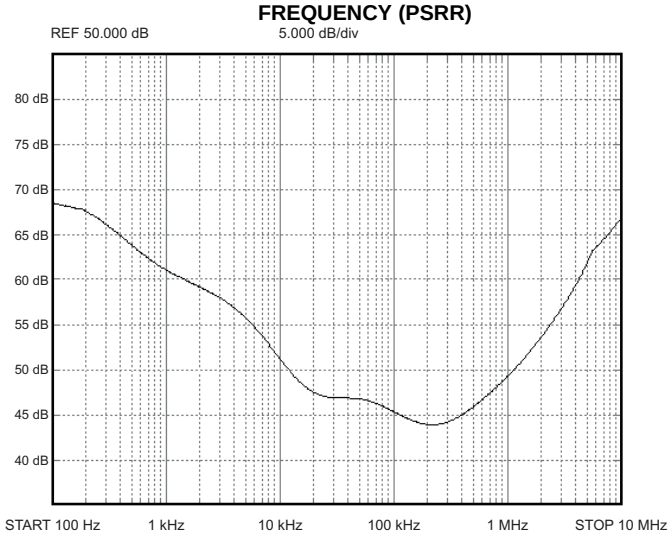

Figure 20.

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TYPICAL CHARACTERISTICS (continued)

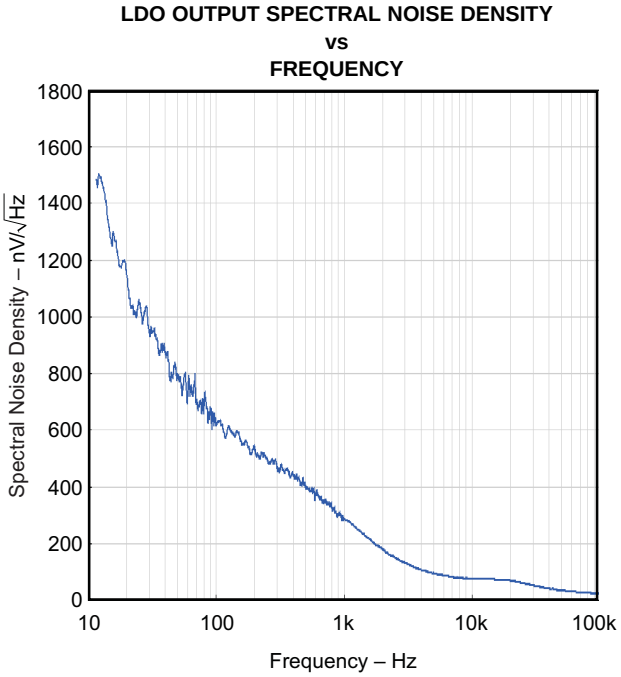

Figure 21.

DETAILED DESCRIPTION

SDAH/SCLH SERIAL INTERFACE (Hs-Mode)

This section describes the SDAH/SCLH interface of the CDC3S04 device. The CDC3S04 operates as a slave device of the two-wire serial SDAH/SCLH bus, compatible with the popular I^2C specification (UM10204-I^2C-bus specification and user manual Rev. 03–19 June 2007). It operates in the high-speed mode (up to 3.4 Mbit/s) and supports 7-bit addressing. The CDC3S04 is fully downward compatible with fast- and standard-mode (F/S) devices for bidirectional communication in a mixed-speed bus system.

Data Protocol

The device supports byte-write and byte-read operations only. There is no block-write or block-read operation supported; therefore, no command code byte is needed.

When a byte has been sent, it is written into the internal register and is immediately effective.

Slave Receiver Address (7 bits)

Device	A6	A5	A4	A3	A2	A1	A0(1)	R/$\overline{W}$
CDC3S04	1	1	0	1	1	0	0	1/0

(1) Address bit A0 is selectable by the ADR_A0 input (pin D1). This allows addressing of two devices connected to the same I^2C bus. The default value is 0, set by an internal pulldown resistor.

Byte-Write Programming Sequence

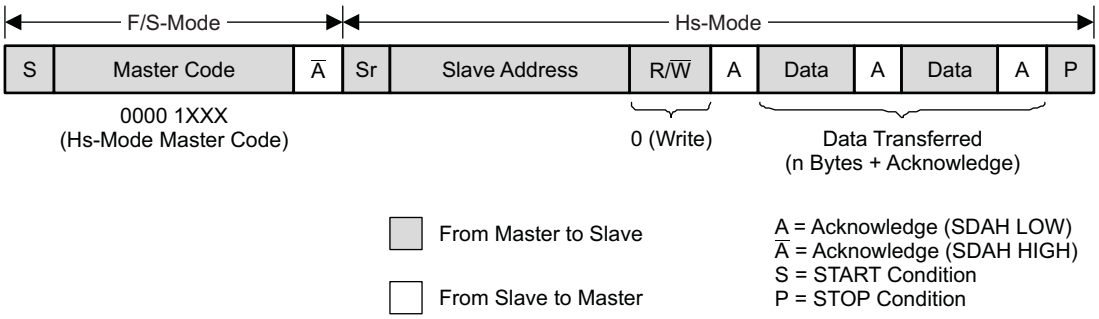

Figure 22. Byte-Write Protocol

Byte-Read Programming Sequence

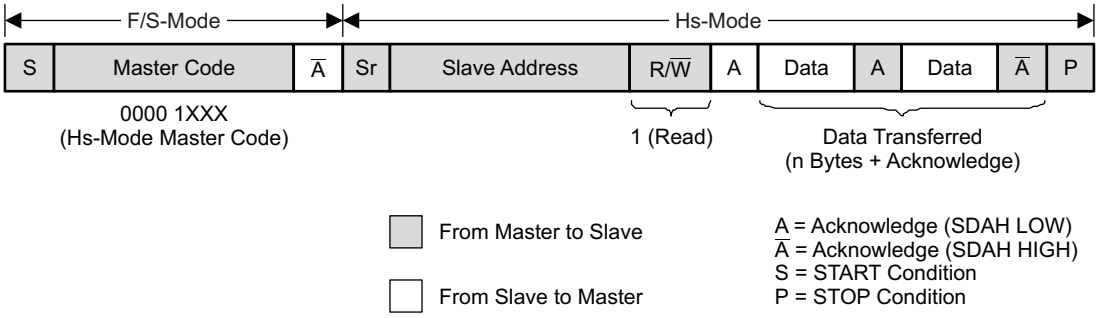

Figure 23. Byte-Read Protocol

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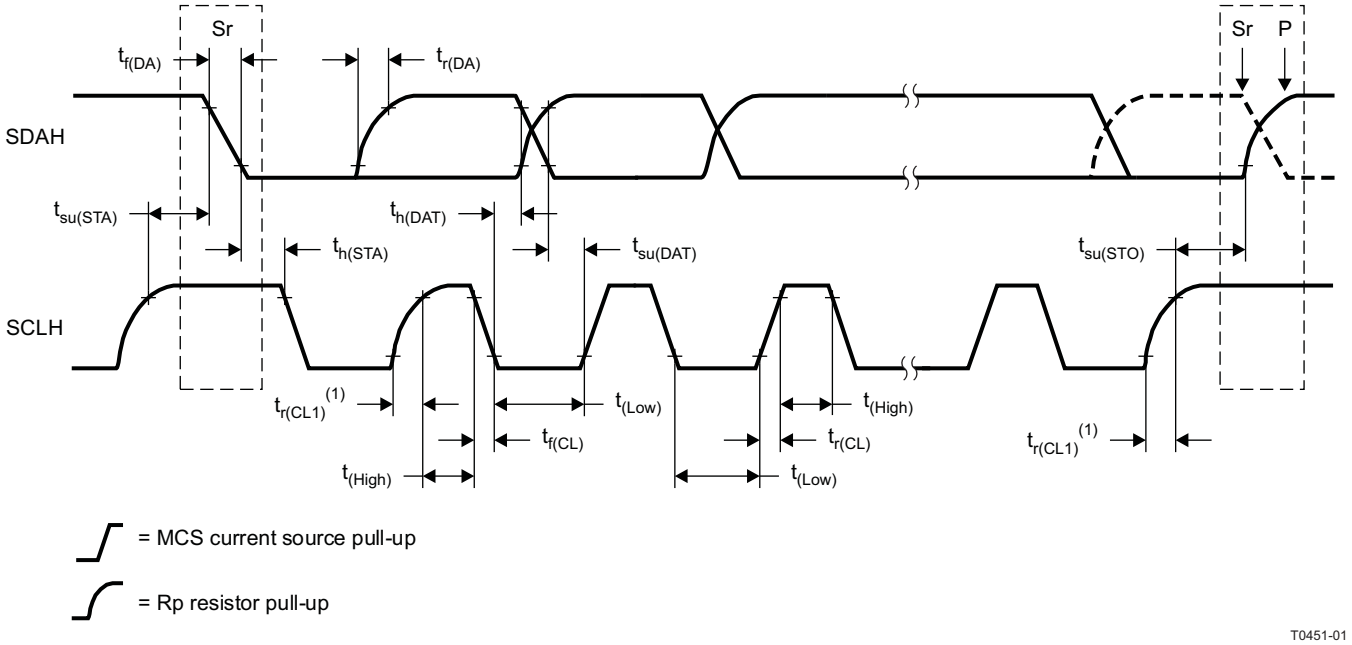

(1) First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 24. Definition of Timing for a Complete Hs-Mode Transfer

The following diagram shows how the CDC3S04 clock buffer is connected to the SDAH/SCLH serial interface bus. Multiple devices can be connected to the bus, but the speed may need to be reduced (3.4 MHz is the maximum) if many devices are connected.

Note that the pullup resistors (R_P) depend on the supply voltage, bus capacitance, and number of connected devices. For more details, see the I^2C bus specification.

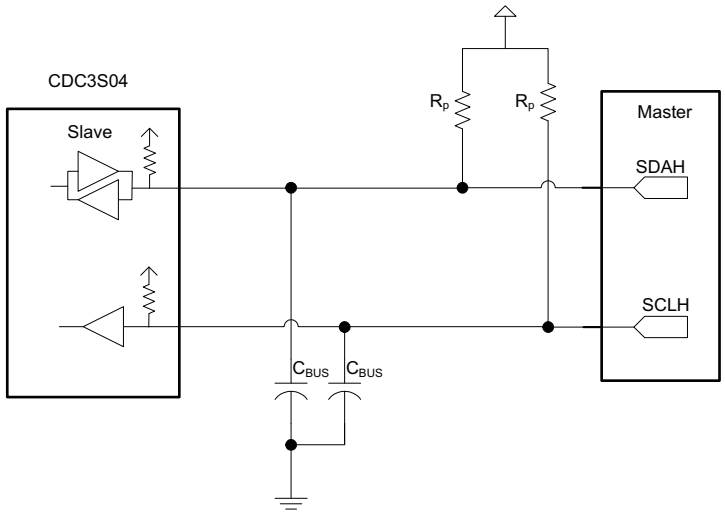

Figure 25. SDAH/SCLH Hardware Interface

SDAH/SCLH Configuration Registers

The output stages are user configurable. Table 3 explains the programmable functions of the CDC3S04.

Table 3. Configuration Register (Shaded Cells Marks Power-Up/Default Setting)

Offset	BIT[1]	Acronym	Default[2]	$\overline{\text{RESET}}$ [3]	Description	0	1	Type
00h	7	REQ4INT	1b	1b	CLK4 off/on[4]	Off	On	R/W
	6	REQ3INT	0b	–	CLK3 off/on[4]	Off	On	
	5	REQ2INT	0b	–	CLK2 off/on[4]	Off	On	
	4	REQ1INT	1b	1b	CLK1 off/on[4]	Off	On	
	3	REQ4POL	1b	–	Selects polarity of REQ4	Active-low	Active-high	
	2	REQ3POL	1b	–	Selects polarity of REQ3	Active-low	Active-high	
	1	REQ2POL	1b	–	Selects polarity of REQ2	Active-low	Active-high	
	0	REQ1POL	1b	–	Selects polarity of REQ1	Active-low	Active-high	
01h	7	MREQ4	1b	–	Defines if REQ4 is used to decode MCLK_REQ	Not used for decoding	Used for decoding	R/W
	6	MREQ3	1b	–	Defines if REQ3 is used to decode MCLK_REQ			
	5	MREQ2	1b	–	Defines if REQ2 is used to decode MCLK_REQ			
	4	MREQ1	1b	–	Defines if REQ1 is used to decode MCLK_REQ			
	3	MCLKOUT1	00b	–	Selects MCLK_REQ output type 00 = wired-OR (default setting) 01 = wired-AND 1x = push-pull			
	2	MCLKOUT0						
	0–1	–	00b	–	Reserved			
02h	7	MREQCTRL1	00b	–	MCLK_REQ generation (see Figure 27) 0x = decoder controlled (default setting) 10 = low 11 = high			R/W
	6	MREQCTRL0						
	5	LDOEN1	00b	–	Switches LDO on or off: 00 = LDO is on (default setting) 01 = LDO is off 1x = decoder controlled (see Figure 27)			
	4	LDOEN0						
	3	REQ4PRIO	1b	1b	Defines external vs internal REQ4 priority	REQ4	REQ4INT	
	2	REQ3PRIO	0b	–	Defines external vs internal REQ3 priority	REQ3	REQ3INT	
	1	REQ2PRIO	0b	–	Defines external vs internal REQ2 priority	REQ2	REQ2INT	
	0	REQ1PRIO	1b	1b	Defines external vs internal REQ1 priority	REQ1	REQ1INT	
03h	7	HIGHDRIVE4	0b	–	Enables high-drive capability CLK4	Typical	High	R/W
	6	HIGHDRIVE3	0b	–	Enables high-drive capability CLK3	Typical	High	
	5	HIGHDRIVE2	0b	–	Enables high-drive capability CLK2	Typical	High	
	4	HIGHDRIVE1	0b	–	Enables high-drive capability CLK1	Typical	High	
	0–3	–	0b	–	Reserved			
04h–Bh[5]		–		–	Reserved			R/W

(1) All data is transferred with the MSB first.
(2) A device reset to default condition is initiated by a V_{DD_DIG} power-up sequence.
(3) "–" means that dedicated bits do not change at $\overline{\text{RESET}}$.
(4) Inactive as long as the REQxPRIO bit is low, external REQx pins are valid (see Figure 26)
(5) Writing data beyond 03h may affect device function.

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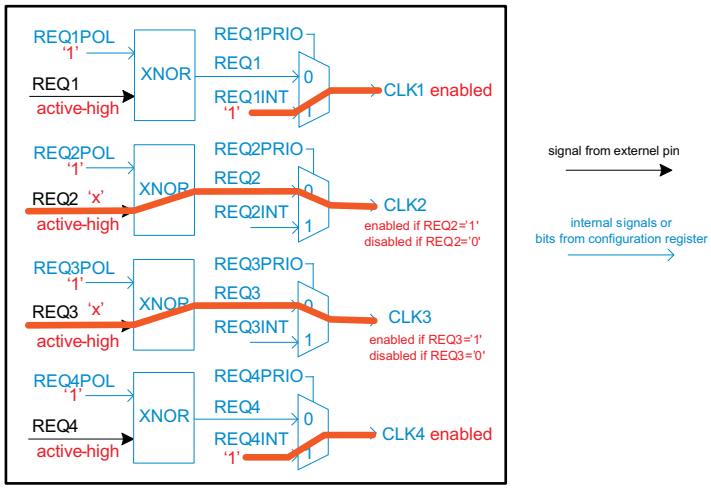

Figure 26. Clock Output Enable Signal
(Shaded Line Marks Power-Up/Default Setting)

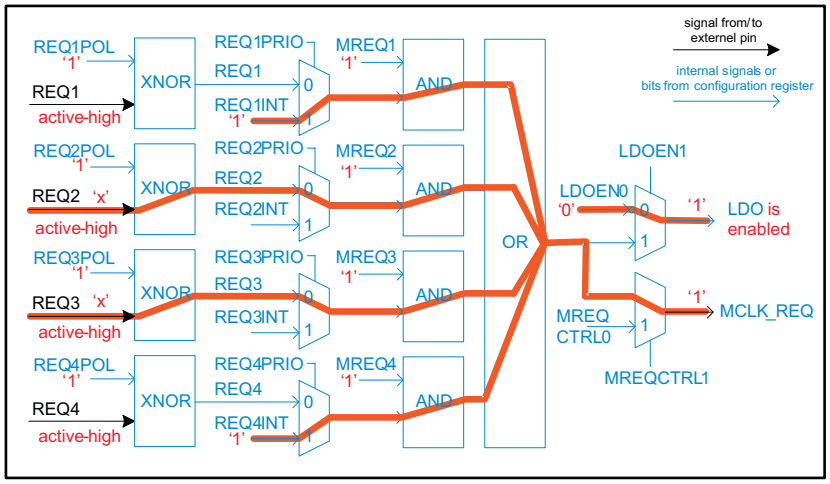

Figure 27. Decoding Scheme for MCLK_REQ and LDOEN
(Shaded Line Marks Power-Up/Default Setting)

APPLICATION INFORMATION

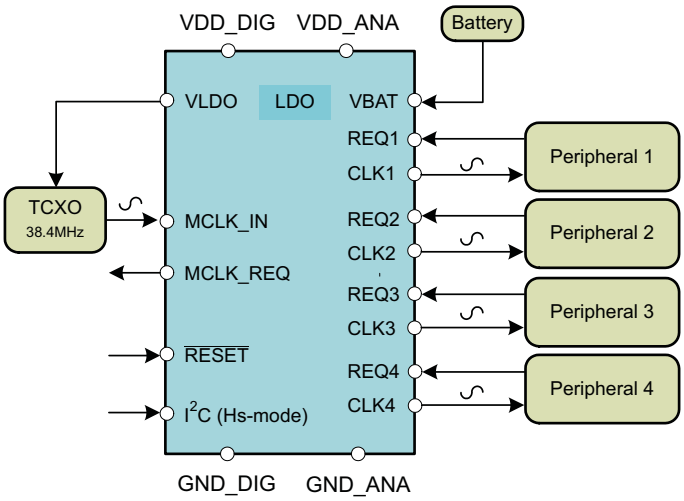

Figure 28. Clock Distribution Scheme

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REVISION HISTORY

Changes from Original (October 2009) to Revision A **Page**

- Changed the format on page 1 (moved 2 paragraphs from page 2 to page 1) 1
- Changed the X axis from 0.1us to 100us....900us 9
- Changed Offset 00h Bit 4 Default value from 0h to 1b 18

Changes from Revision A (July 2010) to Revision B **Page**

- Changed Table 3 "Offset" values listed in "Default" and "$\overline{\text{RESET}}$" columns from "h" to "b". 18

Changes from Revision B (May 2011) to Revision C **Page**

- Changed from Rev B, 2011 to Rev C, 2012 1
- Changed the 8th Feature item from –30°C to –40°C 1
- Changed in the last paragraph of description from –30°C to –40°C 2
- Changed in the ROC table last row, from –30°C to –40°C 4

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC3S04YFFR	Active	Production	DSBGA (YFF) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CDC3S04
CDC3S04YFFR.B	Active	Production	DSBGA (YFF) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CDC3S04

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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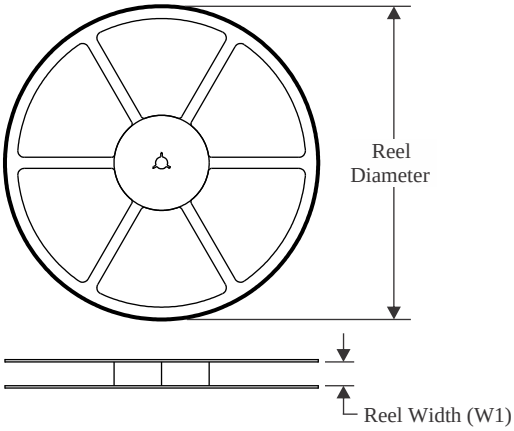
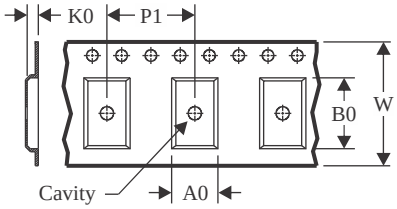
TAPE AND REEL INFORMATION

REEL DIMENSIONS

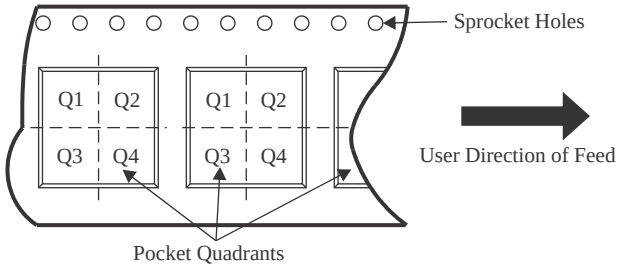


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

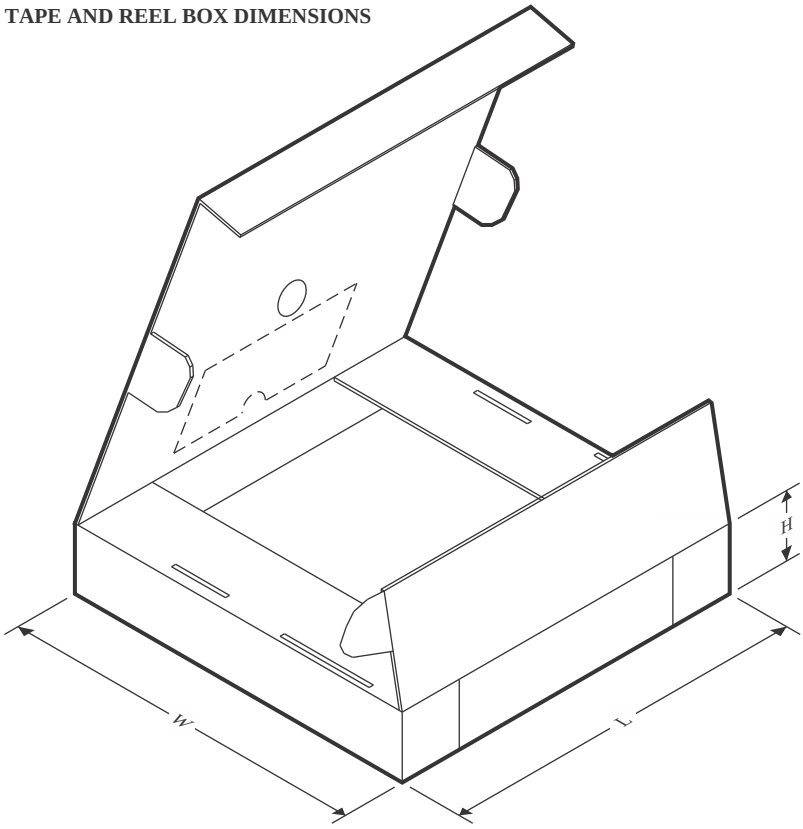
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC3S04YFFR	DSBGA	YFF	20	3000	180.0	8.4	1.63	2.08	0.69	4.0	8.0	Q1

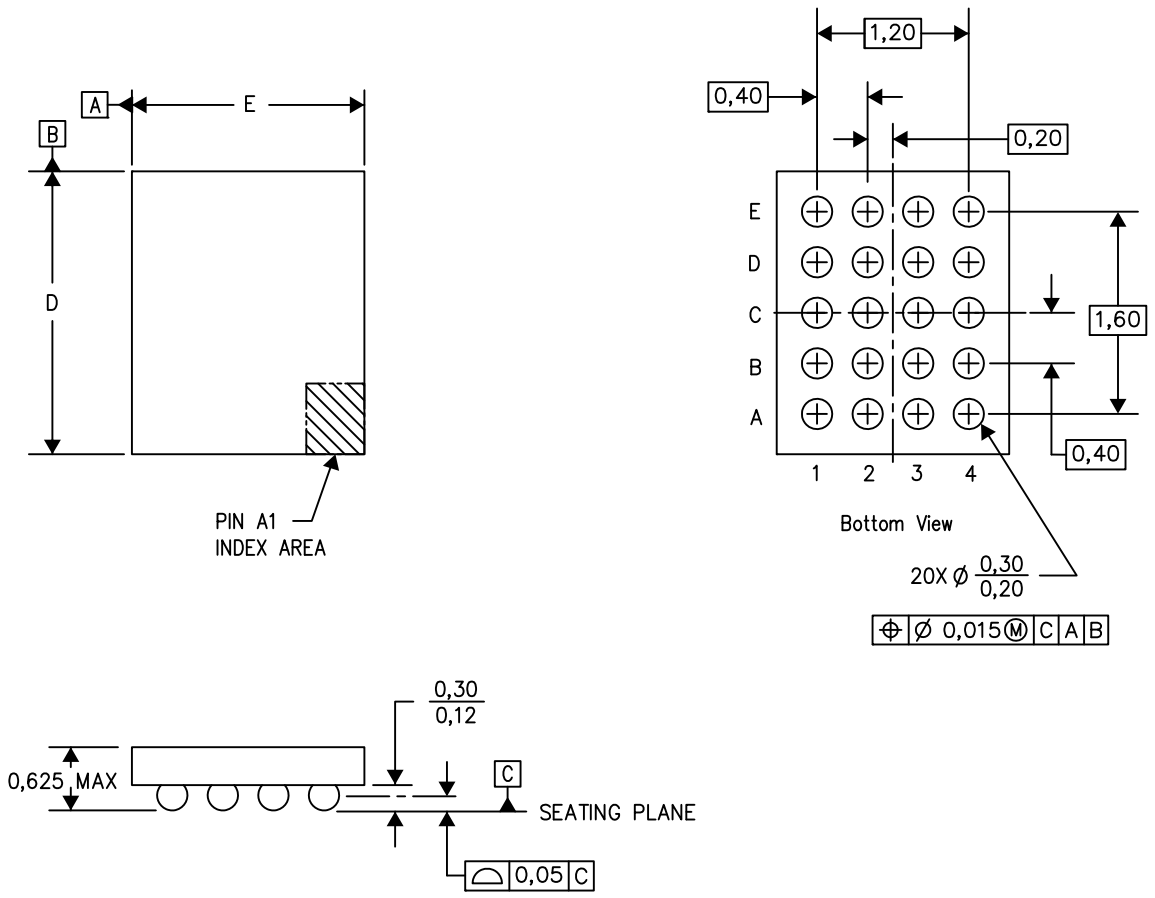
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC3S04YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0

YFF (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.59 mm, Min = 1.53 mm

4207625–9/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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