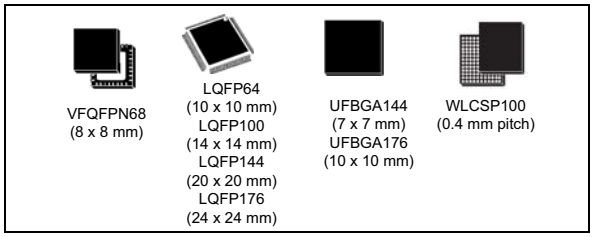
STM32F722xx
STM32F723xx

Arm® Cortex®-M7 32b MCU+FPU, 462DMIPS, up to 512KB flash 256+16+4KB RAM, USB OTG HS/FS, 18 TIMs, 3 ADCs, 21 com IF

Datasheet - production data

Features

- Includes ST state-of-the-art patented technology
- Core: Arm® 32-bit Cortex®-M7 CPU with FPU, adaptive real-time accelerator (ART Accelerator) and L1-cache: 8 Kbytes of data cache and 8 Kbytes of instruction cache, allowing 0-wait state execution from embedded flash memory and external memories, frequency up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1) and DSP instructions.
- Memories
  - Up to 512 Kbytes of flash memory with protection mechanisms (read and write protections, proprietary code readout protection (PCROP))
  - 528 bytes of OTP memory
  - SRAM: 256 Kbytes (including 64 Kbytes of data TCM RAM for critical real-time data) + 16 Kbytes of instruction TCM RAM (for critical real-time routines) + 4 Kbytes of backup SRAM (available in the lowest power modes)
  - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- Dual mode Quad-SPI
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - Dedicated USB power
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low-power



  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 32×32 bit backup registers + 4 Kbytes of backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- Up to 18 timers: up to thirteen 16-bit (1x low-power 16-bit timer available in Stop mode) and two 32-bit timers, each with up to 4 IC/OC/PWMs or pulse counter and quadrature (incremental) encoder inputs. All 15 timers running up to 216 MHz. 2x watchdogs, SysTick timer
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Debug mode
  - SWD and JTAG interfaces
  - Cortex®-M7 Trace Macrocell™
- Up to 140 I/O ports with interrupt capability
  - Up to 136 fast I/Os up to 108 MHz
  - Up to 138 5 V-tolerant I/Os
- Up to 21 communication interfaces
  - Up to 3× I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/4 UARTs (27 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to 5 SPIs (up to 54 Mbit/s), 3 with muxed simplex I2Ss for audio class accuracy via internal audio PLL or external clock
  - 2 x SAIs (serial audio interface)
  - 1 x CAN (2.0B active)

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  - 2 x SDMMCs
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and on-chip Hi-speed PHY or ULPI depending on the part number
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F722xx	STM32F722IC, STM32F722IE, STM32F722RC, STM32F722RE, STM32F722VC, STM32F722VE, STM32F722ZC, STM32F722ZE
STM32F723xx	STM32F723IC, STM32F723IE, STM32F723RC, STM32F723RE,STM32F723VC, STM32F723VE, STM32F723ZC, STM32F723ZE

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F722xx and STM32F723xx microcontrollers.

This document should be ready in conjunction with the *STM32F72xxx and STM32F73xxx advanced Arm®-based 32-bit MCUs* reference manual (RM0431). The reference manual is available from the STMicroelectronics website *www.st.com.*

For information on the Arm® Cortex®-M7 core, refer to the Cortex®-M7 technical reference manual available from the http://www.arm.com website.





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For information on the device errata with respect to the datasheet and reference manual, refer to the STM32F72xxx and STM32F73xxx errata sheet (ES0360), available on the STMicroelectronics website www.st.com.

2 Description

The STM32F722xx and STM32F723xx devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a single floating point unit (SFPU) precision which supports Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F722xx and STM32F723xx devices incorporate high-speed embedded memories with a flash memory up to 512 Kbytes, 256 Kbytes of SRAM (including 64 Kbytes of data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, thirteen general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to three I^2Cs
- Five SPIs, three I^2Ss in half duplex mode. To achieve the audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI or with the integrated HS PHY depending on the part number)
- One CAN
- Two SAI serial audio interfaces
- Two SDMMC host interfaces

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI flash memory interface.

The STM32F722xx and STM32F723xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for the USB (OTG_FS and OTG_HS) and the SDMMC2 (clock, command and 4-bit data) are available on all the packages except LQFP100 and LQFP64 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F722xx and STM32F723xx devices offer devices in 7 packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F722xx and STM32F723xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control,
- Medical equipment,
- Industrial applications: PLC, inverters, circuit breakers,
- Printers, and scanners,
- Alarm systems, video intercom, and HVAC,
- Home audio appliances,
- Mobile applications, Internet of Things,
- Wearable devices: smart watches.

The following table lists the peripherals available on each part number.

Table 2. STM32F722xx and STM32F723xx **features and peripheral counts**

Peripherals		STM32F72xRx		STM32F72xVx		STM32F72xZx		STM32F72xIx	
Flash memory in Kbytes		256	512	256	512	256	512	256	512
SRAM in Kbytes	System	256(176+16+64)							
	Instruction	16							
	Backup	4							
FMC memory controller		No		Yes[1]					
QUADSPI		Yes							
Timers	General-purpose	10[2]							
	Advanced-control	2							
	Basic	2							
	Low-power	No		1					
Random number generator		Yes							
Communication interfaces	SPI/I2S	3/3 (simplex)[3]		4/3 (simplex)[3]		5/3 (simplex)[3]			
	I2C	3							
	USART/UART	4/2		4/4					
	USB OTG FS	Yes							
	USB OTG HS[4]	Yes							
	USB OTG PHY HS controller (USBPHYC)	Yes	No	Yes[11]					
	CAN	1							
	SAI	2							
	SDMMC1	Yes							
	SDMMC2	No		Yes[5][6]					

Table 2. STM32F722xx and STM32F723xx **features and peripheral counts (continued)**

Peripherals	STM32F72xRx		STM32F72xVx	STM32F72xZx	STM32F72xIx
GPIOs	51	50	82 in STM32F722xx 79 in STM32F723xx	114 in STM32F722xx 112 in STM32F723xx	140 in STM32F722xx 138 in STM32F723xx
12-bit ADC Number of channels	3				
	16			24	
12-bit DAC Number of channels	Yes 2				
Maximum CPU frequency	216 MHz(7)				
Operating voltage	1.7 to 3.6 V(8)				
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C(9)				
	Junction temperature: –40 to + 125 °C				
Package	VFQFPN68 (11)	LQFP64 (10)	LQFP100 WLCSP100(11)	LQFP144 UFBGA144(11)	UFBGA176 LQFP176

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. On the STM32F723xx device packages, except the 176-pin ones, the TIM12 is not available, so there are 9 general-purpose timers.
3. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I^2S audio mode.
4. USB OTG HS with the ULPI on the STM32F722xx devices and with integrated HS PHY on the STM32F723xx devices.
5. The SDMMC2 supports a dedicated power rail for clock, command and data 0..4 lines, feature available starting from 144 pin package.
6. The SDMMC2 is not available on the STM32F723Vx devices.
7. 216 MHz maximum frequency for - 40°C to + 85°C ambient temperature range (200 MHz maximum frequency for - 40°C to + 105°C ambient temperature range).
8. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 3.15.2: Internal reset OFF*).
9. Range -40° to +105°C is not available for WLCSP packages.
10. Available only on the STM32F722xx devices.
11. Available only on the STM32F723xx devices.

2.1 Full compatibility throughout the family

The STM32F722xx devices are fully pin-to-pin, compatible with the STM32F7x5xx, STM32F7x6xx, STM32F7x7xx devices.

The STM32F722xx devices are partially pin-to-pin, compatible with the STM32F4xxxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

Figure 1 and *Figure 2* give compatible board designs between the STM32F722xx, with LQFP64 and LQFP100 packages, and STM32F4xx families.

Figure 1. Compatible board design for LQFP100 package

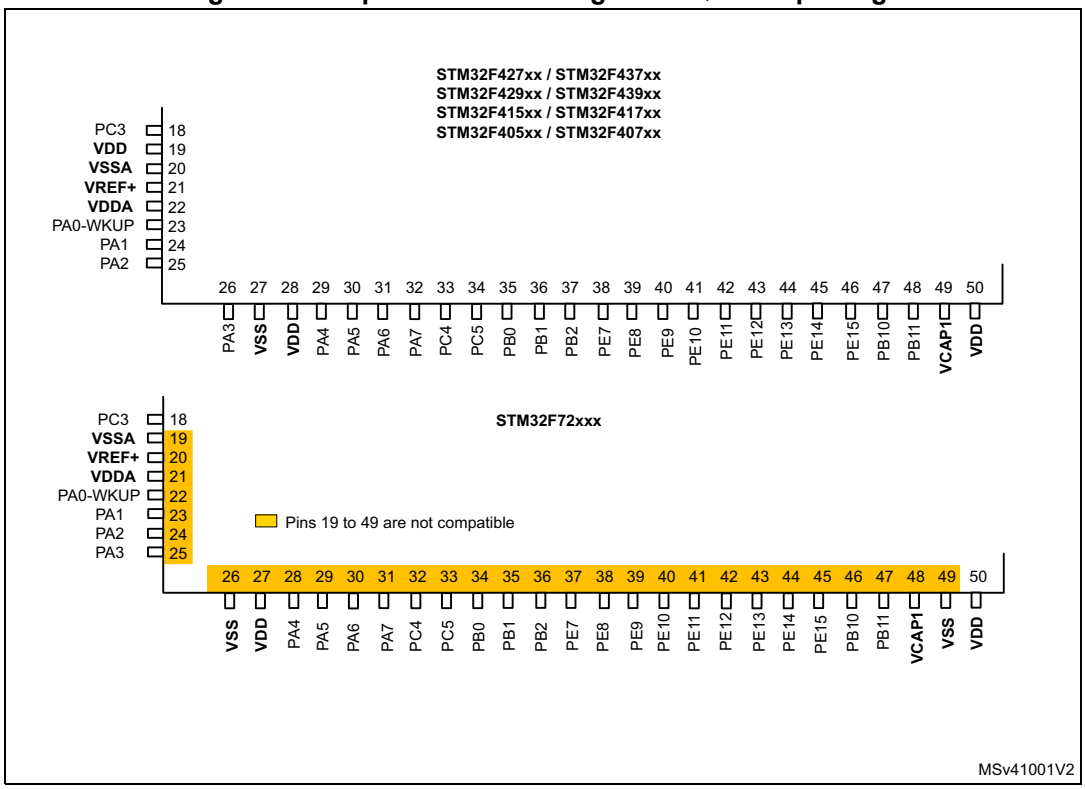
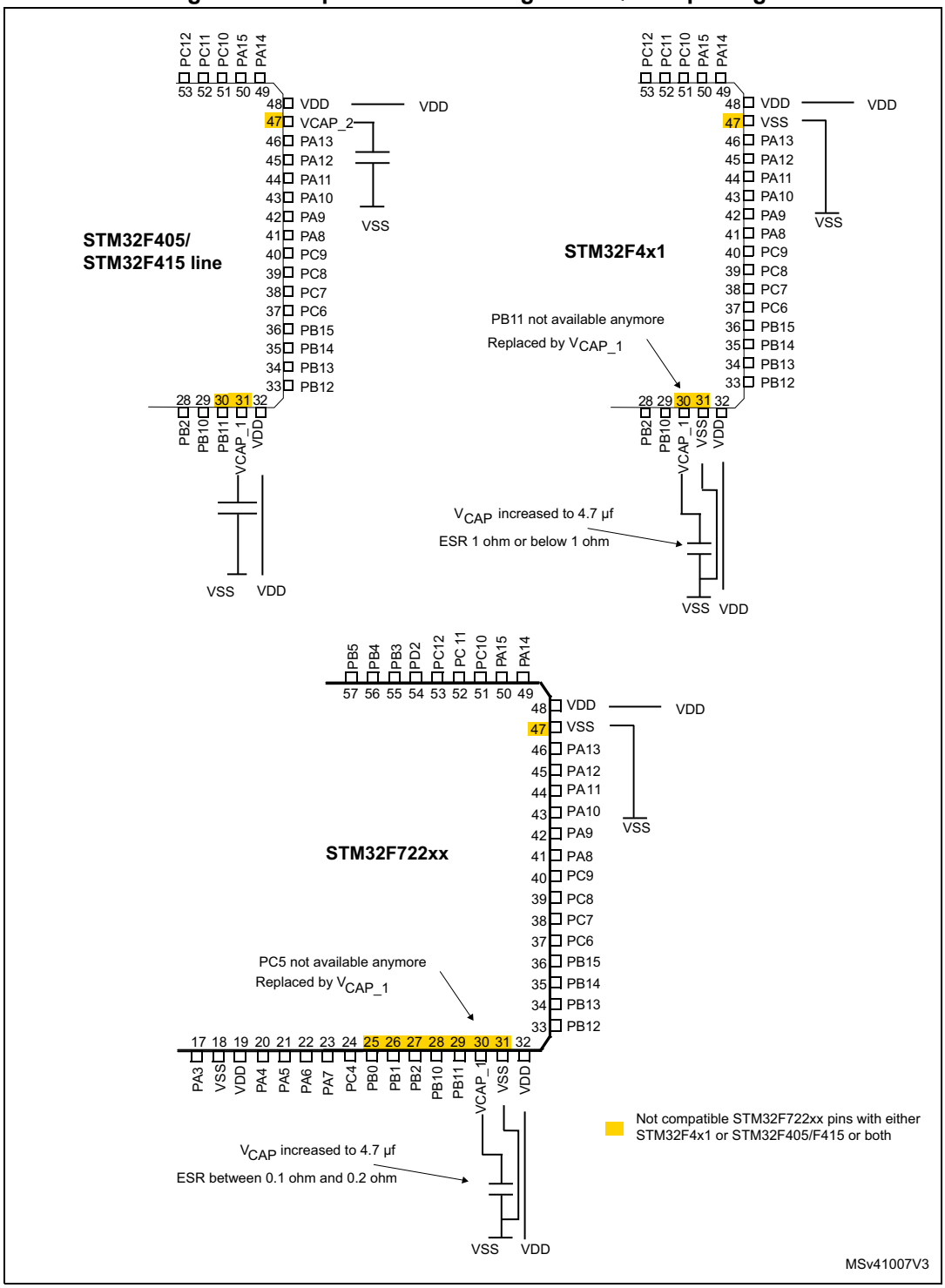


Figure 2. Compatible board design for LQFP64 package



The STM32F722xx LQFP144, UFBGA176 and LQFP176 packages are fully pin to pin compatible with the STM32F4xx devices.

2.2 STM32F723xx versus STM32F722xx LQFP100/ LQFP144/ LQFP176 packages

Figure 3. Compatible board design for LQFP100 package

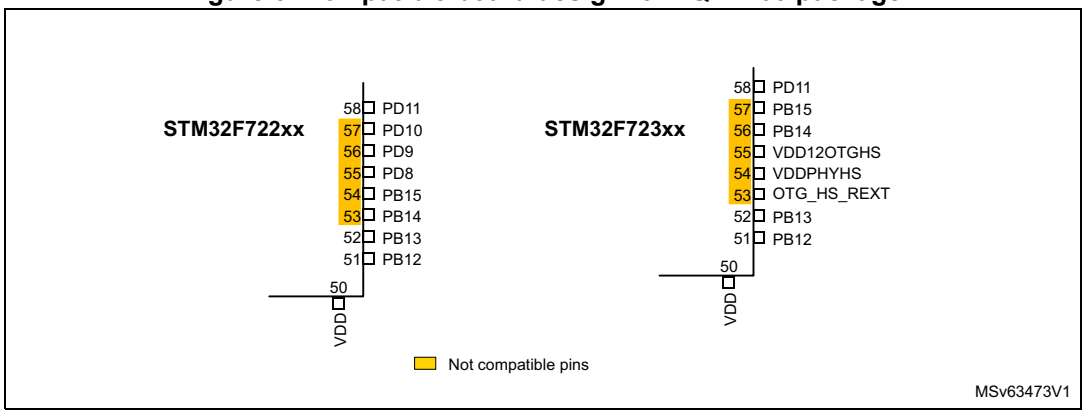


Figure 4. Compatible board design for LQFP144 package

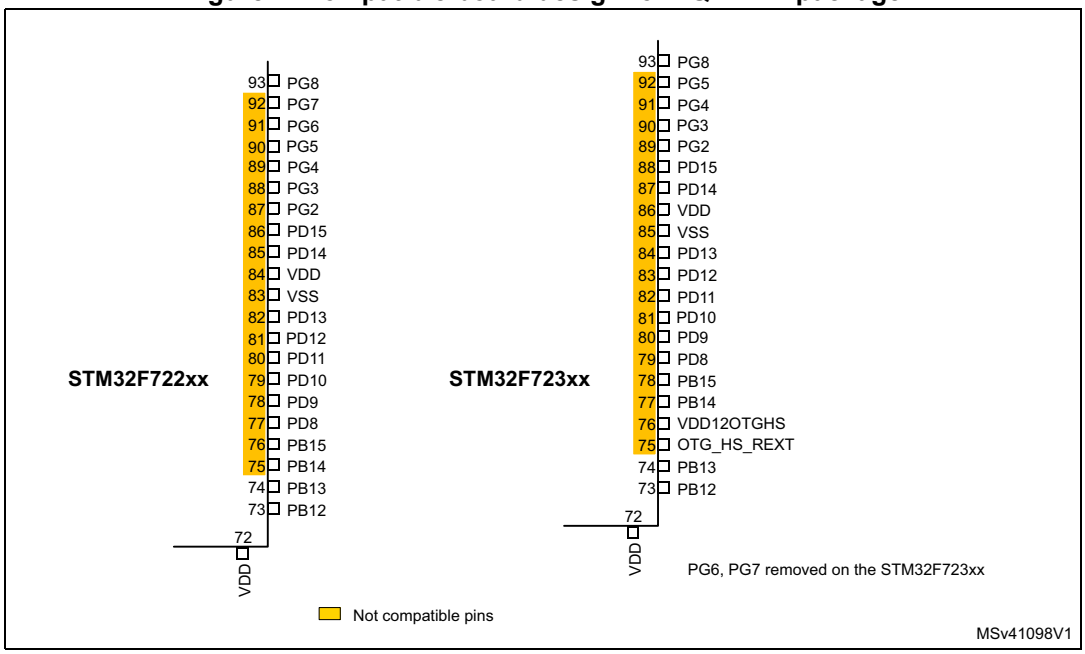


Figure 5. Compatible board design for LQFP176 package

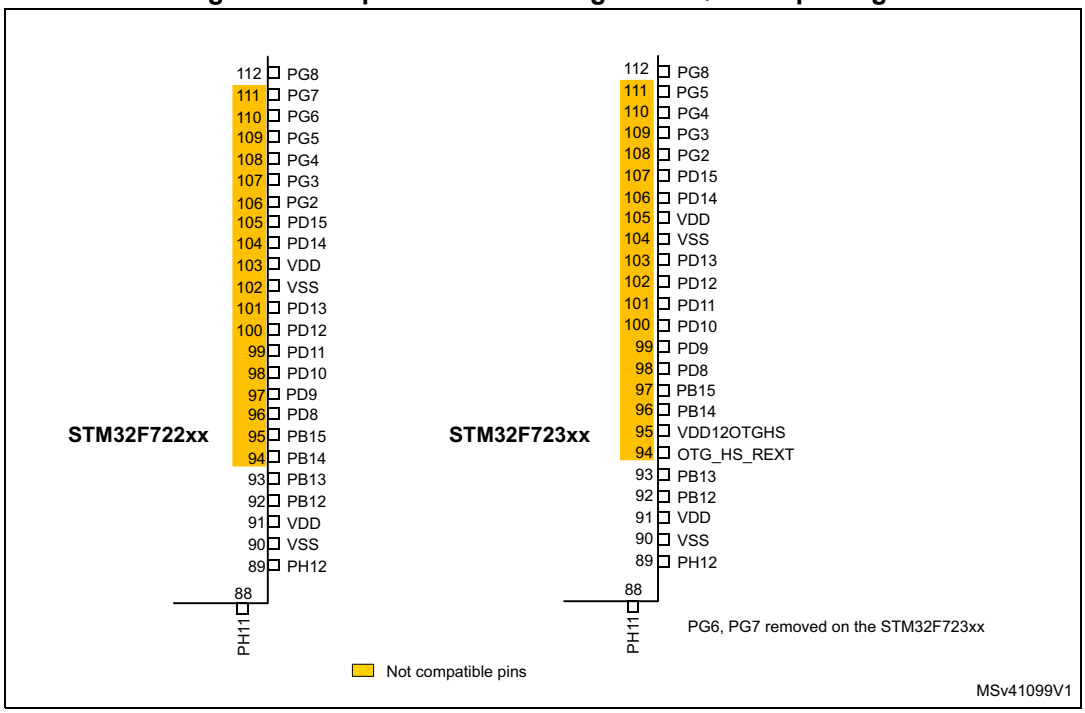
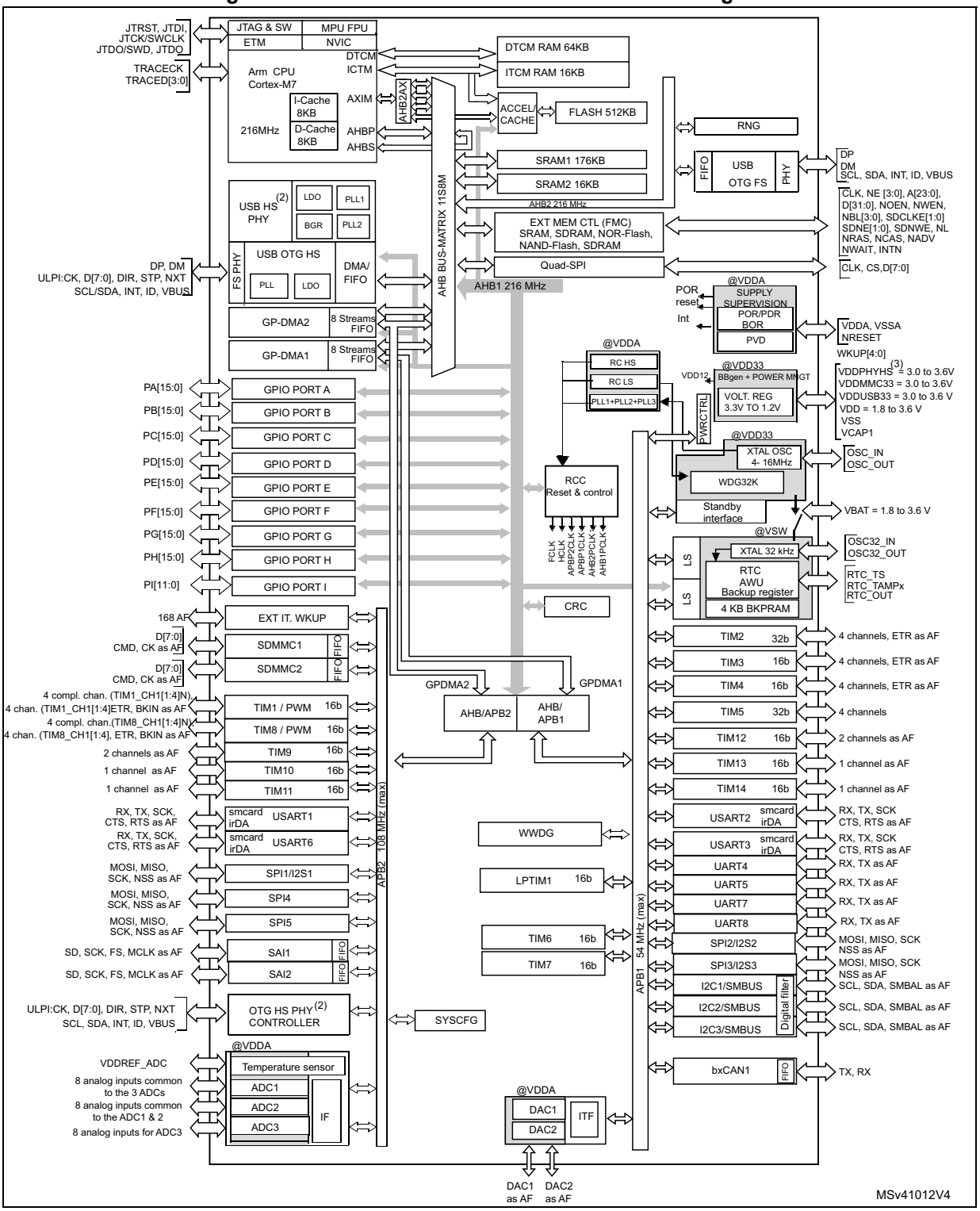


Figure 6 shows the general block diagram of the device family.

Figure 6. STM32F722xx and STM32F723xx **block diagram**



1. The timers connected to APB2 are clocked from TIMxCLK up to 216 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 108 MHz or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.
2. Available only on the STM32F723xx devices.
3. Available only on the STM32F723xx LQFP100 package.

3 Functional overview

3.1 Arm Cortex-M7 with FPU

The Arm Cortex-M7 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (8 Kbytes of I-cache and 8 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- tightly-coupled memory (TCM) interface
- Harvard instruction and data caches and AXI master (AXIM) interface
- dedicated low-latency AHB-Lite peripheral (AHBP) interface

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It supports single precision FPU (floating point unit), speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 6 shows the general block diagram of the STM32F722xx and STM32F723xx family.

Note: Cortex-M7 with FPU core is binary compatible with the Cortex-M4 core.

3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to eight protected areas that can in turn be divided up into eight subareas. The protection area sizes are between 32 bytes and the whole 4 Gbytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded flash memory

The STM32F722xx and STM32F723xx devices embed a flash memory of up to 512 Kbytes available for storing programs and data.

The flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: no access (read, erase, program) to the flash memory or backup SRAM can be performed while the debug feature is connected or while booting from RAM or system memory bootloader.
  - Level 2: debug/chip read protection disabled
- Write protection (WRP): the protected area is protected against erasing and programming.
- Proprietary code readout protection (PCROP): flash memory user sectors (0 to 7) can be protected against D-bus read accesses by using the proprietary readout protection (PCROP). The protected area is execute-only.

3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Embedded SRAM

All the devices feature:

- System SRAM up to 256 Kbytes:
  - SRAM1 on AHB bus Matrix: 176 Kbytes
  - SRAM2 on AHB bus Matrix: 16 Kbytes
  - DTCM-RAM on TCM interface: 64 Kbytes for critical real-time data
- Instruction RAM (ITCM-RAM) 16 Kbytes:
  - It is mapped on TCM interface and reserved only for CPU execution/instruction useful for critical real-time routines.

The data TCM RAM is accessible by the GP-DMAs and peripheral DMAs through the specific AHB slave of the CPU.The instruction TCM RAM is reserved only for CPU. It is accessed at CPU clock speed with 0 wait states.

- 4 Kbytes of backup SRAM

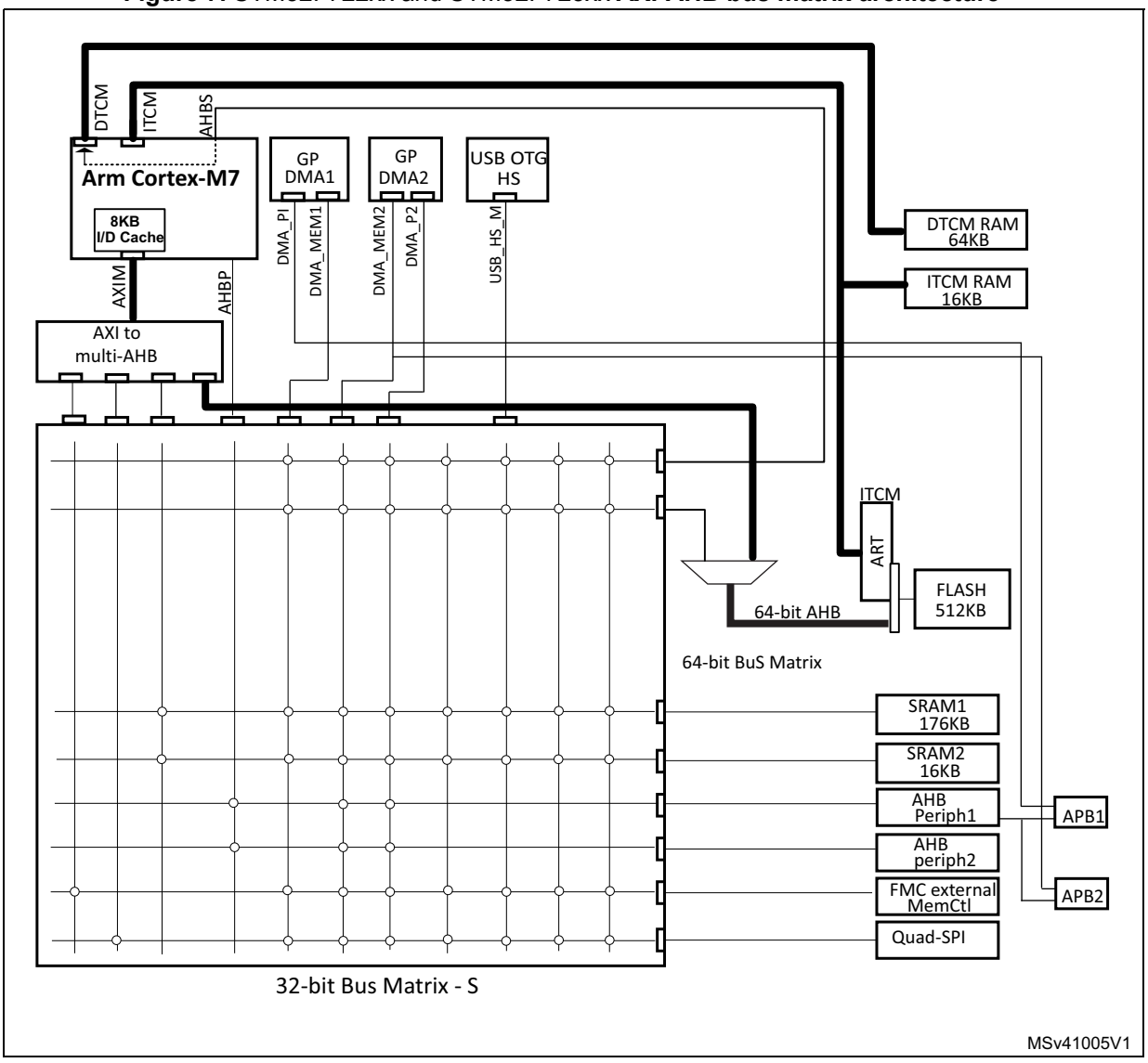
  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.6 AXI-AHB bus matrix

The STM32F722xx and STM32F723xx system architecture is based on two subsystems:

- an AXI-to-multi-AHB bridge converting AXI4 protocol to AHB-Lite protocol:
  - 3x AXI-to-32-bit-AHB bridges connected to AHB bus matrix
  - 1x AXI-to-64-bit-AHB bridge connected to the embedded flash memory
- a multi-AHB bus matrix
  - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, USB HS) and the slaves (flash memory, RAM, FMC, QUADSPI, AHB and APB peripherals), and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 7. STM32F722xx and STM32F723xx **AXI-AHB bus matrix architecture**(1)



1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

3.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with eight streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support a circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. The configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I2S
- I2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- ADC
- SAI
- QUADSPI

3.8 Flexible memory controller (FMC)

The flexible memory controller (FMC) includes three memory controllers:

- NOR/PSRAM memory controller
- NAND/memory controller
- synchronous DRAM (SDRAM/mobile LPSDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/oneNAND flash memory
  - PSRAM (four memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-, 16-, 32-bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller

- HCLK/2 maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports Intel® 8080 and Motorola® 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules, with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.9 Quad-SPI memory interface (QUADSPI)

All the devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting single, dual or quad-SPI flash memories. It can work in:

- Direct mode through registers
- External flash status register polling mode
- Memory-mapped mode

Up to 256 Mbytes of external flash are memory mapped, supporting 8-, 16-, and 32-bit access. The code execution is supported.

The opcode and the frame format are fully programmable. The communication can be either in single-data rate or dual-data rate.

3.10 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 110 maskable interrupt channels, plus the 16 interrupt lines of the Cortex-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with a minimum interrupt latency.

3.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs in the STM32F722xx devices (138 GPIOs in the STM32F723xx devices) can be connected to the 16 external interrupt lines.

3.12 Clocks and startup

On reset the 16 MHz internal HSI RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 216 MHz. Similarly, a full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2), and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 216 MHz, while the maximum frequency of the high-speed APB domains is 108 MHz. The maximum allowed frequency of the low-speed APB domain is 54 MHz.

The devices embed two dedicated PLLs (PLLI2S and PLLSAI) which allow audio class performance to be achieved. In this case, the I^2S and SAI master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

The STM32F723xx devices embed two PLLs inside the PHY HS controller: PLL1 and PLL2. The PLL1 allows an output of 60 MHz used as an input for PLL2 which itself allows the generation of 480 Mbps in the USB OTG High Speed mode.

The PLL1 has as input HSE clock.

3.13 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing any boot memory address to be programmed from 0x0000 0000 to 0x3FFF FFFF, which includes:

- all flash address space mapped on ITCM or AXIM interface
- all RAM address space: ITCM, DTCM RAMs, and SRAMs mapped on AXIM interface
- system memory bootloader

The bootloader is located in system memory. It is used to reprogram the flash memory through a serial interface.

3.14 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through VDD pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: The V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to Section 3.15.2: Internal reset OFF). Refer to Table 3: Voltage regulator configuration mode versus device operating mode to identify the packages supporting this option.

- The $V_{DDSDMMC}$ can be connected either to V_{DD} or to an external independent power supply (1.8 to 3.6 V) for the SDMMC2 pins (clock, command, and 4-bit data).

For example, when the device is powered at 1.8 V, an independent power supply 2.7 V can be connected to $V_{DDSDMMC}$.When the $V_{DDSDMMC}$ is connected to a separated power supply, it is independent from V_{DD} or V_{DDA}, but it must be the last supply to be provided, and the first to disappear. The following conditions $V_{DDSDMMC}$ must be respected:

- During the power-on phase ($V_{DD} < V_{DD_MIN}$), $V_{DDSDMMC}$ must be always lower than V_{DD}.
- During the power-down phase ($V_{DD} < V_{DD_MIN}$), $V_{DDSDMMC}$ must be always lower than V_{DD}.
- The $V_{DDSDMMC}$ rising and falling time rate specifications must be respected.
- In the operating mode phase, $V_{DDSDMMC}$ can be lower or higher than V_{DD}:

  All associated GPIOs powered by $V_{DDSDMMC}$ are operating between $V_{DDSDMMC_MIN}$ and $V_{DDSDMMC_MAX}$.

- The V_{DDUSB} can be connected either to V_{DD} or to an external independent power supply (3.0 to 3.6 V) for USB transceivers (refer to *Figure 8* and *Figure 9*).
  For example, when the device is powered at 1.8 V, an independent power supply 3.3 V can be connected to the V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA}, but it must be the last supply to be provided, and the first to disappear. The following conditions V_{DDUSB} must be respected:
  - During the power-on phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} must be always lower than V_{DD}.
  - During the power-down phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} must be always lower than V_{DD}.
  - The V_{DDUSB} rising and falling time rate specifications must be respected.
  - In the operating mode phase, V_{DDUSB} can be lower or higher than V_{DD}:

    - If the USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.

    - The V_{DDUSB} supplies both USB transceiver (USB OTG_HS and USB OTG_FS). If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB}.

    - If the USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

Figure 8. V_{DDUSB} connected to V_{DD} power supply

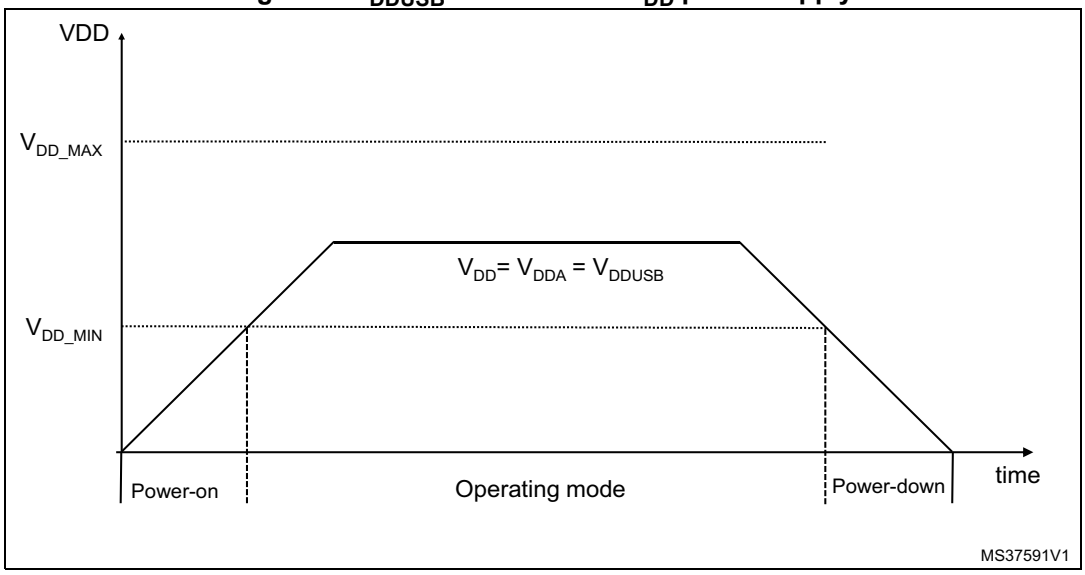
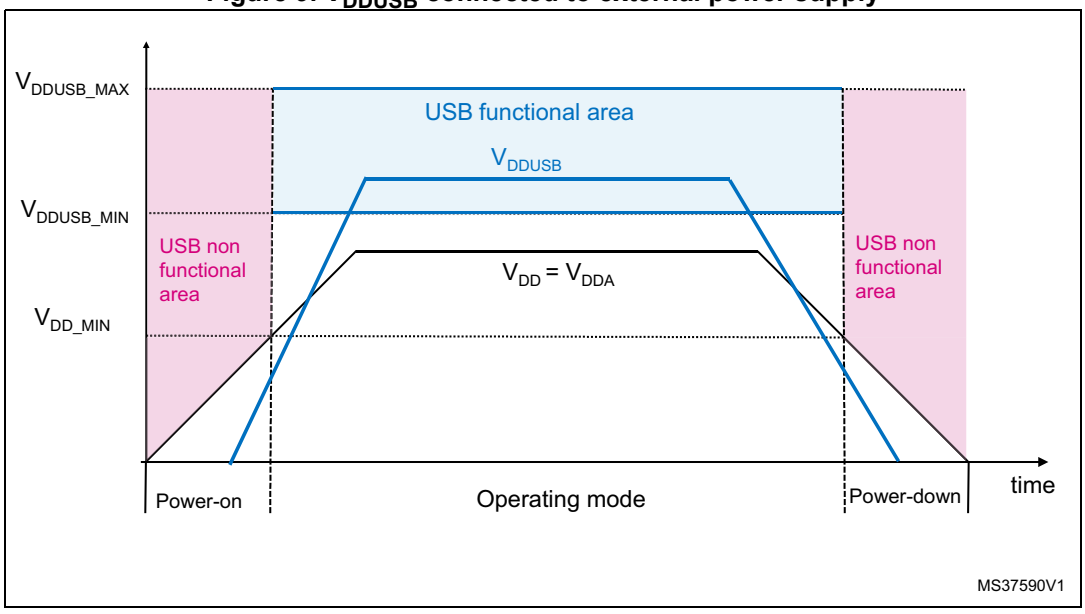


Figure 9. V_{DDUSB} connected to external power supply



On the STM32F7x3xx devices, the USB OTG HS subsystem uses one or two additional power supply pins depending on the package:

- The VDD12OTGHS pin is the output of PHY HS regulator (1.2 V). An external capacitor of 2.2 µF must be connected on the VDD12OTGHS pin.
- On the LQFP100 only, a second power pin VDDPHYHS is used to supply the USB OTG PHY HS and associated GPIOs.The VDDPHYHS follows the same rules provided for the VDDUSB power pin.

3.15 Power supply supervisor

3.15.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry coupled with a brownout reset (BOR) circuitry. At power-on, POR/PDR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

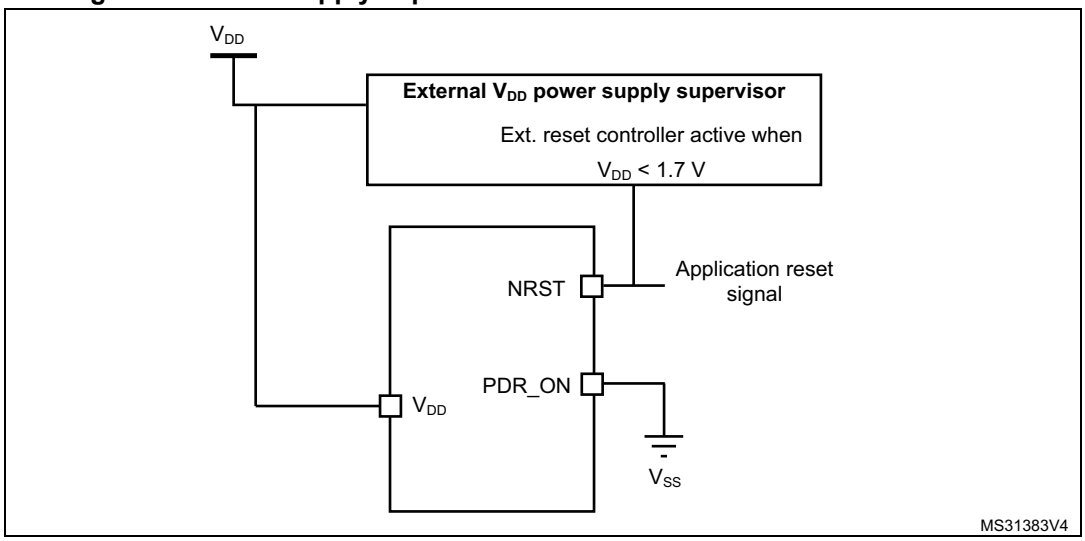
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply, and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold, and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.15.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal POR/PDR circuitry is disabled through the PDR_ON pin.

An external power supply supervisor monitors V_{DD} and NRST, and maintains the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON must be connected to V_{SS} (see the figure below).

Figure 10. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see *Figure 11*).

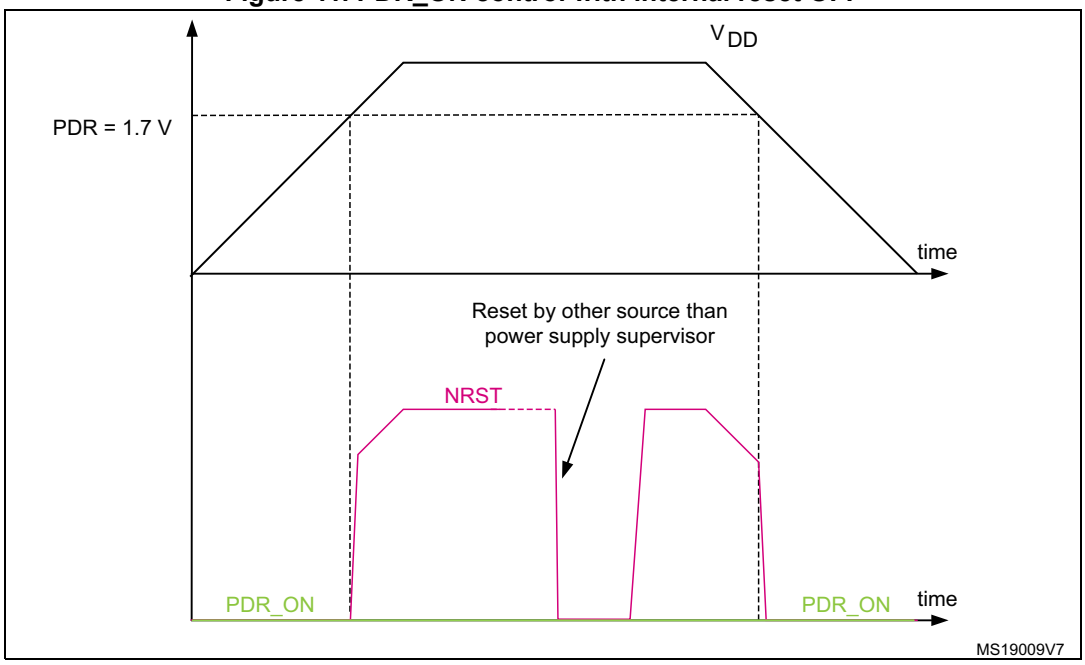
A comprehensive set of power-saving mode allows design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated POR/PDR circuitry is disabled.
- The BOR circuitry must be disabled.
- The embedded PVD is disabled.
- V_{BAT} functionality is no more available, and V_{BAT} pin must be connected to V_{DD}.

All packages, except the LQFP100, disables the internal reset through the PDR_ON signal when connected to V_{SS}.

Figure 11. PDR_ON control with internal reset OFF



3.16 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - main regulator mode (MR)
  - low-power regulator (LPR)
  - power-down
- Regulator OFF

3.16.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/Sleep modes, or in Stop modes:
  - In Run/Sleep modes

    The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). A different voltage scaling is provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
  - In Stop modes

    The MR can be configured in two ways during stop mode:

    - MR operates in normal mode (default mode of MR in Stop mode).
    - MR operates in under-drive mode (reduced leakage mode).
- LPR is used in Stop mode:

  The LP regulator mode is configured by software when entering Stop mode.

  Like the MR mode, the LPR can be configured in two ways during stop mode:
  - LPR operates in normal mode (default mode when LPR is ON).
  - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.

  The power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance, and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

V_{CAP_1} and V_{CAP_2} pins must be connected to 2 × 2.2 µF, ESR < 2 Ω (or 1 × 4.7 µF, ESR between 0.1 Ω and 0.2 Ω if only the V_{CAP_1} pin is provided (on LQFP64 package)).

All the packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

3.16.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode supplies externally a V_{12} voltage source through VCAP_1 and VCAP_2 pins.

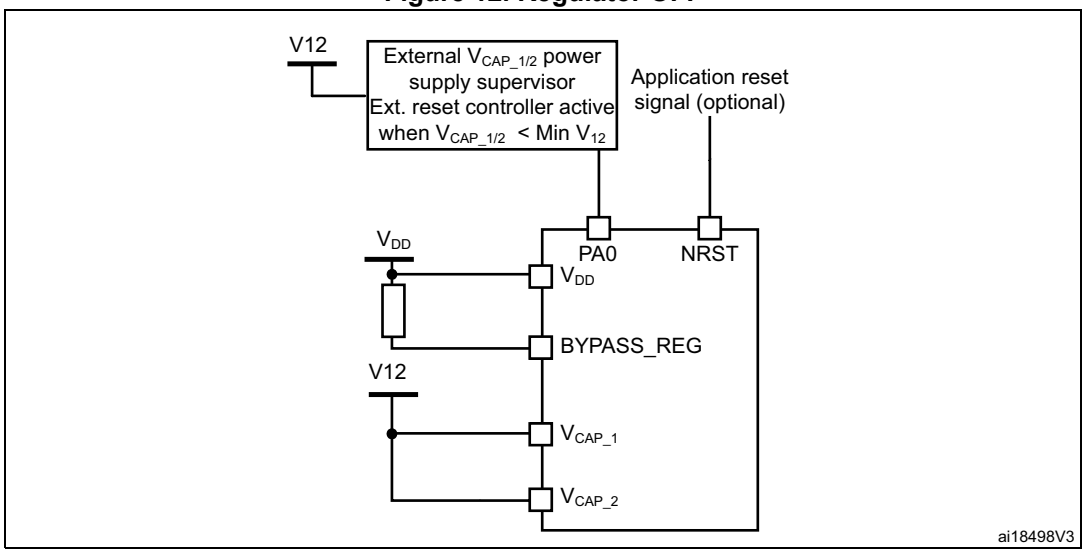
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.The two 2.2 µF ceramic capacitors must be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor can be used to monitor the V_{12} of the logic power domain. The PA0 pin can be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it is used to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

Figure 12. Regulator OFF

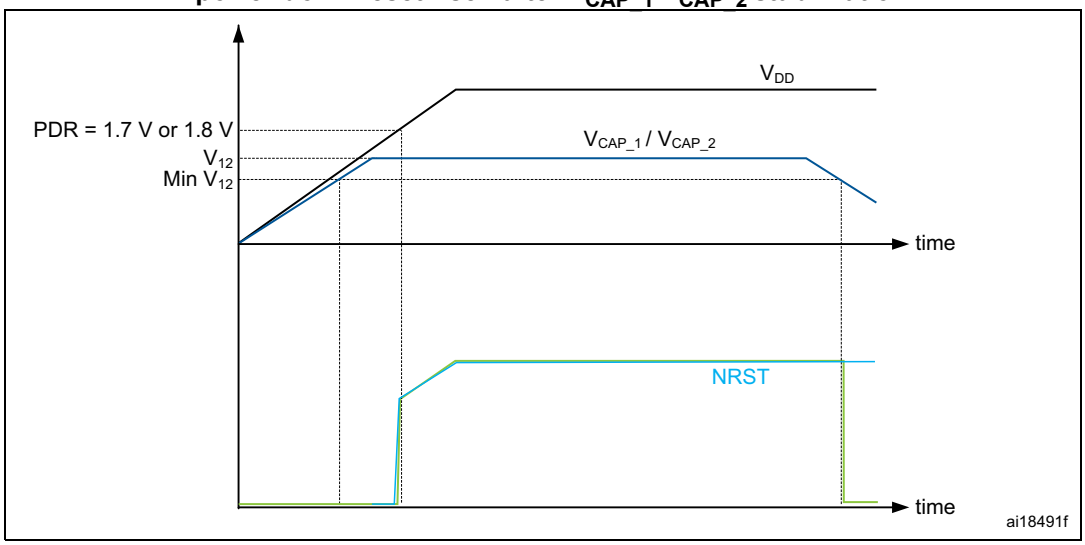


The following conditions must be respected:

- V_{DD} must always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 must be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 13*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 can be asserted low externally (see *Figure 14*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value, and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

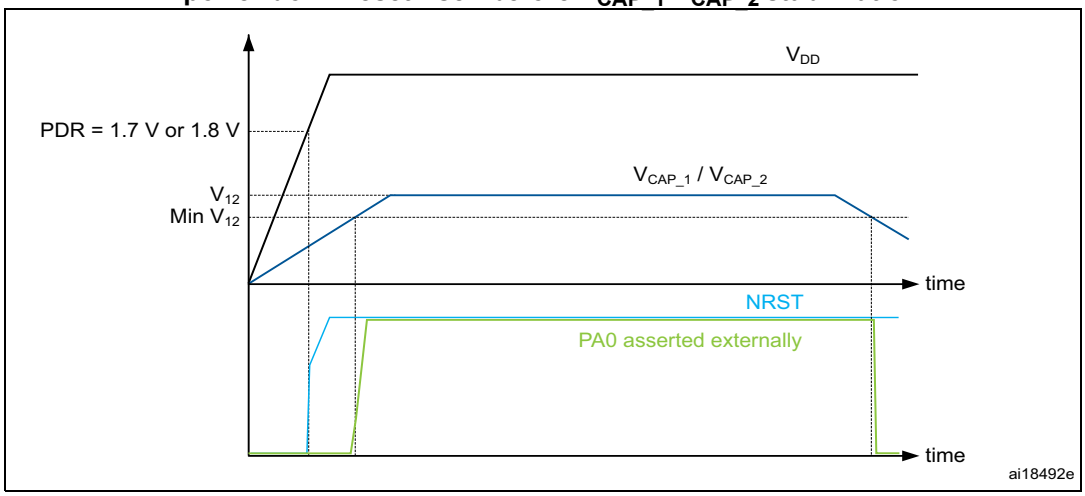
Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application. On the LQFP64 pin package, the V_{CAP_2} is not available.

Figure 13. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 14. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP64, LQFP100	Yes	No	Yes	No
LQFP144			Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP176, UFBGA144, UFBGA176	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

3.17 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- a 32.768 kHz external crystal (LSE)
- an external resonator or oscillator (LSE)
- the internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- the high-speed external clock (HSE) divided by 32

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All the RTC events (alarm, wakeup timer, timestamp, or tamper) can generate an interrupt, and wake up the device from the low-power modes.

3.18 Low-power modes

The devices support three low-power modes to achieve the best compromise between low-power consumption, short startup time, and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate, and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see *Table 5: Voltage regulator modes in Stop mode*):

  – normal mode (default mode when MR or LPR is enabled)

  – under-drive mode

  The device can be woken up from the Stop mode by any of the EXTI lines (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, wakeup, tamper, time stamp events, the USB OTG FS/HS wake up, and the LPTIM1 asynchronous interrupt).

Table 5. Voltage regulator modes in Stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off, so that the entire 1.2 V domain is powered off. The PLL, the HSI RC, and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain, and the backup SRAM when selected.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the six WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm, wakeup, tamper, time stamp event occurs.

  The Standby mode is not supported when the embedded voltage regulator is bypassed, and the 1.2 V domain is controlled by an external power.

3.19 V_{BAT} operation

The VBAT pin is used to power the device V_{BAT} domain from an external battery, an external super-capacitor, or from V_{DD} when no external battery and an external super-capacitor are present.

The V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC, the backup registers, and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When the PDR_ON pin is connected to V_{SS} (internal reset OFF), the V_{BAT} functionality is no more available, and the VBAT pin must be connected to V_{DD}.

3.20 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers, and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 6 compares the features of the advanced-control, general-purpose and basic timers.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	108	216

Table 6. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	108	216
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	108	216
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	54	108/216
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	54	108/216
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	54	108/216

1. The maximum timer clock is either 108 or 216 MHz, depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

3.20.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge- or center-aligned modes)
- one-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the timer Link feature for synchronization or event chaining.

The TIM1 and TIM8 support independent DMA request generation.

3.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F722xx and STM32F723xx devices (see *Table 6* for differences).

- TIM2, TIM3, TIM4, TIM5

  The STM32F722xx and STM32F723xx include four full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWM on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the timer link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

3.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for the DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

The TIM6 and TIM7 support independent DMA request generation.

3.20.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Selectable clock source:

- Internal clock source: LSE, LSI, HSI, or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the pulse-counter application)
- Programmable digital glitch filter
- Encoder mode

3.20.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.20.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.21 Inter-integrated circuit interface (I2C)

The devices embed three I2Cs. Refer to *Table 7: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Controller and target modes, multicontroller capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching

- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I^2C communication speed to be independent from the PCLK reprogramming.
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 7. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3
Standard-mode (up to 100 kbit/s)	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	X	X	X
Independent clock	X	X	X

1. X: supported.

3.22 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed USARTs. Refer to *Table 8: USART implementation* for the features implementation.

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

The USART peripheral supports:

- Full-duplex asynchronous communications
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Dual clock domain allowing convenient baud rate programming independent from the PCLK reprogramming
- A common programmable transmit and receive baud rate of up to 27 Mbit/s when USART clock source is system clock frequency (max is 216 MHz) and oversampling by eight is used.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits) word length
- Programmable data order with MSB-first or LSB-first shifting
- Programmable parity (odd, even, no parity)

- Configurable stop bits (1, 1.5, or 2 stop bits)
- Synchronous mode and clock output for synchronous communications
- Single-wire half-duplex communications
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Multiprocessor communications
- LIN master synchronous break send capability and LIN slave break detection capability
- IrDA SIR encoder decoder supporting 3/16 bit duration for normal mode
- Smartcard mode (T = 0 and T = 1 asynchronous protocols for Smartcards as defined in the ISO/IEC 7816-3 standard)
- Support for Modbus communication

Table 8 summarizes the implementation of all U(S)ARTs instances

Table 8. USART implementation

Features(1)	USART1/2/3/6	UART4/5/7/8
Data length	7, 8 and 9 bits	
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver enable	X	X

1. X: supported.

3.23 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I^2S)

The devices feature up to five SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, and SPI5 can communicate at up to 50 Mbit/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. The SPI interfaces support the NSS pulse mode, TI mode and Hardware CRC calculation. All the SPIs can be served by the DMA controller.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

3.24 Serial audio interface (SAI)

The devices embed two serial audio interfaces.

The serial audio interface is based on two independent audio subblocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I^2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both subblocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two subblocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 and SAI2 can be served by the DMA controller.

3.25 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S and SAI applications. It allows the achievement of an error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S/SAI sample rate change without disabling the main PLL (PLL) used for CPU and USB interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 lHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I^2S/SAI flow with an external PLL (or codec output).

3.26 Audio PLL (PLLSAI)

An additional PLL dedicated to audio is used for the SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

3.27 SD/SDIO/MMC card host interface (SDMMC)

SDMMC host interfaces are available, that support MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDMMC Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

3.28 Controller area network (bxCAN)

The CAN is compliant with the 2.0A and B (active) specifications with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. The CAN has three transmit mailboxes, two receive FIFOs with three stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated to the CAN.

3.29 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)
- BCD support

For the OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.30 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed an USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s).

The STM32F722xx devices feature a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The STM32F723xx devices feature an integrated PHY HS.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has a software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- **For STM32F722xx devices:** External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- **For STM32F723xx devices:** Internal HS OTG PHY support
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

Universal serial-bus controller on-the-go high-speed PHY controller (USBPHYC) only on STM32F723xx devices.

The USB HS PHY controller:

- Sets the PHYPLL1/2 values for the PHY HS.
- Sets the other controls on the PHY HS.
- Controls and monitors the USB PHY LDO.

3.31 True random number generator (RNG)

All the devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

3.32 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

A fast I/O handling allows a maximum I/O toggling up to 108 MHz.

3.33 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In the scan mode, an automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs can be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

3.34 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with the temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT}, ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part must be used.

3.35 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.36 Serial-wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial-wire debug port that enables either a serial-wire debug, or a JTAG probe to be connected to the target.

The debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be reused as GPIO with alternate function): JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

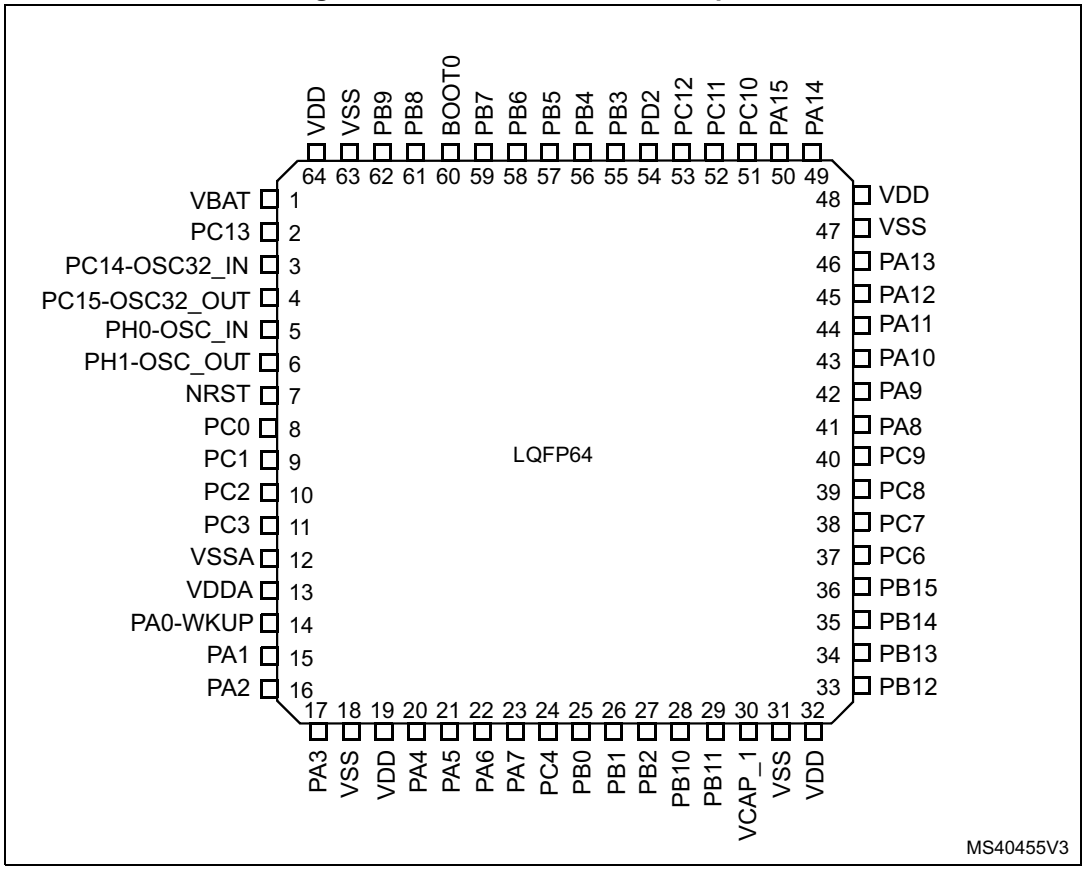
3.37 Embedded Trace Macrocell™

The Arm Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F722xx and STM32F723xx devices through a small number of ETM pins to an external hardware trace port analyser (TPA). The TPA is connected to a host computer using the USB or any other high-speed channel. The real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. The TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

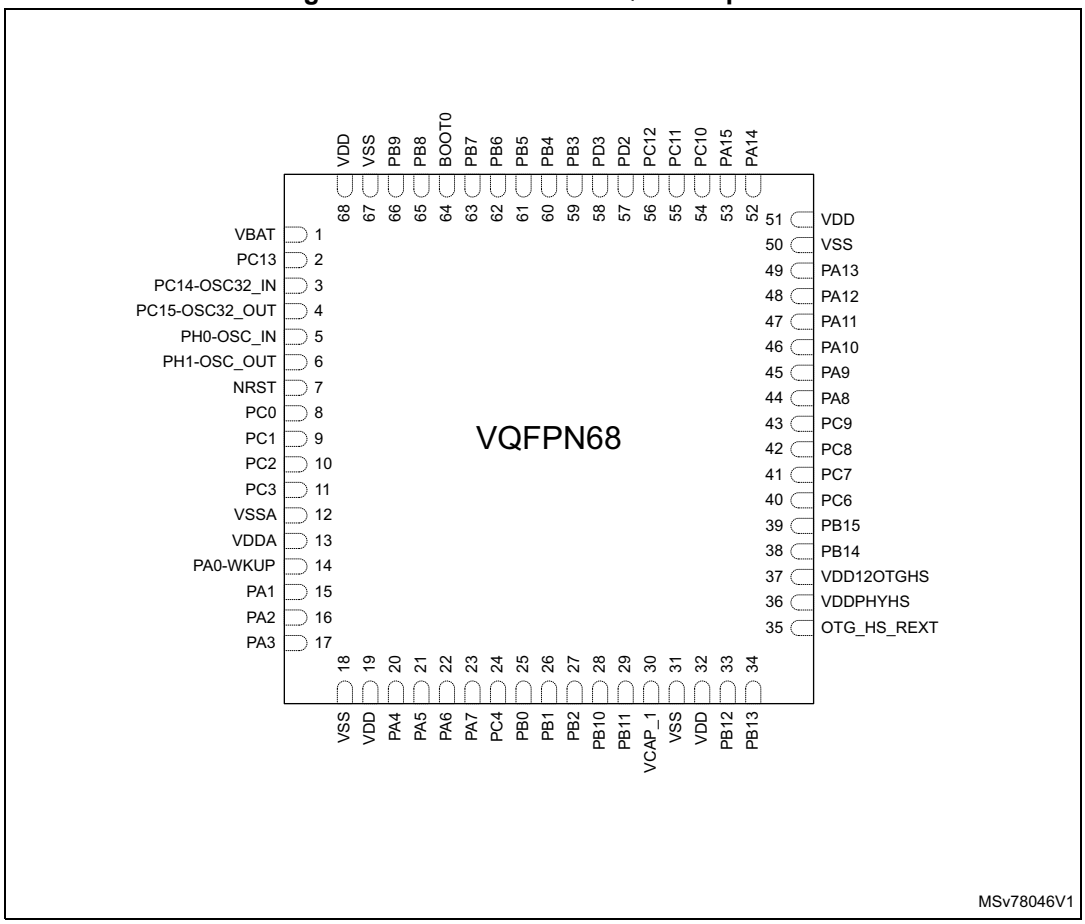
4 Pinouts and pin description

Figure 15. STM32F722xx LQFP64 pinout



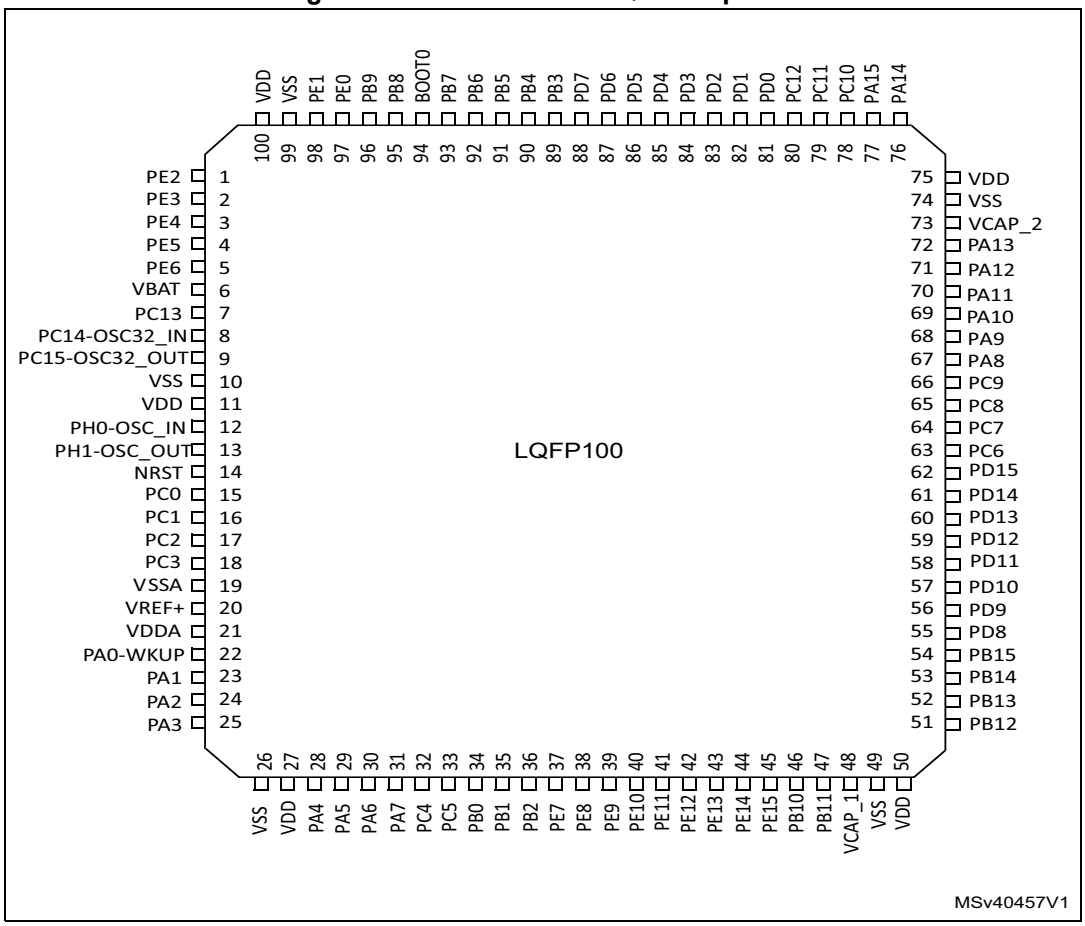
1. The above figure shows the package top view.

Figure 16. STM32F723xx VQFPN68 pinout



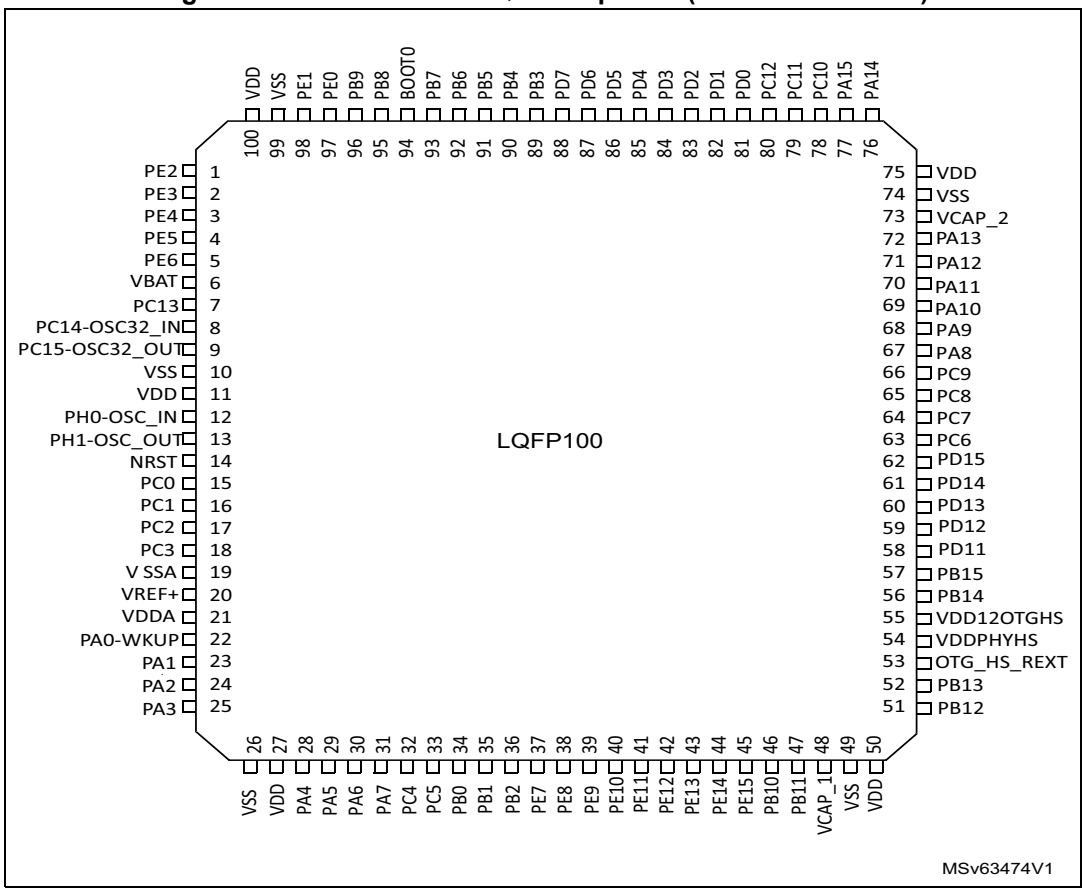
1. The above figure shows the package top view.

Figure 17. STM32F722xx LQFP100 pinout



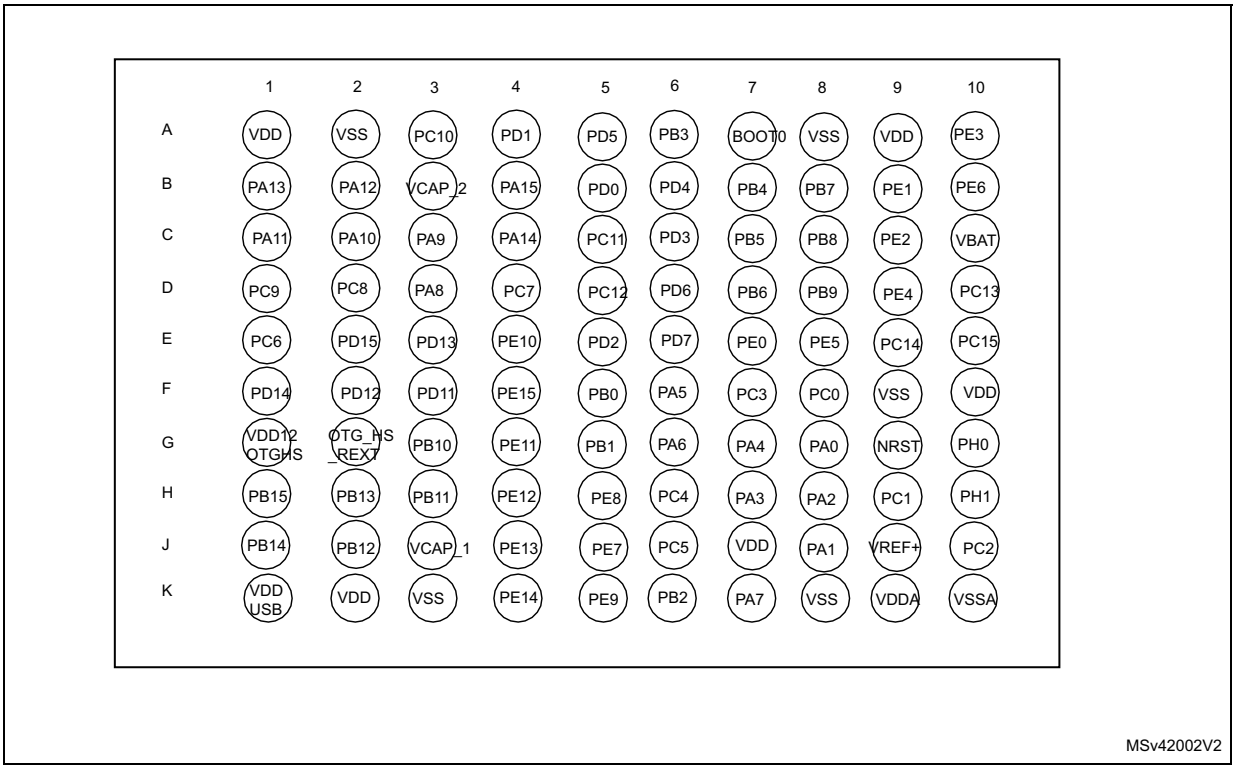
1. The above figure shows the package top view.

Figure 18. STM32F723xx LQFP100 pinout (with OTG PHY HS)



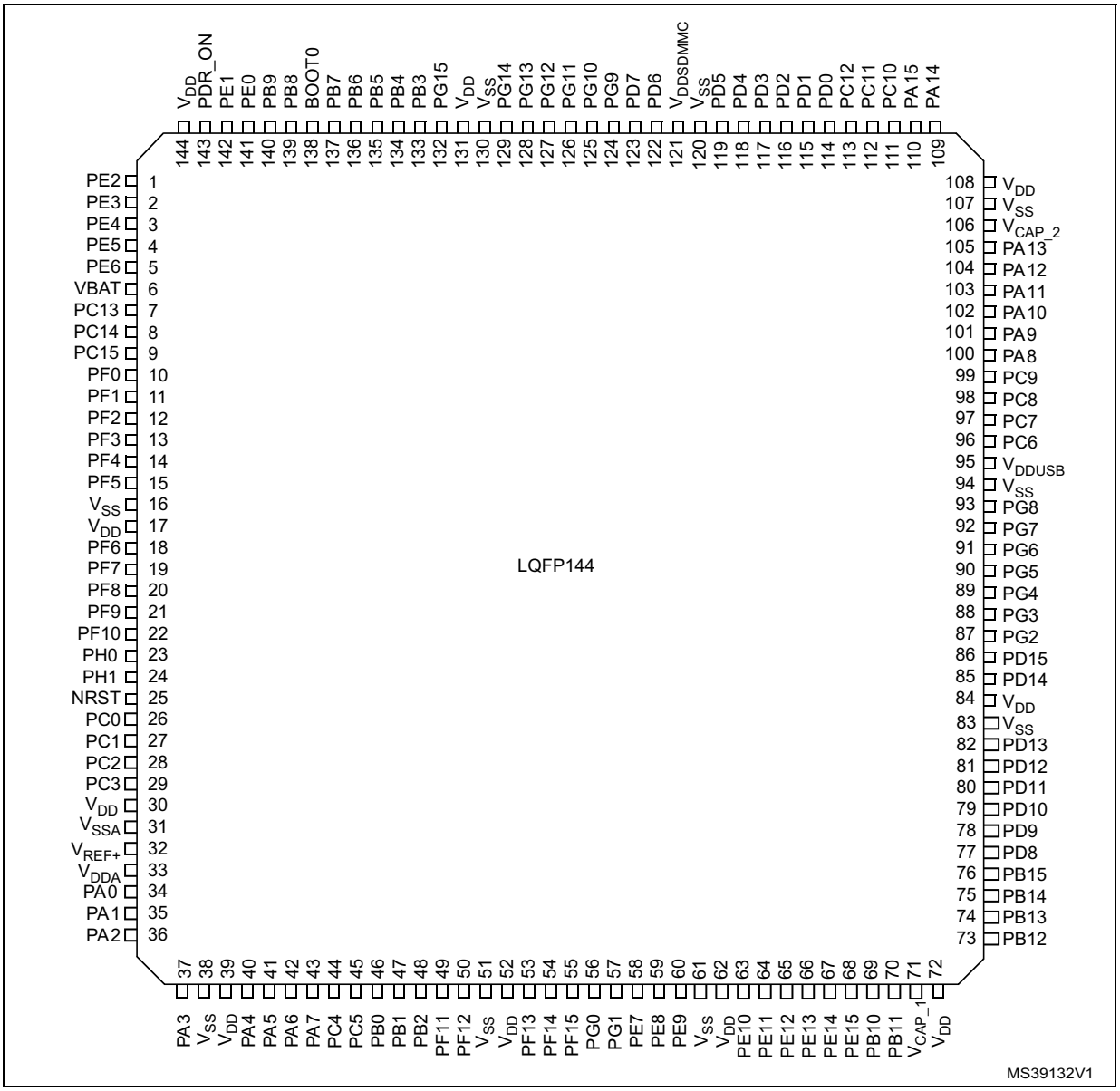
1. The above figure shows the package top view.

Figure 19. STM32F723xx WLCSP100 ballout (with OTG PHY HS)



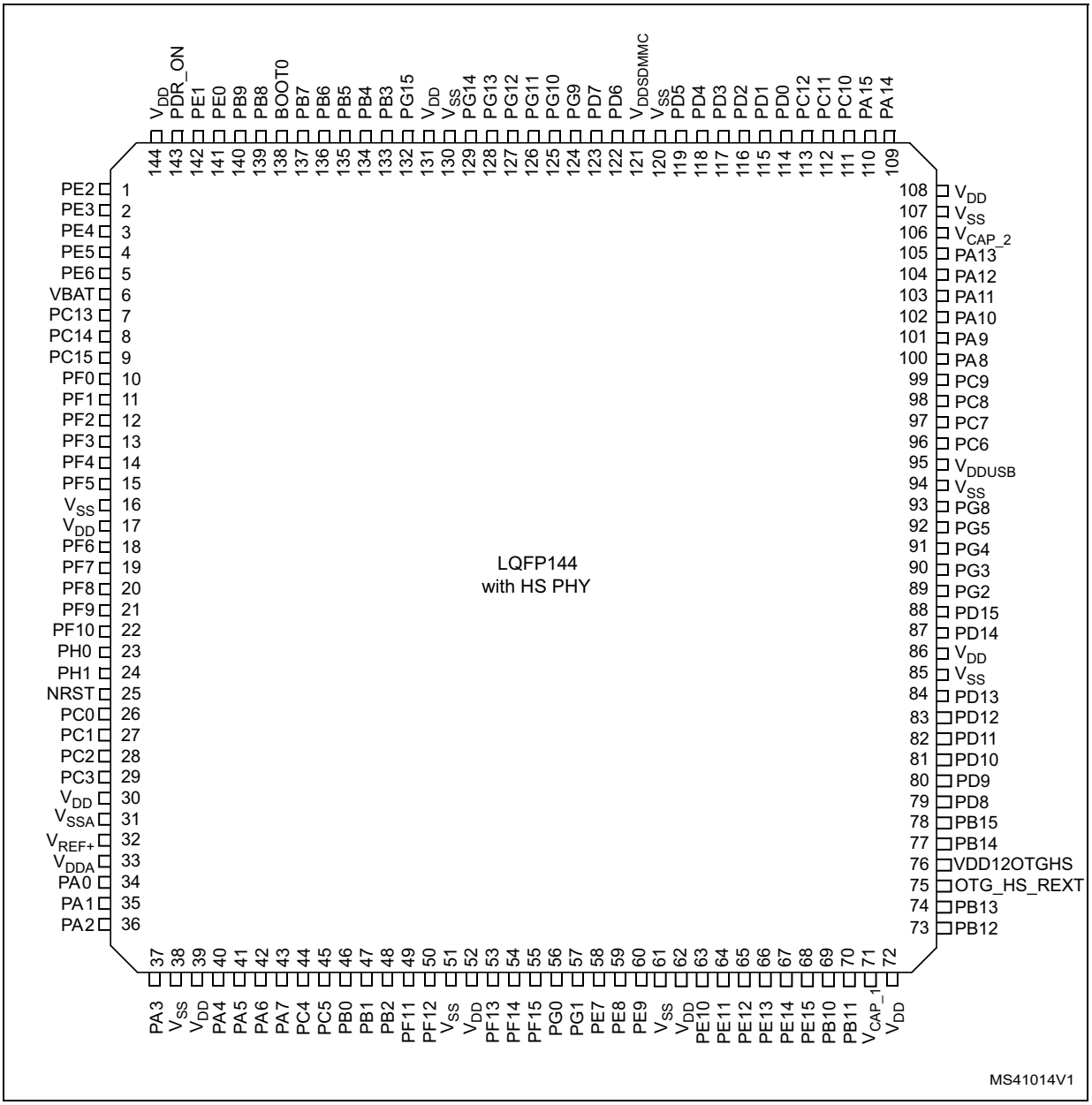
1. The above figure shows the package top view.

Figure 20. STM32F722xx LQFP144 pinout



1. The above figure shows the package top view.

Figure 21. STM32F723xx LQFP144 pinout (with OTG PHY HS)



1. The above figure shows the package top view.

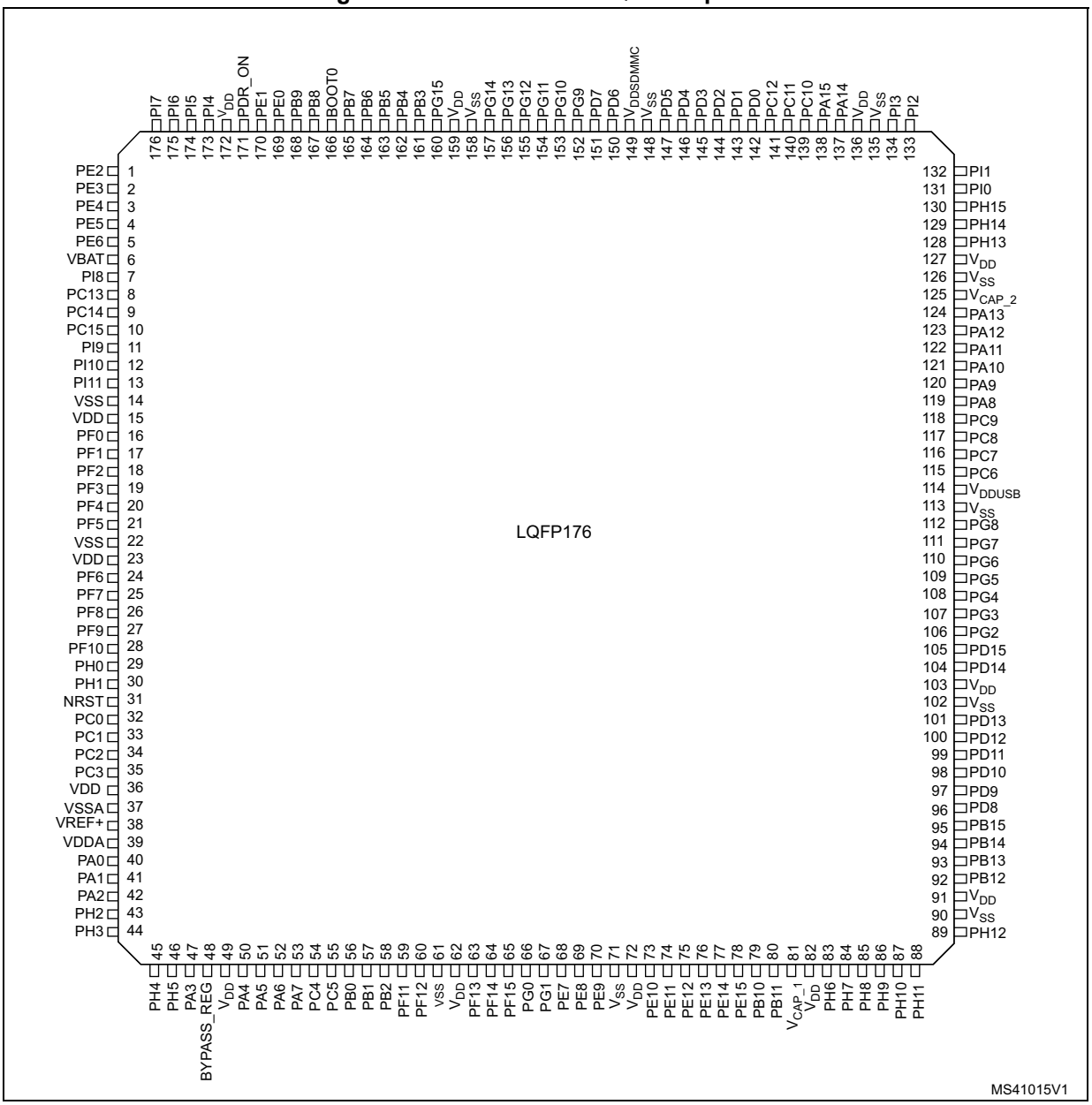
Figure 22. STM32F723xx UFBGA144 ballout (with OTG PHY HS)

	1	2	3	4	5	6	7	8	9	10	11	12
A	PC13	PE3	PE2	PE1	PE0	PB4	PB3	PD6	PD7	PA15	PA14	PA13
B	PC14-OSC32_IN	PE4	PE5	PE6	PB9	PB5	PG15	PG12	PD5	PC11	PC10	PA12
C	PC15-OSC32_OUT	VBAT	PF0	PF1	PB8	PB6	PG14	PG11	PD4	PC12	VDDUSB	PA11
D	PH0 - OSC_IN	VSS	VDD	PF2	BOOT0	PB7	PG13	PG10	PD3	PD1	PA10	PA9
E	PH1 - OSC_OUT	PF3	PF4	PF5	PDR_ON	VSS	VSS	PG9	PD2	PD0	PC9	PA8
F	NRST	PF7	PF6	VDD	VDD	VDD	VDD	VDD	VDD	VDD	PC8	PC7
G	PF10	PF9	PF8	VSS	VDD	VDD	VDD	VSS	VCAP_2	VSS	PG8	PC6
H	PC0	PC1	PC2	PC3	BYPASS_REG	VSS	VCAP_1	PE11	PD11	VDD12OTGHS	OTG_HS_REXT	PG5
J	VSSA	PA0	PA4	PC4	PB2	PG1	PE10	PE12	PD10	PG4	PG3	PG2
K	VREF-	PA1	PA5	PC5	PF13	PG0	PE9	PE13	PD9	PD13	PD14	PD15
L	VREF+	PA2	PA6	PB0	PF12	PF15	PE8	PE14	PD8	PD12	PB14	PB15
M	VDDA	PA3	PA7	PB1	PF11	PF14	PE7	PE15	PB10	PB11	PB12	PB13

MSv42000V1

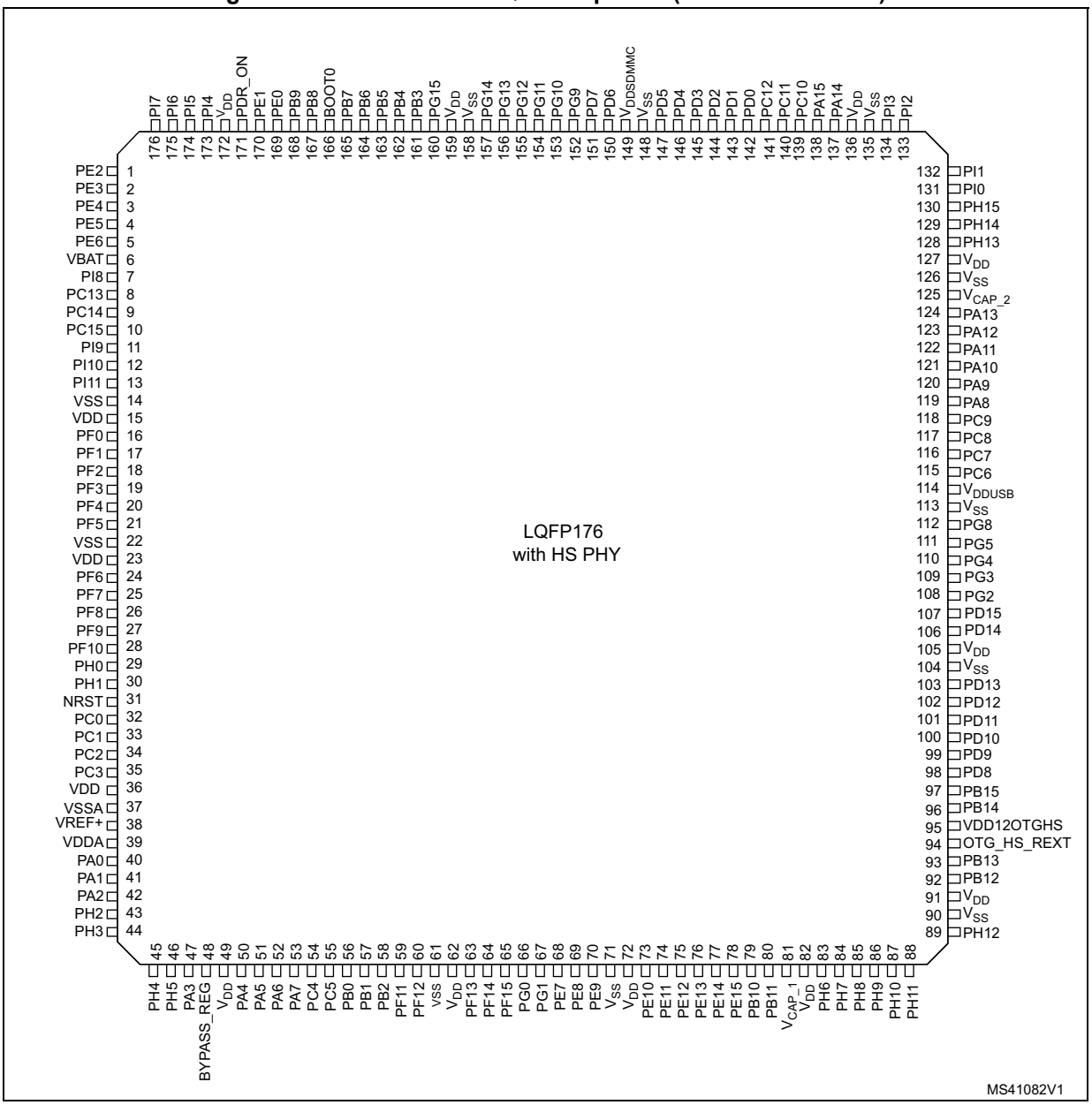
1. The above figure shows the package top view.

Figure 23. STM32F722xx LQFP176 pinout



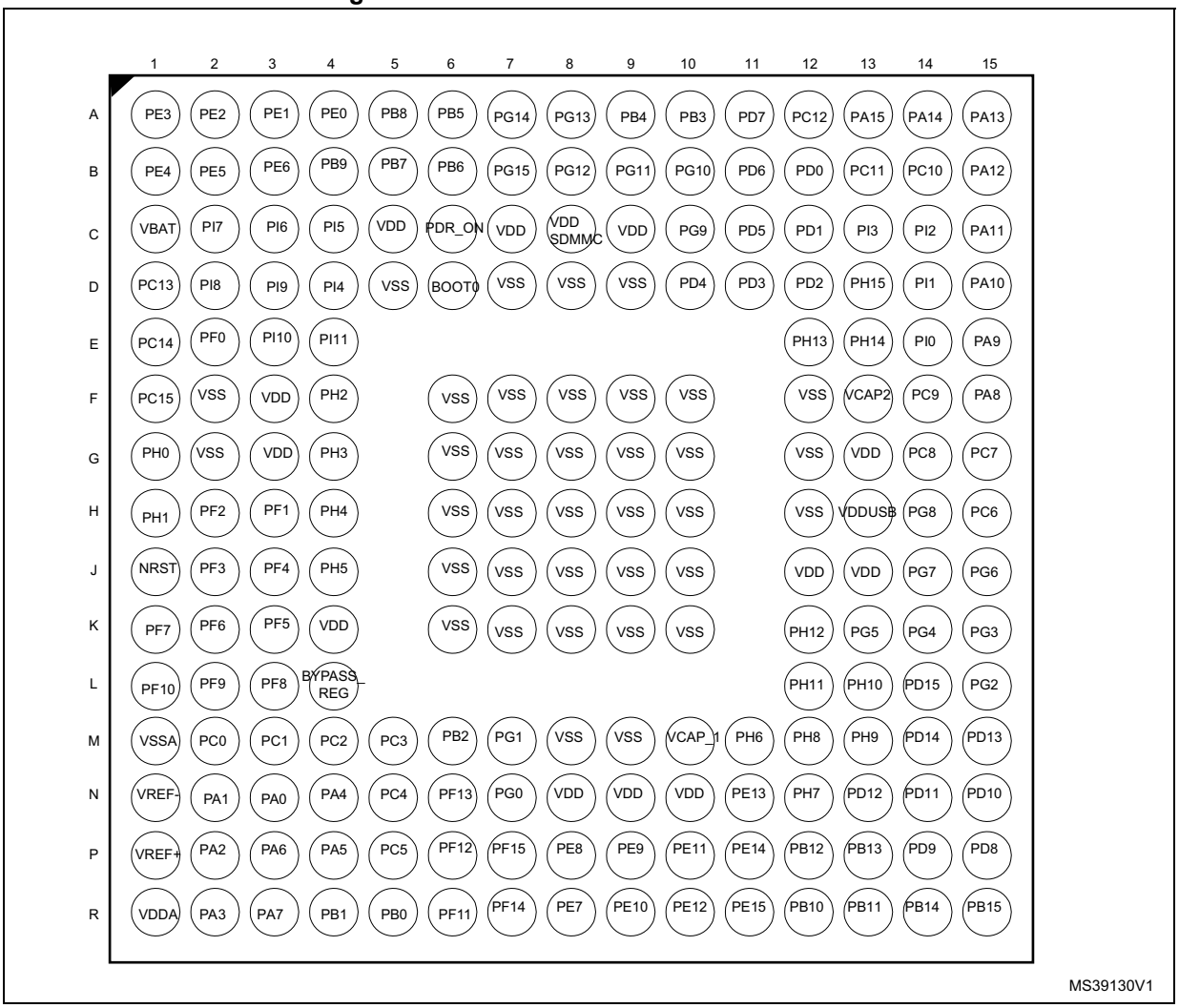
1. The above figure shows the package top view.

Figure 24. STM32F723xx LQFP176 pinout (with OTG PHY HS)



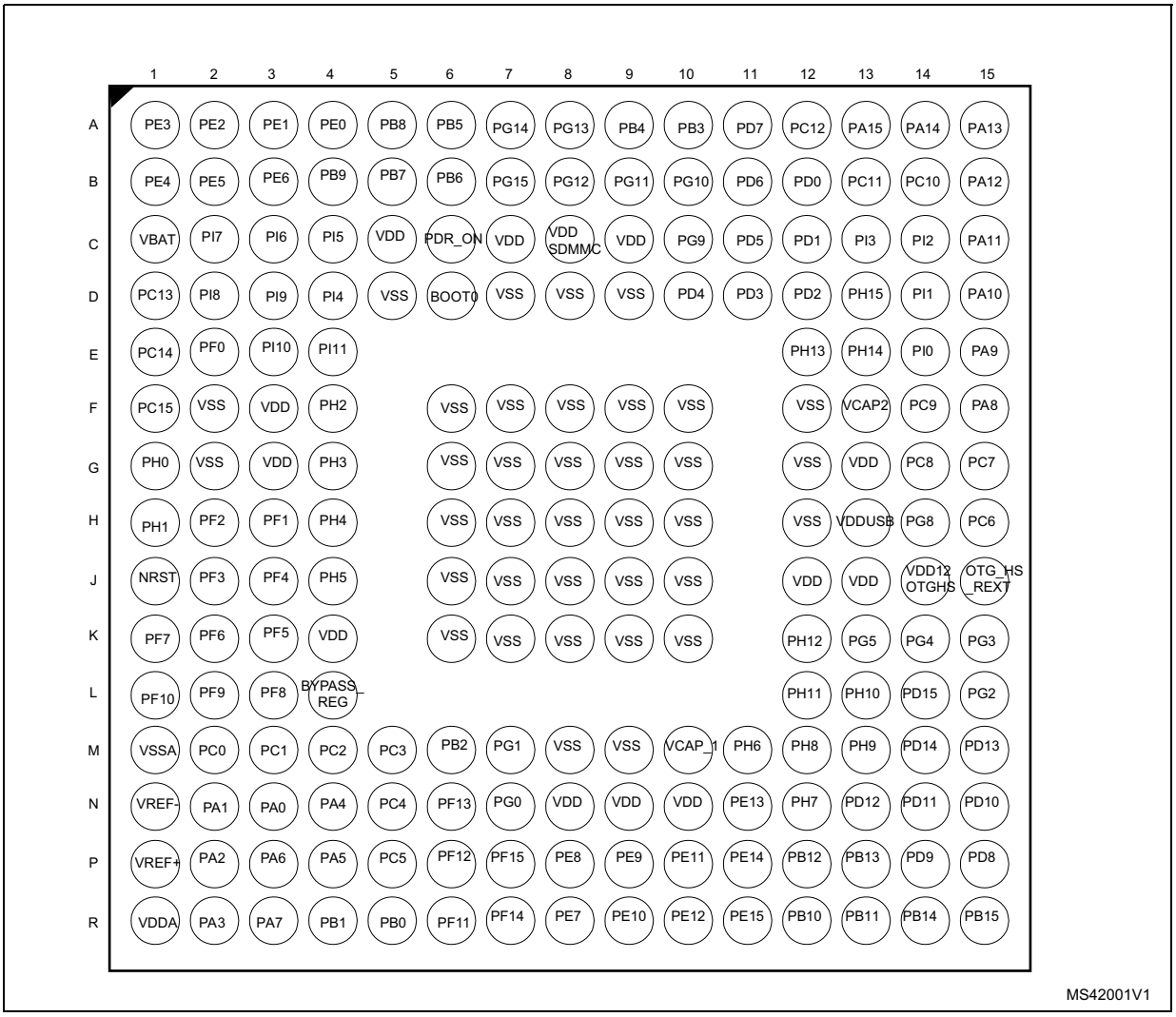
1. The above figure shows the package top view.

Figure 25. STM32F722xx UFBGA176 ballout



1. The above figure shows the package top view.

Figure 26. STM32F723xx UFBGA176 ballout (with OTG PHY HS)



1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5V tolerant I/O, I2C Fm+ option.
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F722xx and STM32F723xx pin and ball definition

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	1	1	A2	1	-[2]	1	C9	A2	A3	1	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, FMC_A23, EVENTOUT	-
-	2	2	A1	2	-[2]	2	A10	A1	A2	2	2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
-	3	3	B1	3	-[2]	3	D9	B1	B2	3	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, EVENTOUT	-
-	4	4	B2	4	-[2]	4	E8	B2	B3	4	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, EVENTOUT	-
-	5	5	B3	5	-[2]	5	B10	B3	B4	5	5	PE6	I/O	FT	-	TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCK_B, FMC_A22, EVENTOUT	-
1	6	6	C1	6	1	6	C10	C1	C2	6	6	VBAT	S	-	-	-	-
-	-	-	D2	7	-	-	-	D2	-	-	7	PI8	I/O	FT	(3) (4)	EVENTOUT	RTC_TAMP2/ RTC_TS, WKUP5

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
2	7	7	D1	8	2	7	D10	D1	A1	7	8	PC13	I/O	FT	(3) (4)	EVENTOUT	RTC_TAMP1/ RTC_TS/ RTC_OUT, WKUP4
3	8	8	E1	9	3	8	E9	E1	B1	8	9	PC14-OSC32_IN (PC14)	I/O	FT	(3) (4) (6)	EVENTOUT	OSC32_IN
4	9	9	F1	10	4	9	E10	F1	C1	9	10	PC15-OSC32_OUT (PC15)	I/O	FT	(3) (4) (6)	EVENTOUT	OSC32_OUT
-	-	-	D3	11	-	-	-	D3	-	-	11	PI9	I/O	FT	-	UART4_RX, CAN1_RX, FMC_D30, EVENTOUT	-
-	-	-	E3	12	-	-	-	E3	-	-	12	PI10	I/O	FT	-	FMC_D31, EVENTOUT	-
-	-	-	E4	13	-	-	-	E4	-	-	13	PI11	I/O	FT	(5)	OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	-	F2	14	-	-	-	F2	-	-	14	VSS	S	-	-	-	-
-	-	-	F3	15	-	-	-	F3	-	-	15	VDD	S	-	-	-	-
-	-	10	E2	16	-	-	-	E2	C3	10	16	PF0	I/O	FTf	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	11	H3	17	-	-	-	H3	C4	11	17	PF1	I/O	FTf	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	12	H2	18	-	-	-	H2	D4	12	18	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	13	J2	19	-	-	-	J2	E2	13	19	PF3	I/O	FT	-	FMC_A3, EVENTOUT	ADC3_IN9
-	-	14	J3	20	-	-	-	J3	E3	14	20	PF4	I/O	FT	-	FMC_A4, EVENTOUT	ADC3_IN14

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	15	K3	21	-	-	-	K3	E4	15	21	PF5	I/O	FT	-	FMC_A5, EVENTOUT	ADC3_IN15
-	10	16	G2	22	-	10	F9	G2	D2	16	22	VSS	S	-	-	-	-
-	11	17	G3	23	-	11	F10	G3	D3	17	23	VDD	S	-	-	-	-
-	-	18	K2	24	-	-	-	K2	F3	18	24	PF6	I/O	FT	-	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, QUADSPI_BK1_IO3, EVENTOUT	ADC3_IN4
-	-	19	K1	25	-	-	-	K1	F2	19	25	PF7	I/O	FT	-	TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, QUADSPI_BK1_IO2, EVENTOUT	ADC3_IN5
-	-	20	L3	26	-	-	-	L3	G3	20	26	PF8	I/O	FT	-	SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_IN6
-	-	21	L2	27	-	-	-	L2	G2	21	27	PF9	I/O	FT	-	SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_IN7
-	-	22	L1	28	-	-	-	L1	G1	22	28	PF10	I/O	FT	-	EVENTOUT	ADC3_IN8
5	12	23	G1	29	5	12	G10	G1	D1	23	29	PH0-OSC_IN	I/O	FT	(6)	EVENTOUT	OSC_IN

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
6	13	24	H1	30	6	13	H10	H1	E1	24	30	PH1-OSC_OUT	I/O	FT	(6)	EVENTOUT	OSC_OUT
7	14	25	J1	31	7	14	G9	J1	F1	25	31	NRST	I/O	RST	-	-	-
8	15	26	M2	32	8	15	F8	M2	H1	26	32	PC0	I/O	FT	(5)	SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT	ADC1_IN10, ADC2_IN10, ADC3_IN10
9	16	27	M3	33	9	16	H9	M3	H2	27	33	PC1	I/O	FT	-	TRACED0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, EVENTOUT	ADC1_IN11, ADC2_IN11, ADC3_IN11, RTC_TAMP3, WKUP3
10	17	28	M4	34	10	17	J10	M4	H3	28	34	PC2	I/O	FT	(5)	SPI2_MISO, OTG_HS_ULPI_DIR, FMC_SDNE0, EVENTOUT	ADC1_IN12, ADC2_IN12, ADC3_IN12
11	18	29	M5	35	11	18	F7	M5	H4	29	35	PC3	I/O	FT	(5)	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, FMC_SDCKE0, EVENTOUT	ADC1_IN13, ADC2_IN13, ADC3_IN13
-	-	30	-	36	-	-	J7	-	F10	30	36	VDD	S	-	-	-	-
12	19	31	M1	37	12	19	K10	M1	J1	31	37	VSSA	S	-	-	-	-
-	-	-	N1	-	-	-	-	N1	K1	-	-	VREF-	S	-	-	-	-
13	20	32	P1	38	-	20	J9	P1	L1	32	38	VREF+	S	-	-	-	-
-	21	33	R1	39	13	21	K9	R1	M1	33	39	VDDA	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
14	22	34	N3	40	14	22	G8	N3	J2	34	40	PA0-WKUP	I/O	FT	(6)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI2_SD_B, EVENTOUT	ADC1_IN0, ADC2_IN0, ADC3_IN0, WKUP1
15	23	35	N2	41	15	23	J8	N2	K2	35	41	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCK_B, EVENTOUT	ADC1_IN1, ADC2_IN1, ADC3_IN1
16	24	36	P2	42	16	24	H8	P2	L2	36	42	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, EVENTOUT	ADC1_IN2, ADC2_IN2, ADC3_IN2, WKUP2
-	-	-	F4	43	-	-	-	F4	-	-	43	PH2	I/O	FT	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, FMC_SDCKE0, EVENTOUT	-
-	-	-	G4	44	-	-	-	G4	-	-	44	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCK_B, FMC_SDNE0, EVENTOUT	-
-	-	-	H4	45	-	-	-	H4	-	-	45	PH4	I/O	FTf	(5)	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-
-	-	-	J4	46	-	-	-	J4	-	-	46	PH5	I/O	FTf	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
17	25	37	R2	47	17	25	H7	R2	M2	37	47	PA3	I/O	FT	(5)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, EVENTOUT	ADC1_IN3, ADC2_IN3, ADC3_IN3
18	26	38	-	-	18	26	K8	-	G4	38	-	VSS	S	-	-	-	-
-	-	-	L4	48	-	-	-	L4	H5	-	48	BYPASS_REG	I	FT	-	-	-
19	27	39	K4	49	19	27	-	K4	F4	39	49	VDD	S	-	-	-	-
20	28	40	N4	50	20	28	G7	N4	J3	40	50	PA4	I/O	TTa	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, EVENTOUT	ADC1_IN4, ADC2_IN4, DAC_OUT1
21	29	41	P4	51	21	29	F6	P4	K3	41	51	PA5	I/O	TTa	(5)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, OTG_HS_ULPI_CK, EVENTOUT	ADC1_IN5, ADC2_IN5, DAC_OUT2
22	30	42	P3	52	22	30	G6	P3	L3	42	52	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, EVENTOUT	ADC1_IN6, ADC2_IN6
23	31	43	R3	53	23	31	K7	R3	M3	43	53	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, FMC_SDNWE, EVENTOUT	ADC1_IN7, ADC2_IN7
24	32	44	N5	54	24	32	H6	N5	J4	44	54	PC4	I/O	FT	-	I2S1_MCK, FMC_SDNE0, EVENTOUT	ADC1_IN14, ADC2_IN14
-	33	45	P5	55	-[2]	33	J6	P5	K4	45	55	PC5	I/O	FT	-	FMC_SDCKE0, EVENTOUT	ADC1_IN15, ADC2_IN15

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
25	34	46	R5	56	25	34	F5	R5	L4	46	56	PB0	I/O	FT	(5)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, OTG_HS_ULPI_D1, EVENTOUT	ADC1_IN8, ADC2_IN8
26	35	47	R4	57	26	35	G5	R4	M4	47	57	PB1	I/O	FT	(5)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, EVENTOUT	ADC1_IN9, ADC2_IN9
27	36	48	M6	58	27	36	K6	M6	J5	48	58	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT	-
-	-	49	R6	59	-	-	-	R6	M5	49	59	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, EVENTOUT	-
-	-	50	P6	60	-	-	-	P6	L5	50	60	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	51	M8	61	-	-	-	M8	-	51	61	VSS	S	-	-	-	-
-	-	52	N8	62	-	-	-	N8	G5	52	62	VDD	S	-	-	-	-
-	-	53	N6	63	-	-	-	N6	K5	53	63	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	-	54	R7	64	-	-	-	R7	M6	54	64	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	-	55	P7	65	-	-	-	P7	L6	55	65	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	-	56	N7	66	-	-	-	N7	K6	56	66	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	-	57	M7	67	-	-	-	M7	J6	57	67	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-
-	37	58	R8	68	-[2]	37	J5	R8	M7	58	68	PE7	I/O	FT	-	TIM1_ETR, UART7_Rx, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	38	59	P8	69	-[2]	38	H5	P8	L7	59	69	PE8	I/O	FT	-	TIM1_CH1N, UART7_Tx, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
-	39	60	P9	70	-[2]	39	K5	P9	K7	60	70	PE9	I/O	FT	-	TIM1_CH1, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	-	61	M9	71	-	-	-	M9	H6	61	71	VSS	S	-	-	-	-
-	-	62	N9	72	-	-	-	N9	G6	62	72	VDD	S	-	-	-	-
-	40	63	R9	73	-[2]	40	E4	R9	J7	63	73	PE10	I/O	FT	-	TIM1_CH2N, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-
-	41	64	P10	74	-[2]	41	G4	P10	H8	64	74	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, SAI2_SD_B, FMC_D8, EVENTOUT	-
-	42	65	R10	75	-[2]	42	H4	R10	J8	65	75	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, SAI2_SCK_B, FMC_D9, EVENTOUT	-
-	43	66	N11	76	-[2]	43	J4	N11	K8	66	76	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, SAI2_FS_B, FMC_D10, EVENTOUT	-
-	44	67	P11	77	-[2]	44	K4	P11	L8	67	77	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11,, EVENTOUT	-
-	45	68	R11	78	-[2]	45	F4	R11	M8	68	78	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
28	46	69	R12	79	28	46	G3	R12	M9	69	79	PB10	I/O	FTf	(5)	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OTG_HS_ULPI_D3, EVENTOUT	-
29	47	70	R13	80	29	47	H3	R13	M10	70	80	PB11	I/O	FTf	(5)	TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, EVENTOUT	-
30	48	71	M10	81	30	48	J3	M10	H7	71	81	VCAP_1	S	-	-	-	-
31	49	-	-	-	31	49	K3	-	-	-	-	VSS	S	-	-	-	-
32	50	72	N10	82	32	50	K2	N10	G7	72	82	VDD	S	-	-	-	-
-	-	-	M11	83	-	-	-	M11	-	-	83	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, FMC_SDNE1, EVENTOUT	-
-	-	-	N12	84	-	-	-	N12	-	-	84	PH7	I/O	FTf	-	I2C3_SCL, SPI5_MISO, FMC_SDCKE1, EVENTOUT	-
-	-	-	M12	85	-	-	-	M12	-	-	85	PH8	I/O	FTf	-	I2C3_SDA, FMC_D16, EVENTOUT	-
-	-	-	M13	86	-	-	-	M13	-	-	86	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, EVENTOUT	-
-	-	-	L13	87	-	-	-	L13	-	-	87	PH10	I/O	FT	-	TIM5_CH1, FMC_D18, EVENTOUT	-
-	-	-	L12	88	-	-	-	L12	-	-	88	PH11	I/O	FT	-	TIM5_CH2, FMC_D19, EVENTOUT	-
-	-	-	K12	89	-	-	-	K12	-	-	89	PH12	I/O	FT	-	TIM5_CH3, FMC_D20, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	H12	90	-	-	-	H12	-	-	90	VSS	S	-	-	-	-
-	-	-	J12	91	-	-	K2	J12	-	-	91	VDD	S	-	-	-	-
33	51	73	P12	92	33	51	J2	P12	M11	73	92	PB12	I/O	FT	(5)	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, OTG_HS_ULPI_D5, OTG_HS_ID, EVENTOUT	-
34	52	74	P13	93	34	52	H2	P13	M12	74	93	PB13	I/O	FT	(5)	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, OTG_HS_ULPI_D6, EVENTOUT	OTG_HS_VBUS
-	-	-	-	-	35	53	G2	J15	H11	75	94	OTG_HS_REXT	-	-	-	USB HS OTG PHY calibration resistor	
-	-	-	-	-	36	54	-	-	-	-	-	VDDPHYHS	-	-	-	-	-
-	-	-	-	-	37	55	G1	J14	H10	76	95	VDD12OTGHS	-	-	-	-	-
35	53	75	R14	94	38	-	-	-	-	-	-	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, USART3_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
-	-	-	-	-	-	56	J1	R14	L11	77	96	PB14	I/O	FT	-	OTG_HS_DM	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
36	54	76	R15	95	-	-	-	-	-	-	-	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-
-	-	-	-	-	39	57	H1	R15	L12	78	97	PB15	I/O	FT	-	OTG_HS_DP	-
-	55	77	P15	96	-	-	-	P15	L9	79	98	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
-	56	78	P14	97	-	-	-	P14	K9	80	99	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
-	57	79	N15	98	-	-	-	N15	J9	81	100	PD10	I/O	FT	-	USART3_CK, FMC_D15, EVENTOUT	-
-	58	80	N14	99	-[2]	58	F3	N14	H9	82	101	PD11	I/O	FT	-	USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
-	59	81	N13	100	-[2]	59	F2	N13	L10	83	102	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
-	60	82	M15	101	-[2]	60	E3	M15	K10	84	103	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	-	83	-	102	-	-	-	-	G8	85	104	VSS	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	84	J13	103	-	-	-	J13	F8	86	105	VDD	S	-	-	-	-
-	61	85	M14	104	-[2]	61	F1	M14	K11	87	106	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
-	62	86	L14	105	-[2]	62	E2	L14	K12	88	107	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	87	L15	106	-	-	-	L15	J12	89	108	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	-	88	K15	107	-	-	-	K15	J11	90	109	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	-	89	K14	108	-	-	-	K14	J10	91	110	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	-	90	K13	109	-	-	-	K13	H12	92	111	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	-	91	J15	110	-	-	-	-	-	-	-	PG6	I/O	FT	-	EVENTOUT	-
-	-	92	J14	111	-	-	-	-	-	-	-	PG7	I/O	FT	-	USART6_CK, FMC_INT, EVENTOUT	-
-	-	93	H14	112	-	-	-	H14	G11	93	112	PG8	I/O	FT	-	USART6_RTS, FMC_SDCLK, EVENTOUT	-
-	-	94	G12	113	-	-	-	G12	-	94	113	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	F10	-	-	VDD	-	-	-	-	-
-	-	95	H13	114	-	-	K1	H13	C11	95	114	VDDUSB	S	-	-	-	-
37	63	96	H15	115	40	63	E1	H15	G12	96	115	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDMMC2_D6, SDMMC1_D6, EVENTOUT	-
38	64	97	G15	116	41	64	D4	G15	F12	97	116	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDMMC2_D7, SDMMC1_D7, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
39	65	98	G14	117	42	65	D2	G14	F11	98	117	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, EVENTOUT	-
40	66	99	F14	118	43	66	D1	F14	E11	99	118	PC9	I/O	FTf	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, EVENTOUT	-
41	67	100	F15	119	44	67	D3	F15	E12	100	119	PA8	I/O	FTf	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, EVENTOUT	-
42	68	101	E15	120	45	68	C3	E15	D12	101	120	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, EVENTOUT	OTG_FS_VBUS
43	69	102	D15	121	46	69	C2	D15	D11	102	121	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, EVENTOUT	-
44	70	103	C15	122	47	70	C1	C15	C12	103	122	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
45	71	104	B15	123	48	71	B2	B15	B12	104	123	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	72	105	A15	124	49	72	B1	A15	A12	105	124	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
-	73	106	F13	125	-	73	B3	F13	G9	106	125	VCAP_2	S	-	-	-	-
47	74	107	F12	126	50	74	A2	F12	G10	107	126	VSS	S	-	-	-	-
48	75	108	G13	127	51	75	A1	G13	F9	108	127	VDD	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68(2)	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	E12	128	-	-	-	E12	-	-	128	PH13	I/O	FT	-	TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, EVENTOUT	-
-	-	-	E13	129	-	-	-	E13	-	-	129	PH14	I/O	FT	-	TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, EVENTOUT	-
-	-	-	D13	130	-	-	-	D13	-	-	130	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, EVENTOUT	-
-	-	-	E14	131	-	-	-	E14	-	-	131	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, EVENTOUT	-
-	-	-	D14	132	-	-	-	D14	-	-	132	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, EVENTOUT	-
-	-	-	C14	133	-	-	-	C14	-	-	133	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, FMC_D26, EVENTOUT	-
-	-	-	C13	134	-	-	-	C13	-	-	134	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, EVENTOUT	-
-	-	-	D9	135	-	-	-	D9	-	-	135	VSS	S	-	-	-	-
-	-	-	C9	136	-	-	-	C9	-	-	136	VDD	S	-	-	-	-
49	76	109	A14	137	52	76	C4	A14	A11	109	137	PA14 (JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
50	77	110	A13	138		77	B4	A13	A10	110	138	PA15 (JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, UART4_RTS, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
51	78	111	B14	139	53	78	A3	B14	B11	111	139	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, EVENTOUT	-
52	79	112	B13	140	54	79	C5	B13	B10	112	140	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, EVENTOUT	-
53	80	113	A12	141	55	80	D5	A12	C10	113	141	PC12	I/O	FT	-	TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, EVENTOUT	-
-	81	114	B12	142	56	81	B5	B12	E10	114	142	PD0	I/O	FT	-	CAN1_RX, FMC_D2, EVENTOUT	-
-	82	115	C12	143	-[2]	82	A4	C12	D10	115	143	PD1	I/O	FT	-	CAN1_TX, FMC_D3, EVENTOUT	-
54	83	116	D12	144	-[2]	83	E5	D12	E9	116	144	PD2	I/O	FT	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, EVENTOUT	-
-	84	117	D11	145	57	84	C6	D11	D9	117	145	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, EVENTOUT	-
-	85	118	D10	146	58	85	B6	D10	C9	118	146	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-
-	86	119	C11	147	-[2]	86	A5	C11	B9	119	147	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	-	120	D8	148	-[2]	-	-	D8	E7	120	148	VSS	S	-	-	-	-
-	-	121	C8	149	-	-	-	C8	F7	121	149	VDDSDMMC	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	87	122	B11	150	-	87	D6	B11	A8	122	150	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, SDMMC2_CK, FMC_NWAIT, EVENTOUT	-
-	88	123	A11	151	-[2]	88	E6	A11	A9	123	151	PD7	I/O	FT	-	USART2_CK SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	124	C10	152	-[2]	-	-	C10	E8	124	152	PG9	I/O	FT	-	USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, SDMMC2_D0, FMC_NE2/FMC_NCE, EVENTOUT	-
-	-	125	B10	153	-	-	-	B10	D8	125	153	PG10	I/O	FT	-	SAI2_SD_B, SDMMC2_D1, FMC_NE3, EVENTOUT	-
-	-	126	B9	154	-	-	-	B9	C8	126	154	PG11	I/O	FT	-	SDMMC2_D2, FMC_INT, EVENTOUT	-
-	-	127	B8	155	-	-	-	B8	B8	127	155	PG12	I/O	FT	-	LPTIM1_IN1, USART6_RTS, SDMMC2_D3, FMC_NE4, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	128	A8	156	-	-	-	A8	D7	128	156	PG13	I/O	FT	-	TRACED0, LPTIM1_OUT, USART6_CTS, FMC_A24, EVENTOUT	-
-	-	129	A7	157	-	-	-	A7	C7	129	157	PG14	I/O	FT	-	TRACED1, LPTIM1_ETR, USART6_TX, QUADSPI_BK2_IO3, FMC_A25, EVENTOUT	-
-	-	130	D7	158	-	-	-	D7	-	130	158	VSS	S	-	-	-	-
-	-	131	C7	159	-	-	-	C7	F6	131	159	VDD	S	-	-	-	-
-	-	132	B7	160	-	-	-	B7	B7	132	160	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, EVENTOUT	-
55	89	133	A10	161	-	89	A6	A10	A7	133	161	PB3 (JTDO/ TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SDMMC2_D2, EVENTOUT	-
56	90	134	A9	162	59	90	B7	A9	A6	134	162	PB4 (NJTRST)	I/O	FT	-	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, SPI2_NSS/I2S2_WS, SDMMC2_D3, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
57	91	135	A6	163	60	91	C7	A6	B6	135	163	PB5	I/O	FT	(5)	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, OTG_HS_ULPI_D7, FMC_SDCKE1, EVENTOUT	-
58	92	136	B6	164	61	92	D7	B6	C6	136	164	PB6	I/O	FTf	-	TIM4_CH1, I2C1_SCL, USART1_TX, QUAD SPI_BK1_NCS, FMC_SDNE1, EVENTOUT	-
59	93	137	B5	165	62	93	B8	B5	D6	137	165	PB7	I/O	FTf	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, EVENTOUT	-
60	94	138	D6	166	63	94	A7	D6	D5	138	166	BOOT	I	B	-	-	VPP
61	95	139	A5	167	64	95	C8	A5	C5	139	167	PB8	I/O	FTf	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, SDMMC2_D4, SDMMC1_D4, EVENTOUT	-
62	96	140	B4	168	65	96	D8	B4	B5	140	168	PB9	I/O	FTf	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDMMC2_D5, SDMMC1_D5, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	97	141	A4	169	66	97	E7	A4	A5	141	169	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_Rx, SAI2_MCK_A, FMC_NBL0, EVENTOUT	-
-	98	142	A3	170	-[2]	98	B9	A3	A4	142	170	PE1	I/O	FT	-	LPTIM1_IN2, UART8_Tx, FMC_NBL1, EVENTOUT	-
63	99	-	D5	-	-[2]	99	A8	D5	E6	-	-	VSS	S	-	-	-	-
-	-	143	C6	171	67	-	-	C6	E5	143	171	PDR_ON	S	-	-	-	-
64	100	144	C5	172	-	100	A9	C5	F5	144	172	VDD	S	-	-	-	-
-	-	-	D4	173	68	-	-	D4	-	-	173	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCK_A, FMC_NBL2, EVENTOUT	-
-	-	-	C4	174	-	-	-	C4	-	-	174	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, EVENTOUT	-
-	-	-	C3	175	-	-	-	C3	-	-	175	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68[2]	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	C2	176	-	-	-	C2	-	-	176	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, EVENTOUT	-
-	-	-	F6	-	-	-	-	F6	-	-	-	VSS	S	-	-	-	-
-	-	-	F7	-	-	-	-	F7	-	-	-	VSS	S	-	-	-	-
-	-	-	F8	-	-	-	-	F8	-	-	-	VSS	S	-	-	-	-
-	-	-	F9	-	-	-	-	F9	-	-	-	VSS	S	-	-	-	-
-	-	-	F10	-	-	-	-	F10	-	-	-	VSS	S	-	-	-	-
-	-	-	G6	-	-	-	-	G6	-	-	-	VSS	S	-	-	-	-
-	-	-	G7	-	-	-	-	G7	-	-	-	VSS	S	-	-	-	-
-	-	-	G8	-	-	-	-	G8	-	-	-	VSS	S	-	-	-	-
-	-	-	G9	-	-	-	-	G9	-	-	-	VSS	S	-	-	-	-
-	-	-	G10	-	-	-	-	G10	-	-	-	VSS	S	-	-	-	-
-	-	-	H6	-	-	-	-	H6	-	-	-	VSS	S	-	-	-	-
-	-	-	H7	-	-	-	-	H7	-	-	-	VSS	S	-	-	-	-
-	-	-	H8	-	-	-	-	H8	-	-	-	VSS	S	-	-	-	-
-	-	-	H9	-	-	-	-	H9	-	-	-	VSS	S	-	-	-	-
-	-	-	H10	-	-	-	-	H10	-	-	-	VSS	S	-	-	-	-
-	-	-	J6	-	-	-	-	J6	-	-	-	VSS	S	-	-	-	-
-	-	-	J7	-	-	-	-	J7	-	-	-	VSS	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin number												Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx												
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	VQFPN68(2)	LQFP100	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	J8	-	-	-	-	J8	-	-	-	VSS	S	-	-	-	-
-	-	-	J9	-	-	-	-	J9	-	-	-	VSS	S	-	-	-	-
-	-	-	J10	-	-	-	-	J10	-	-	-	VSS	S	-	-	-	-
-	-	-	K6	-	-	-	-	K6	-	-	-	VSS	S	-	-	-	-
-	-	-	K7	-	-	-	-	K7	-	-	-	VSS	S	-	-	-	-
-	-	-	K8	-	-	-	-	K8	-	-	-	VSS	S	-	-	-	-
-	-	-	K9	-	-	-	-	K9	-	-	-	VSS	S	-	-	-	-
-	-	-	K10	-	-	-	-	K10	-	-	-	VSS	S	-	-	-	-

1. Function availability depends on the chosen device.
2. NC (not connected) pins are not bonded. To prevent additional current consumption during low-power modes, these pins must be configured in software as push-pull outputs and explicitly driven low by setting their corresponding output data register bits to 0.

   The affected pins are: PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PC5, PD0, PD1, PD4, PD5, PD6, PD7, PD11, PD12, PD13, PD14, and PD15.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:

   - The speed should not exceed 2 MHz with a maximum load of 30 pF.

   - These I/Os must not be used as a current source (e.g. to drive an LED).
4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset).
5. ULPI signals not available on the STM32F723xx devices.
6. If the device is in regulator OFF/internal reset ON mode (BYPASS_REG pin is set to VDD), then PA0 is used as an internal reset (active low).

Table 11. FMC pin definition

Pin name	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	-
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	DA8	D8	D8
PE12	D9	DA9	D9	D9
PE13	D10	DA10	D10	D10
PE14	D11	DA11	D11	D11
PE15	D12	DA12	D12	D12
PD8	D13	DA13	D13	D13
PD9	D14	DA14	D14	D14
PD10	D15	DA15	D15	D15
PH8	D16	-	-	D16
PH9	D17	-	-	D17
PH10	D18	-	-	D18
PH11	D19	-	-	D19
PH12	D20	-	-	D20
PH13	D21	-	-	D21
PH14	D22	-	-	D22
PH15	D23	-	-	D23
PI0	D24	-	-	D24
PI1	D25	-	-	D25
PI2	D26	-	-	D26
PI3	D27	-	-	D27
PI6	D28	-	-	D28
PI7	D29	-	-	D29
PI9	D30	-	-	D30
PI10	D31	-	-	D31
PD7	NE1	NE1	-	-
PG9	NE2	NE2	NCE	-
PG10	NE3	NE3	-	-
PG11	-	-	-	-
PG12	NE4	NE4	-	-
PD3	CLK	CLK	-	-
PD4	NOE	NOE	NOE	-
PD5	NWE	NWE	NWE	-
PD6	NWAIT	NWAIT	NWAIT	-
PB7	NADV	NADV	-	-

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF6	-	-	-	-
PF7	-	-	-	-
PF8	-	-	-	-
PF9	-	-	-	-
PF10	-	-	-	-
PG6	-	-	-	-
PG7	-	-	INT	-
PE0	NBL0	NBL0	-	NBL0
PE1	NBL1	NBL1	-	NBL1
PI4	NBL2	-	-	NBL2
PI5	NBL3	-	-	NBL3
PG8	-	-	-	SDCLK
PC0	-	-	-	SDNWE
PF11	-	-	-	SDNRAS
PG15	-	-	-	SDNCAS
PH2	-	-	-	SDCKE0
PH3	-	-	-	SDNE0
PH6	-	-	-	SDNE1
PH7	-	-	-	SDCKE1
PH5	-	-	-	SDNWE
PC2	-	-	-	SDNE0
PC3	-	-	-	SDCKE0
PB5	-	-	-	SDCKE1
PB6	-	-	-	SDNE1

Table 12. STM32F722xx and STM32F723xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port A	PA0	-	TIM2_ CH1/ TIM2_ ETR	TIM5_ CH1	TIM8_ ETR	-	-	-	USART2_ CTS	UART4_ TX	-	SAI2_ SD_B	-	-	-	-	EVENT OUT
	PA1	-	TIM2_ CH2	TIM5_ CH2	-	-	-	-	USART2_ RTS	UART4_ RX	QUADSPI_ BK1_IO3	SAI2_ MCLK_B	-	-	-	-	EVENT OUT
	PA2	-	TIM2_ CH3	TIM5_ CH3	TIM9_ CH1	-	-	-	USART2_ TX	SAI2_ SCK_B	-	-	-	-	-	-	EVENT OUT
	PA3	-	TIM2_ CH4	TIM5_ CH4	TIM9_ CH2	-	-	-	USART2_ RX	-	-	OTG_HS_ ULPI_D0	-	-	-	-	EVENT OUT
	PA4	-	-	-	-	-	SPI1_ NSS/ I2S1_WS	SPI3_ NSS/ I2S3_WS	USART2_ CK	-	-	-	-	OTG_ HS_ SOF	-	-	EVENT OUT
	PA5	-	TIM2_ CH1/ TIM2_ ETR	-	TIM8_ CH1N	-	SPI1_ SCK/ I2S1_CK	-	-	-	-	OTG_HS_ ULPI_CK	-	-	-	-	EVENT OUT
	PA6	-	TIM1_ BKIN	TIM3_ CH1	TIM8_ BKIN	-	SPI1_ MISO	-	-	-	TIM13_ CH1	-	-	-	-	-	EVENT OUT
	PA7	-	TIM1_ CH1N	TIM3_ CH2	TIM8_ CH1N	-	SPI1_ MOSI/ I2S1_SD	-	-	-	TIM14_ CH1	-	-	FMC_ SDNWE	-	-	EVENT OUT
	PA8	MCO1	TIM1_ CH1	-	TIM8_ BKIN2	I2C3_ SCL	-	-	USART1_ CK	-	-	OTG_FS_ SOF	-	-	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMMC2/ ETH	UART7/ FMC/ SDMMC1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port A	PA9	-	TIM1_ CH2	-	-	I2C3_ SMBA	SPI2_ SCK/ I2S2_CK	-	USART1_ TX	-	-	-	-	-	-	-	EVENT OUT
	PA10	-	TIM1_ CH3	-	-	-	-	-	USART1_ RX	-	-	OTG_ FS_ID	-	-	-	-	EVENT OUT
	PA11	-	TIM1_ CH4	-	-	-	-	-	USART1_ CTS	-	CAN1_RX	OTG_ FS_DM	-	-	-	-	EVENT OUT
	PA12	-	TIM1_ ETR	-	-	-	-	-	USART1_ RTS	SAI2_ FS_B	CAN1_TX	OTG_ FS_DP	-	-	-	-	EVENT OUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_ CH1/ TIM2_ ETR	-	-	-	SPI1_ NSS/ I2S1_WS	SPI3_ NSS/ I2S3_WS	-	UART4_ RTS	-	-	-	-	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port B	PB0	-	TIM1_ CH2N	TIM3_ CH3	TIM8_ CH2N	-	-	-	-	UART4_ CTS	-	OTG_HS_ ULPI_D1	-	-	-	-	EVENT OUT
	PB1	-	TIM1_ CH3N	TIM3_ CH4	TIM8_ CH3N	-	-	-	-	-	-	OTG_HS_ ULPI_D2	-	-	-	-	EVENT OUT
	PB2	-	-	-	-	-	-	SAI1_ SD_A	SPI3_ MOSI/ I2S3_SD	-	QUADSPI_ CLK	-	-	-	-	-	EVENT OUT
	PB3	JTDO/ TRAC ESWO	TIM2_ CH2	-	-	-	SPI1_ SCK/ I2S1_CK	SPI3_ SCK/ I2S3_CK	-	-	-	SDMMC2_ D2	-	-	-	-	EVENT OUT
	PB4	NJTR ST	-	TIM3_ CH1	-	-	SPI1_ MISO	SPI3_ MISO	SPI2_ NSS/ I2S2_WS	-	-	SDMMC2_ D3	-	-	-	-	EVENT OUT
	PB5	-	-	TIM3_ CH2	-	I2C1_SM BA	SPI1_ MOSI/ I2S1_SD	SPI3_ MOSI/ I2S3_SD	-	-	-	OTG_HS_ ULPI_D7	-	FMC_S DCKE1	-	-	EVENT OUT
	PB6	-	-	TIM4_ CH1	-	I2C1_ SCL	-	-	USART1_ TX	-	-	QUADSPI_ BK1_ NCS	-	FMC_S DNE1	-	-	EVENT OUT
	PB7	-	-	TIM4_ CH2	-	I2C1_ SDA	-	-	USART1_ RX	-	-	-	-	FMC_ NL	-	-	EVENT OUT
	PB8	-	-	TIM4_ CH3	TIM10_ CH1	I2C1_ SCL	-	-	-	-	CAN1_RX	SDMMC2_ D4	-	SDMMC 1_D4	-	-	EVENT OUT
	PB9	-	-	TIM4_ CH4	TIM11_ CH1	I2C1_ SDA	SPI2_ NSS/ I2S2_WS	-	-	-	CAN1_TX	SDMMC2_ D5	-	SDMMC 1_D5	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port B	PB10	-	TIM2_ CH3	-	-	I2C2_ SCL	SPI2_ SCK/ I2S2_CK	-	USART3_ TX	-	-	OTG_HS_ ULPI_D3	-	-	-	-	EVENT OUT
	PB11	-	TIM2_ CH4	-	-	I2C2_ SDA	-	-	USART3_ RX	-	-	OTG_HS_ ULPI_D4	-	-	-	-	EVENT OUT
	PB12	-	TIM1_ BKIN	-	-	I2C2_ SMBA	SPI2_ NSS/ I2S2_WS	-	USART3_ CK	-	-	OTG_HS_ ULPI_D5	-	OTG_ HS_ID	-	-	EVENT OUT
	PB13	-	TIM1_ CH1N	-	-	-	SPI2_ SCK/ I2S2_CK	-	USART3_ CTS	-	-	OTG_HS_ ULPI_D6	-	-	-	-	EVENT OUT
	PB14	-	TIM1_ CH2N	-	TIM8_ CH2N	-	SPI2_ MISO	-	USART3_ RTS	-	TIM12_ CH1	SDMMC2_ D0	-	OTG_ HS_DM	-	-	EVENT OUT
	PB15	RTC_ REFIN	TIM1_ CH3N	-	TIM8_ CH3N	-	SPI2_ MOSI/ I2S2_SD	-	-	-	TIM12_ CH2	SDMMC2_ D1	-	OTG_* HS_DP	-	-	EVENT OUT
Port C	PC0	-	-	-	-	-	-	-	-	SAI2_ FS_B	OTG_HS_ DBG[0]	OTG_HS_ ULPI_STP	-	FMC_S DNWE	-	-	EVENT OUT
	PC1	TRAC ED0	-	-	-	-	SPI2_ MOSI/ I2S2_SD	SAI1_ SD_A	-	-	OTG_HS_ DBG[1]	-	-	-	-	-	EVENT OUT
	PC2	-	-	-	-	-	SPI2_ MISO	-	-	-	OTG_HS_ DBG[2]	OTG_HS_ ULPI_DIR	-	FMC_ SDNE0	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port C	PC3	-	-	-	-	-	SPI2_ MOSI/ I2S2_SD	-	-	-	OTG_HS_ DBG[3]	OTG_HS_ ULPI_NXT	-	FMC_S DCKE0	-	-	EVENT OUT
	PC4	-	-	-	-	-	I2S1_ MCK	-	-	-	-	-	-	FMC_S DNE0	-	-	EVENT OUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_S DCKE0	-	-	EVENT OUT
	PC6	-	-	TIM3_ CH1	TIM8_ CH1	-	I2S2_ MCK	-	-	USART6 _TX	-	SDMMC2_ D6	-	SDMMC 1_D6	-	-	EVENT OUT
	PC7	-	-	TIM3_ CH2	TIM8_ CH2	-	-	I2S3_MC K	-	USART6 _RX	-	SDMMC2_ D7	-	SDMMC 1_D7	-	-	EVENT OUT
	PC8	TRAC ED1	-	TIM3_ CH3	TIM8_ CH3	-	-	-	UART5_ RTS	USART6 _CK	-	-	-	SDMMC 1_D0	-	-	EVENT OUT
	PC9	MCO2	-	TIM3_ CH4	TIM8_ CH4	I2C3_ SDA	I2S_CKIN	-	UART5_ CTS	-	QUADSPI_ BK1_IO0	-	-	SDMMC 1_D1	-	-	EVENT OUT
	PC10	-	-	-	-	-	-	SPI3_ SCK/ I2S3_CK	USART3_ TX	UART4_ TX	QUADSPI_ BK1_IO1	-	-	SDMMC 1_D2	-	-	EVENT OUT
	PC11	-	-	-	-	-	-	SPI3_ MISO	USART3_ RX	UART4_ RX	QUADSPI_ BK2_NCS	-	-	SDMMC 1_D3	-	-	EVENT OUT
	PC12	TRAC ED3	-	-	-	-	-	SPI3_ MOSI/ I2S3_SD	USART3_ CK	UART5_ TX	-	-	-	SDMMC 1_CK	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port C	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_ D2	-	-	EVENT OUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FMC_ D3	-	-	EVENT OUT
	PD2	TRAC ED2	-	TIM3_ ETR	-	-	-	-	-	UART5_ RX	-	-	-	SDMMC 1_CMD	-	-	EVENT OUT
	PD3	-	-	-	-	-	SPI2_ SCK/ I2S2_CK	-	USART2_ CTS	-	-	-	-	FMC_ CLK	-	-	EVENT OUT
	PD4	-	-	-	-	-	-	-	USART2_ RTS	-	-	-	-	FMC_ NOE	-	-	EVENT OUT
	PD5	-	-	-	-	-	-	-	USART2_ TX	-	-	-	-	FMC_ NWE	-	-	EVENT OUT
	PD6	-	-	-	-	-	SPI3_ MOSI/ I2S3_SD	SAI1_ SD_A	USART2_ RX	-	-	-	SDMM C2_C K	FMC_ NWAIT	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port D	PD7	-	-	-	-	-	-	-	USART2_ CK	-	-	-	SDMM C2_C MD	FMC_ NE1	-	-	EVENT OUT
	PD8	-	-	-	-	-	-	-	USART3_ TX	-	-	-	-	FMC_ D13	-	-	EVENT OUT
	PD9	-	-	-	-	-	-	-	USART3_ RX	-	-	-	-	FMC_ D14	-	-	EVENT OUT
	PD10	-	-	-	-	-	-	-	USART3_ CK	-	-	-	-	FMC_ D15	-	-	EVENT OUT
	PD11	-	-	-	-	-	-	-	USART3_ CTS	-	QUADSPI_ BK1_IO0	SAI2_ SD_A	-	FMC_ A16/ FMC_ CLE	-	-	EVENT OUT
	PD12	-	-	TIM4_ CH1	LPTIM1 _IN1	-	-	-	USART3_ RTS	-	QUADSPI_ BK1_IO1	SAI2_ FS_A	-	FMC_ A17/ FMC_ ALE	-	-	EVENT OUT
	PD13	-	-	TIM4_ CH2	LPTIM1 _OUT	-	-	-	-	-	QUADSPI_ BK1_IO3	SAI2_ SCK_A	-	FMC_ A18	-	-	EVENT OUT
	PD14	-	-	TIM4_ CH3	-	-	-	-	-	UART8_ CTS	-	-	-	FMC_ D0	-	-	EVENT OUT
	PD15	-	-	TIM4_ CH4	-	-	-	-	-	UART8_ RTS	-	-	-	FMC_ D1	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port E	PE0	-	-	TIM4_ ETR	LPTIM1 _ETR	-	-	-	-	UART8_ RX	-	SAI2_ MCLK_A	-	FMC_ NBL0	-	-	EVENT OUT
	PE1	-	-	-	LPTIM1 _IN2	-	-	-	-	UART8_ TX	-	-	-	FMC_ NBL1	-	-	EVENT OUT
	PE2	TRAC ECLK	-	-	-	-	SPI4_ SCK	SAI1_ MCLK_A	-	-	QUADSPI_ BK1_IO2	-	-	FMC_ A23	-	-	EVENT OUT
	PE3	TRAC ED0	-	-	-	-	-	SAI1_ SD_B	-	-	-	-	-	FMC_ A19	-	-	EVENT OUT
	PE4	TRAC ED1	-	-	-	-	SPI4_ NSS	SAI1_ FS_A	-	-	-	-	-	FMC_ A20	-	-	EVENT OUT
	PE5	TRAC ED2	-	-	TIM9_ CH1	-	SPI4_ MISO	SAI1_ SCK_A	-	-	-	-	-	FMC_ A21	-	-	EVENT OUT
	PE6	TRAC ED3	TIM1_ BKIN2	-	TIM9_ CH2	-	SPI4_ MOSI	SAI1_ SD_A	-	-	-	SAI2_ MCLK_B	-	FMC_ A22	-	-	EVENT OUT
	PE7	-	TIM1_ ETR	-	-	-	-	-	-	UART7_ RX	-	QUADSPI_ BK2_IO0	-	FMC_ D4	-	-	EVENT OUT
	PE8	-	TIM1_ CH1N	-	-	-	-	-	-	UART7_ TX	-	QUADSPI_ BK2_IO1	-	FMC_ D5	-	-	EVENT OUT
	PE9	-	TIM1_ CH1	-	-	-	-	-	-	UART7_ RTS	-	QUADSPI_ BK2_IO2	-	FMC_ D6	-	-	EVENT OUT
	PE10	-	TIM1_ CH2N	-	-	-	-	-	-	UART7_ CTS	-	QUADSPI_ BK2_IO3	-	FMC_ D7	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMMC2/ ETH	UART7/ FMC/ SDMMC1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port E	PE11	-	TIM1_ CH2	-	-	-	SPI4_ NSS	-	-	-	-	SAI2_ SD_B	-	FMC_ D8	-	-	EVENT OUT
	PE12	-	TIM1_ CH3N	-	-	-	SPI4_ SCK	-	-	-	-	SAI2_ SCK_B	-	FMC_ D9	-	-	EVENT OUT
	PE13	-	TIM1_ CH3	-	-	-	SPI4_ MISO	-	-	-	-	SAI2_ FS_B	-	FMC_ D10	-	-	EVENT OUT
	PE14	-	TIM1_ CH4	-	-	-	SPI4_ MOSI	-	-	-	-	SAI2_ MCLK_B	-	FMC_ D11	-	-	EVENT OUT
	PE15	-	TIM1_ BKIN	-	-	-	-	-	-	-	-	-	-	FMC_ D12	-	-	EVENT OUT
Port F	PF0	-	-	-	-	I2C2_ SDA	-	-	-	-	-	-	-	FMC_ A0	-	-	EVENT OUT
	PF1	-	-	-	-	I2C2_ SCL	-	-	-	-	-	-	-	FMC_ A1	-	-	EVENT OUT
	PF2	-	-	-	-	I2C2_ SMBA	-	-	-	-	-	-	-	FMC_ A2	-	-	EVENT OUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A3	-	-	EVENT OUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A4	-	-	EVENT OUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A5	-	-	EVENT OUT
	PF6	-	-	-	TIM10_ CH1	-	SPI5_ NSS	SAI1_ SD_B	-	UART7_ RX	QUADSPI_ BK1_IO3	-	-	-	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port F	PF7	-	-	-	TIM11_ CH1	-	SPI5_ SCK	SAI1_ MCLK_B	-	UART7_ TX	QUADSPI_ BK1_IO2	-	-	-	-	-	EVENT OUT
	PF8	-	-	-	-	-	SPI5_ MISO	SAI1_ SCK_B	-	UART7_ RTS	TIM13_ CH1	QUADSPI_ BK1_IO0	-	-	-	-	EVENT OUT
	PF9	-	-	-	-	-	SPI5_ MOSI	SAI1_ FS_B	-	UART7_ CTS	TIM14_ CH1	QUADSPI_ BK1_IO1	-	-	-	-	EVENT OUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF11	-	-	-	-	-	SPI5_ MOSI	-	-	-	-	SAI2_ SD_B	-	FMC_S DNRAS	-	-	EVENT OUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A6	-	-	EVENT OUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A7	-	-	EVENT OUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A8	-	-	EVENT OUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A9	-	-	EVENT OUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A10	-	-	EVENT OUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A11	-	-	EVENT OUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A12	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port G	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A13	-	-	EVENT OUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A14/ FMC_ BA0	-	-	EVENT OUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ A15/ FMC_ BA1	-	-	EVENT OUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PG7	-	-	-	-	-	-	-	-	USART6 _CK	-	-	-	FMC_ INT	-	-	EVENT OUT
	PG8	-	-	-	-	-	-	-	-	USART6 _RTS	-	-	-	FMC_S DCLK	-	-	EVENT OUT
	PG9	-	-	-	-	-	-	-	-	USART6 _RX	QUADSPI_ BK2_IO2	SAI2_ FS_B	SDMM C2_D 0	FMC_ NE2/ FMC_ NCE	-	-	EVENT OUT
	PG10	-	-	-	-	-	-	-	-	-	-	SAI2_ SD_B	SDMM C2_D 1	FMC_ NE3	-	-	EVENT OUT
	PG11	-	-	-	-	-	-	-	-	-	-	SDMMC2_ D2	-	FMC_ INT	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port G	PG12	-	-	-	LPTIM1 _IN1	-	-	-	-	USART6 _RTS	-	-	SDMM C2_ D3	FMC_ NE4	-		EVENT OUT
	PG13	TRAC ED0	-	-	LPTIM1 _OUT	-	-	-	-	USART6 _CTS	-	-	-	FMC_ A24	-	-	EVENT OUT
	PG14	TRAC ED1	-	-	LPTIM1 _ETR	-	-	-	-	USART6 _TX	QUADSPI_ BK2_IO3	-	-	FMC_ A25	-	-	EVENT OUT
	PG15	-	-	-	-	-	-	-	-	USART6 _CTS	-	-	-	FMC_S DNCAS	-	-	EVENT OUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PH2	-	-	-	LPTIM1 _IN2	-	-	-	-	-	QUADSPI_ BK2_IO0	SAI2_ SCK_B	-	FMC_S DCKE0	-	-	EVENT OUT
	PH3	-	-	-	-	-	-	-	-	-	QUADSPI_ BK2_IO1	SAI2_ MCLK_B	-	FMC_ SDNE0	-	-	EVENT OUT
	PH4	-	-	-	-	I2C2_ SCL	-	-	-	-	-	OTG_HS_ ULPI_NXT	-	-	-	-	EVENT OUT
	PH5	-	-	-	-	I2C2_ SDA	SPI5_ NSS	-	-	-	-	-	-	FMC_ SDNWE	-	-	EVENT OUT
	PH6	-	-	-	-	I2C2_ SMBA	SPI5_ SCK	-	-	-	TIM12_ CH1	-	-	FMC_ SDNE1	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMM C2/ ETH	UART7/ FMC/ SDMM C1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port H	PH7	-	-	-	-	I2C3_ SCL	SPI5_ MISO	-	-	-	-	-	-	FMC_S DCKE1	-	-	EVENT OUT
	PH8	-	-	-	-	I2C3_ SDA	-	-	-	-	-	-	-	FMC_ D16	-	-	EVENT OUT
	PH9	-	-	-	-	I2C3_ SMBA	-	-	-	-	TIM12_ CH2	-	-	FMC_ D17	-	-	EVENT OUT
	PH10	-	-	TIM5_ CH1	-	-	-	-	-	-	-	-	-	FMC_ D18	-	-	EVENT OUT
	PH11	-	-	TIM5_ CH2	-	-	-	-	-	-	-	-	-	FMC_ D19	-	-	EVENT OUT
	PH12	-	-	TIM5_ CH3	-	-	-	-	-	-	-	-	-	FMC_ D20	-	-	EVENT OUT
	PH13	-	-	-	TIM8_ CH1N	-	-	-	-	UART4_ TX	CAN1_TX	-	-	FMC_ D21	-	-	EVENT OUT
	PH14	-	-	-	TIM8_ CH2N	-	-	-	-	UART4_ RX	CAN1_RX	-	-	FMC_ D22	-	-	EVENT OUT
	PH15	-	-	-	TIM8_ CH3N	-	-	-	-	-	-	-	-	FMC_ D23	-	-	EVENT OUT
Port I	PI0	-	-	TIM5_ CH4	-	-	SPI2_ NSS/ I2S2_WS	-	-	-	-	-	-	FMC_ D24	-	-	EVENT OUT
	PI1	-	-	-	TIM8_ BKIN2	-	SPI2_ SCK/ I2S2_CK	-	-	-	-	-	-	FMC_ D25	-	-	EVENT OUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/ UART5/ TIM1/2	TIM3/ 4/5	TIM8/9/ 10/11/ LPTIM1/ DFSDM/ CEC	I2C1/ 2/3/4/ USART1/ CEC	SPI1/ I2S1/ SPI2/ I2S2/ SPI3/ I2S3/ SPI4/5/6	SPI2/ I2S2/ SPI3/ I2S3/ SAI1/ I2C4/ UART4/ DFSDM	SPI2/ I2S2/ SPI3/ I2S3/ SPI6/ USART 1/2/3/ UART5/ DFSDM/ SPDIF	SPI6/ SAI2/ USART6/ UART4/ 5/7/8/ OTG1_ FS/ SPDIF	CAN1/2/ TIM12/ 13/14/ QUADSPI/ FMC/ OTG2_HS/ LCD	SAI2/ QUADSPI/ SDMMC2/ DFSDM/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ CAN3/ SDMMC2/ ETH	UART7/ FMC/ SDMMC1/ MDIOS/ OTG2_ FS	DCMI/ LCD/ DSI	LCD	SYS
Port I	PI2	-	-	-	TIM8_ CH4	-	SPI2_ MISO	-	-	-	-	-	-	FMC_ D26	-	-	EVENT OUT
	PI3	-	-	-	TIM8_ ETR	-	SPI2_ MOSI/ I2S2_SD	-	-	-	-	-	-	FMC_ D27	-	-	EVENT OUT
	PI4	-	-	-	TIM8_ BKIN	-	-	-	-	-	-	SAI2_ MCLK_A	-	FMC_ NBL2	-	-	EVENT OUT
	PI5	-	-	-	TIM8_ CH1	-	-	-	-	-	-	SAI2_ SCK_A	-	FMC_ NBL3	-	-	EVENT OUT
	PI6	-	-	-	TIM8_ CH2	-	-	-	-	-	-	SAI2_ SD_A	-	FMC_ D28	-	-	EVENT OUT
	PI7	-	-	-	TIM8_ CH3	-	-	-	-	-	-	SAI2_ FS_A	-	FMC_ D29	-	-	EVENT OUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PI9	-	-	-	-	-	-	-	-	UART4_ RX	CAN1_RX	-	-	FMC_ D30	-	-	EVENT OUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	-	FMC_ D31	-	-	EVENT OUT
	PI11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ ULPI_DIR	-	-	-	-	EVENT OUT

5 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 27*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 28*.

Figure 27. Pin loading conditions

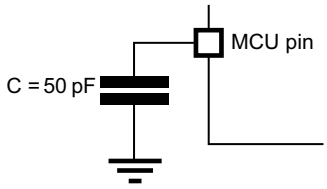
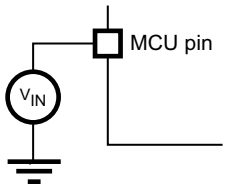
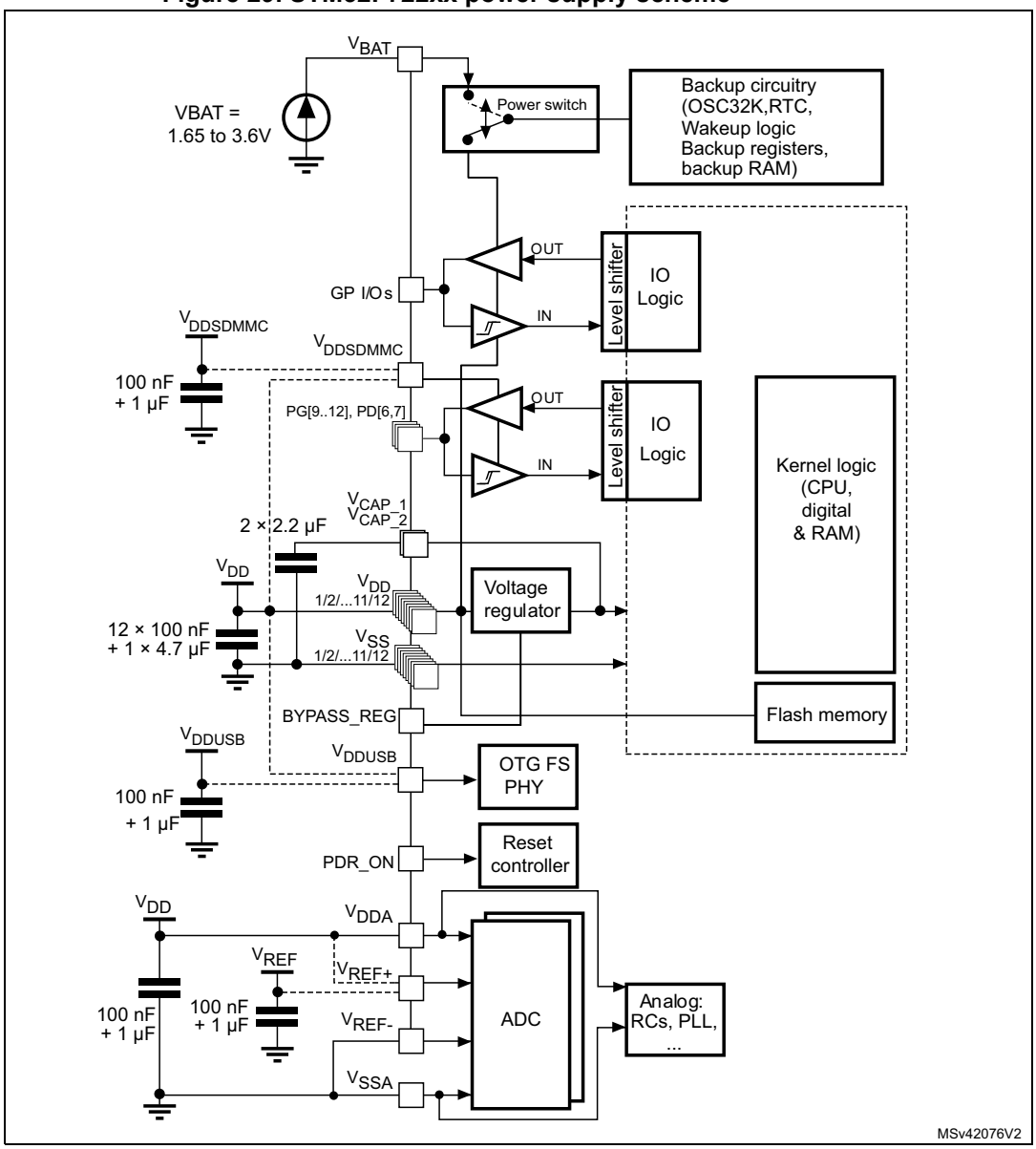


Figure 28. Pin input voltage



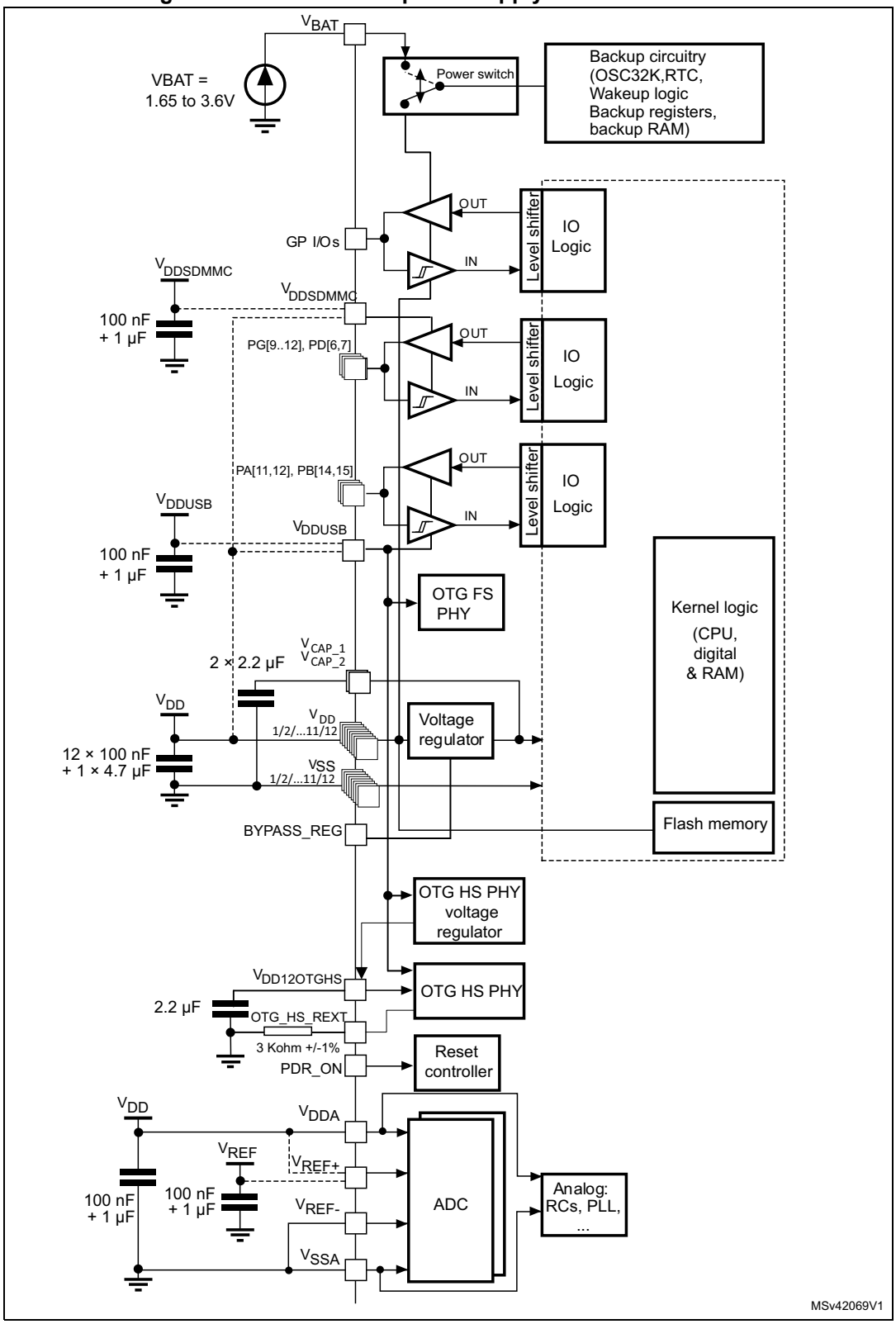
6.1.6 Power supply scheme

Figure 29. STM32F722xx power supply scheme



1. The two 2.2 µF ceramic capacitors must be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
2. The 4.7 µF ceramic capacitor must be connected to one of the VDD pin.
3. $V_{DDA} = V_{DD}$ and $V_{SSA} = V_{SS}$.

Figure 30. STM32F723xx power supply scheme



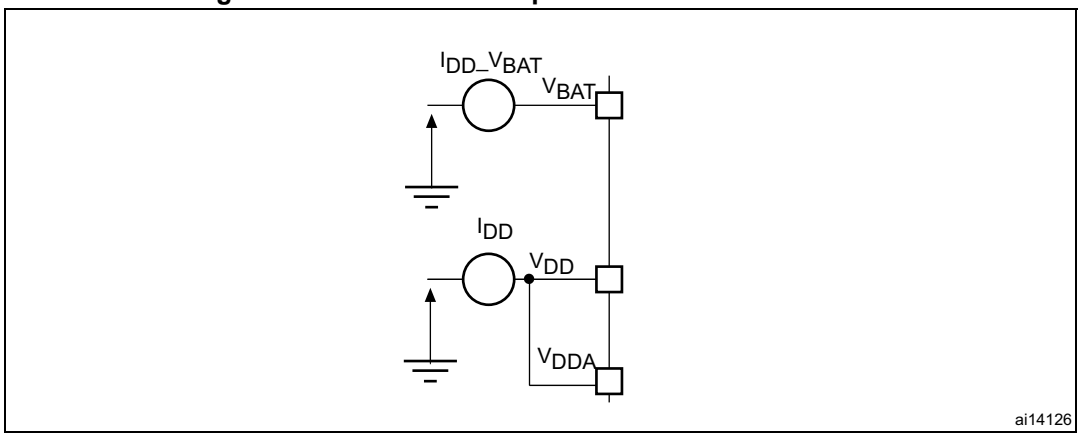
1. In all the packages (except LQFP100), the V_{DDUSB} allows supplying the PHY FS in PA11/PA12 and the PHY HS on PB14/PB15. In the LQFP100, the PHY HS on PB14/PB15 is supplied by $V_{DDPHYHS}$.

2. The two 2.2 µF ceramic capacitors must be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 µF ceramic capacitor must be connected to one of the VDD pin.
4. $V_{DDA} = V_{DD}$ and $V_{SSA} = V_{SS}$.

Caution: Each power supply pair (such as V_{DD}/V_{SS} or V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This may cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 31. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics*, and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD}, V_{BAT}, V_{DDUSB}, $V_{DDPHYHS}$ and $V_{DDSDMMC}$) (1)	− 0.3	4.0	V
V_{IN}	Input voltage on FT pins(2)	V_{SS} − 0.3	V_{DD}+4.0	
	Input voltage on TTa pins	V_{SS} − 0.3	4.0	
	Input voltage on any other pin	V_{SS} − 0.3	4.0	
	Input voltage on BOOT pin	V_{SS}	9.0	

Table 13. Voltage characteristics (continued)

Symbol	Ratings	Min	Max	Unit
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins(3)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.18: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}, $V_{DDSDMMC}$, $V_{DDPHYHS}$, V_{DDUSB}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 14* for the values of the maximum allowed injected current.
3. Include VREF- pin.

Table 14. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	300	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	− 300	
ΣI_{VDDUSB}	Total current into V_{DDUSB} power line (source)	25	
$\Sigma I_{VDDSDMMC}$	Total current into $V_{DDSDMMC}$ power line (source)	60	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
$I_{VDDSDMMC}$	Maximum current into $V_{DDSDMMC}$ power line (source): PG[12:9], PD[7:6]	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	− 100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/Os and control pin	− 25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins (2)	120	
	Total output current sunk by sum of all USB I/Os	25	
	Total output current sourced by sum of all I/Os and control pins(2)	− 120	
$I_{INJ(PIN)}$	Injected current on FT, FTf, RST and B pins (3)	− 5/+0	
	Injected current on TTa pins(4)	±5	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 13: Voltage characteristics* for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	− 65 to +150	°C
T_J	Maximum junction temperature	125	

6.3 Operating conditions

6.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions[1]		Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), regulator ON, over-drive OFF		0	-	144	MHz
		Power scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF	0	-	168	
			Over-drive ON		-	180	
		Power scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF	0	-	180	
			Over-drive ON		-	216[2]	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF		0	-	45	
		Over-drive ON		0	-	54	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF		0	-	90	
		Over-drive ON		0	-	108	

Table 16. General operating conditions (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	1.7[3]	-	3.6	V
V_{DDA}[4][5]	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}[6]	1.7[3]	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11,PA12, PB14 and PB15 pins)	USB not used	1.7	3.3	3.6	
		USB used	3.0	-	3.6	
$V_{DDSPHYHS}$	USB PHY HS supply voltage in the STM32F723 LQFP100 (supply voltage for PB14 and PB15)	USB PHY HS not used	1.7	3.3	3.6	
		USB PHY HS used	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	
$V_{DDSDMMC}$	SDMMC2 supply voltage (supply voltage for PG[12:9] and PD6 pins)	It can be different from V_{DD}	1.7	-	3.6	
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	Power scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 144 MHz HCLK max frequency	1.08	1.14	1.20	V
		Power scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON	1.20	1.26	1.32	
		Power scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 180 MHz HCLK max frequency with over-drive OFF or 216 MHz with over-drive ON	1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins[7]	Max frequency 144 MHz	1.10	1.14	1.20	
		Max frequency 168MHz	1.20	1.26	1.32	
		Max frequency 180 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST and FT pins[8]	2 V ≤V_{DD} ≤3.6 V	− 0.3	-	5.5	
		V_{DD} ≤2 V	− 0.3	-	5.2	
	Input voltage on TTa pins	-	− 0.3	-	V_{DDA}+ 0.3	
	Input voltage on BOOT pin	-	0	-	9	

Table 16. General operating conditions (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7[9]	LQFP64	-	-	881	mW
		LQFP100	-	-	1117	
		WLCSP100	-	-	558	
		LQFP144	-	-	1587	
		LQFP176	-	-	1869	
		UFBGA144	-	-	476	
		UFBGA176	-	-	485	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	− 40	-	85	°C
		Low power dissipation[10]	− 40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	− 40	-	105	°C
		Low power dissipation[10]	− 40	-	125	
T_J	Junction temperature range	6 suffix version	− 40	-	105	°C
		7 suffix version	− 40	-	125	

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2. 216 MHz maximum frequency for 6 suffix version (200 MHz maximum frequency for 7 suffix version).
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
4. When the ADC is used, refer to *Table 67: ADC characteristics*.
5. If VREF+ pin is present, it must respect the following condition: $V_{DDA} - V_{REF+} < 1.2$ V.
6. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
7. The over-drive mode is not supported when the internal regulator is OFF.
8. To sustain a voltage higher than V_{DD} + 0.3, the internal pull-up and pull-Down resistors must be disabled.
9. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
10. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 17. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum HCLK frequency vs Flash memory wait states (1)(2)	I/O operation	Possible Flash memory operations
V_{DD} =1.7 to 2.1 V[3]	Conversion time up to 1.2 Msps	20 MHz	180 MHz with 8 wait states and over-drive OFF	No I/O compensation	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	22 MHz	216 MHz with 9 wait states and over-drive ON	No I/O compensation	16-bit erase and program operations

Table 17. Limitations depending on the operating power supply range (continued)

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum HCLK frequency vs Flash memory wait states (1)(2)	I/O operation	Possible Flash memory operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	216 MHz with 8 wait states and over-drive ON	I/O compensation works	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(4)	Conversion time up to 2.4 Msps	30 MHz	216 MHz with 7 wait states and over-drive ON	I/O compensation works	32-bit erase and program operations

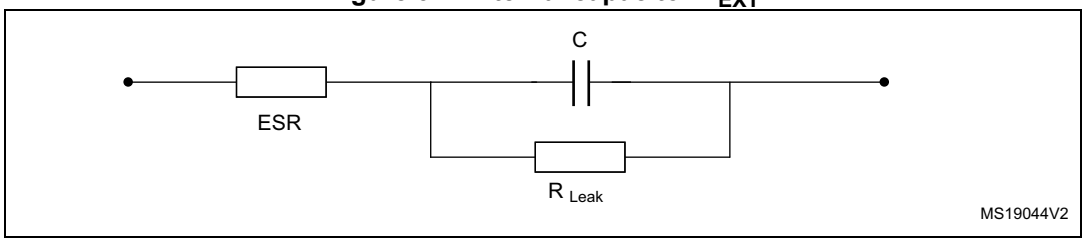
1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator or L1-cache is used to achieve a performance equivalent to 0-wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
4. The voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins are degraded between 2.7 and 3 V.

6.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP1/VCAP2 pins. C_{EXT} is specified in *Table 18*.

Note: The VCAP2 pin is not available on the LQFP64 package.

Figure 32. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 18. VCAP1/VCAP2 operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

Table 19. VCAP1 operating conditions in the LQFP64 package(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	4.7 µF
ESR	ESR of external capacitor	between 0.1 Ω and 0.2 Ω

1. When bypassing the voltage regulator, the 4.7 µF V_{CAP} capacitor is not required and should be replaced by two 100 nF decoupling capacitors.

6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 20. Operating conditions at power-up/power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up/power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 21. Operating conditions at power-up/power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reaches below 1.08 V.

6.3.5 Reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 22. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.75	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}$(1)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(1)(2)	POR reset temporization	-	0.5	1.5	3.0	ms

Table 22. Reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	250	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

6.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in *Table 23*. They are sbject to general operating conditions for T_A.

Table 23. Over-drive switching characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	µs
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed by design.

6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 31: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see *Table 17: Limitations depending on the operating power supply range*).
- When the regulator is ON, the voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 144$ MHz
  - Scale 2 for 144 MHz < $f_{HCLK} \leq 168$ MHz
  - Scale 1 for 168 MHz < $f_{HCLK} \leq 216$ MHz. The over-drive is only ON at 216 MHz.
- When the regulator is OFF, the V12 is provided externally as described in *Table 16: General operating conditions*:
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range and for T_A= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range and a maximum ambient temperature (T_A) unless otherwise specified.
- For the voltage range 1.7 V ≤ V_{DD} ≤ 3.6 V, the maximum frequency is 180 MHz.

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	All peripherals enabled(2)(3)	216	156	170(4)	180(4)	200	mA
			200	144	154	164.6	183	
			180	127	134(4)	143(4)	158(4)	
			168	113	119	127.4	141	
			144	86	96	112.6	126	
			60	41	44	52.8	65	
			25	22	24	33.5	45	
		All peripherals disabled(3)	216	99	110(4)	119.6(4)	138.5	
			200	92	102	113.1	132	
			180	81	90(4)	96.7(4)	125(4)	
			168	72	78	86.5	100.1	
			144	55	61	77.1	90.8	
			60	24	25	38.5	50.3	
			25	12	13	26.3	38.1	

1. Guaranteed by characterization results.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.
4. Guaranteed by test in production.

Table 25. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	All peripherals enabled(2)(3)	216	155.3	164	175.8	185	mA
			200	144.7	153.6	165.2	176	
			180	127.3	135	143.5	154	
			168	113.1	119.1	127.8	138	
			144	86.9	91.6	99.5	110	
			60	41.2	43.6	53.1	64	
			25	21.7	24	33.6	43.8	
		All peripherals disabled(3)	216	90	106	120.4	130	
			200	84	99	113.8	124	
			180	74	86.6	97.3	107	
			168	66	76	87	97	
			144	51	59	68.2	78	
			60	23	27	38.8	49	
			25	11	13.6	26.4	36.8	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 26. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory or SRAM on AXI (L1-cache disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in Run mode	All peripherals enabled(2)(3)	216	129.3	137.6	162.8	173	mA
			200	122	128	153.2	163.3	
			180	108	117	136.4	146	
			168	99	104.5	122.3	132	
			144	80	84.7	99.3	109.2	
			60	42	45	59.5	70	
			25	23	23.4	37.8	48	
		All peripherals disabled(3)	216	73.3	82.3	107.4	119	
			200	70	77	101.8	113.5	
			180	62	71	90.2	101	
			168	59	63.6	81.4	92.1	
			144	49	53.3	67.9	79	
			60	26	31	45.1	56	
			25	14	16	30.6	41.2	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 27. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory on ITCM interface (ART disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in Run mode	All peripherals enabled(2)(3)	216	138	151	174.7	184	mA
			200	133	141	164.3	174	
			180	110	131	149.2	159	
			168	99	117	134	144	
			144	79	98	111.7	121	
			60	49	53	64	75	
			25	27	30	38.3	48	
		All peripherals disabled(3)	216	82	96	119.5	131	
			200	81	89	113.1	124	
			180	65	85	103.1	114	
			168	58	76	93.2	104	
			144	48	67	80.4	91	
			60	33	36	49.7	60	
			25	18	21	31.1	41	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 28. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in Run mode from V_{12} and V_{DD} supplies	All peripherals enabled(2)(3)	180	112	1.4	120	2	132.7	2	142	2	mA
			168	110	1.4	106.4	2	118.7	2	130	2	
			144	78	1.3	82.5	2	93.6	2	103	2	
			60	37	1.1	37.6	2	49.3	2	60	2	
			25	19	1.1	18.5	2	30.4	2	40	2	
		All peripherals disabled(3)	180	74	1.4	78	2	89.3	2	99	2	
			168	64	1.4	68	2	80.1	2	90	2	
			144	51	1.3	54	2	63.5	2	74	2	
			60	22	1.1	24	2	35.2	2	45	2	
			25	10	1.2	12	2	23.2	2	35	2	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 29. Typical and maximum current consumption in Sleep mode, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in Sleep mode	All peripherals enabled(2)	216	82	96(3)	109.3(3)	128.3	mA
			200	77	84	103.4	122.6	
			180	67	72(3)	88.3(3)	120(3)	
			168	60	64	78.9	92.7	
			144	46	49	61.8	73.6	
			60	24	26	37.2	49	
			25	14	16	27	38.8	
		All peripherals disabled	216	24	28(3)	42.9(3)	62.2	
			200	22	26	41.9	61.2	
			180	19	21(3)	33.2(3)	48(3)	
			168	17	19	30.1	43.9	
			144	13	15	24.6	36.3	
			60	7	9	20.5	32.3	
			25	5	7	18.8	30.6	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Guaranteed by test in production.

Table 30. Typical and maximum current consumption in Sleep mode, regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in Run mode from V_{12} and V_{DD} supplies	All peripherals enabled(2)	180	62	1.3	67.5	2	84.4	2	95	2	mA
			168	55	1.3	59.8	2	75.4	2	86	2	
			144	43	1.3	46.3	2	59.6	2	70	2	
			60	22	1	24	2	35.8	2	46	2	
			25	13	1	15	2	25.8	2	36	2	
		All peripherals disabled	180	17	1.3	19	2	31.4	2	42	2	
			168	15	1.3	17	2	28.4	2	40	2	
			144	12	1.2	14	2	23.2	2	33	2	
			60	5	1	6	2	19.3	2	29	2	
			25	3	1	4	2	17.6	2	28	2	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

Table 31. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)			Unit
				V_{DD} = 3.6 V			
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
$I_{DD_STOP_NM}$ (normal mode)	Supply current in Stop mode, main regulator in Run mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.45	2	12	22	mA
		Flash memory in Deep power down mode, all oscillators OFF	0.4	2	12	22	
	Supply current in Stop mode, main regulator in low-power mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.32	1.5	10	18	
		Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.27	1.5	10	18	
$I_{DD_STOP_UDM}$ (under-drive mode)	Supply current in Stop mode, main regulator in low-voltage and under-drive modes	Regulator in Run mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.15	0.8	5	7	
		Regulator in Low-power mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.1	0.7	4	7	

1. Data based on characterization, tested in production.

Table 32. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			T_A = 25 °C			T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.7 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.3 V			
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM OFF, RTC and LSE OFF	1.09	1.13	1.4	4	27	55	µA
		Backup SRAM ON, RTC and LSE OFF	1.85	1.88	2.17	5	30	60	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	1.65	1.86	2.43	7	47	95.5	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	1.67	1.88	2.46	7	47.5	97	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	1.8	2.01	2.61	7.5	50.5	102.5	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	1.92	2.13	2.73	8	53	107	
		Backup SRAM ON, RTC ON and LSE in low drive mode	2.39	2.6	3.23	9	62	127	
		Backup SRAM ON, RTC ON and LSE in medium low drive mode	2.41	2.64	3.25	9	63	128	
		Backup SRAM ON, RTC ON and LSE in medium high drive mode	2.67	2.89	2.53	10	68	139	
		Backup SRAM ON, RTC ON and LSE in high drive mode	2.68	2.9	3.51	10	68	138	

1. PDR is OFF for V_{DD}=1.7V. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA.
2. Guaranteed by characterization results.

Table 33. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions[1]	Typ			Max[2]		Unit
			T_A =25 °C			T_A =85 °C	T_A =105 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT}= 3.3 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Supply current in V_{BAT} mode	Backup SRAM OFF, RTC and LSE OFF	0.035	0.037	0.043	4	10	µA
		Backup SRAM ON, RTC and LSE OFF	0.69	0.71	0.73	9	20	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	0.57	0.74	1.05	98	244	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	0.59	0.76	1.08	101	251	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	0.69	0.86	1.19	111	277	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	0.8	0.98	1.31	122	305	
		Backup SRAM ON, RTC ON and LSE in low drive mode	1.22	1.41	1.74	162	405	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	1.25	1.43	1.78	166	414	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	1.46	1.65	2.01	187	468	
		Backup SRAM ON, RTC ON and LSE in High drive mode	1.46	1.65	2.01	187	468	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization results.

Figure 33. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in low drive mode)

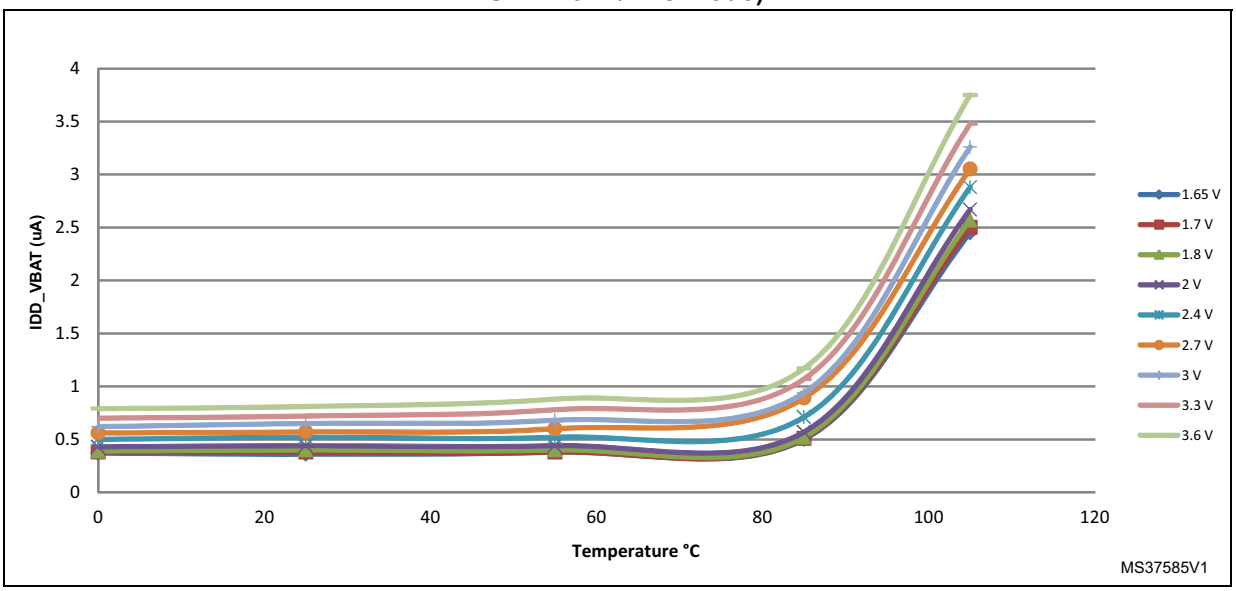


Figure 34. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in medium low drive mode)

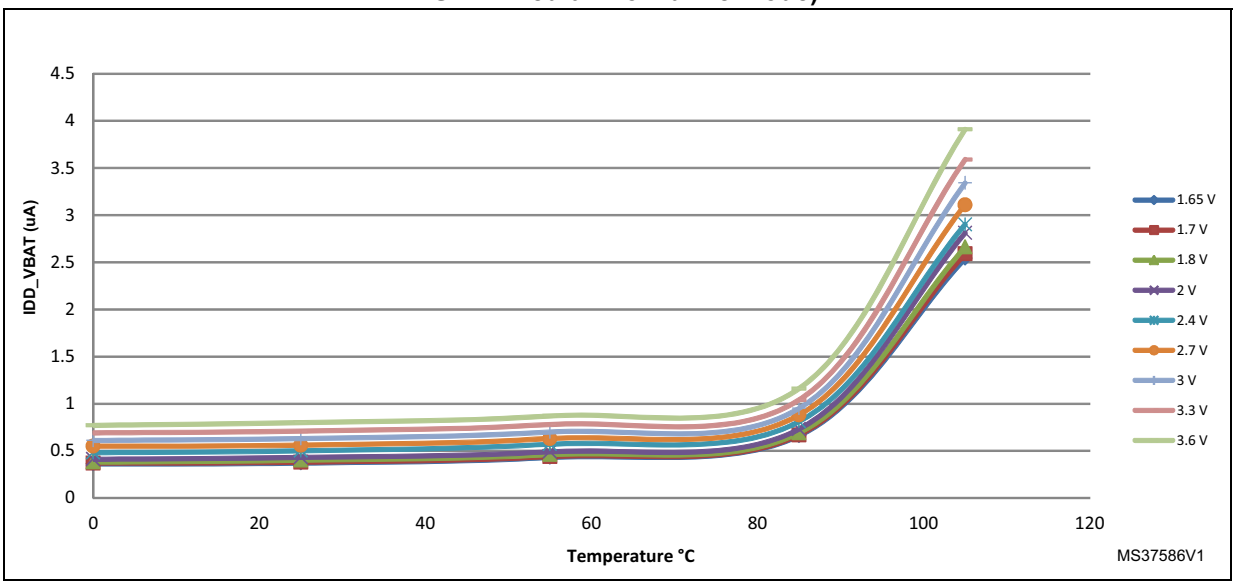


Figure 35. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in medium high drive mode)

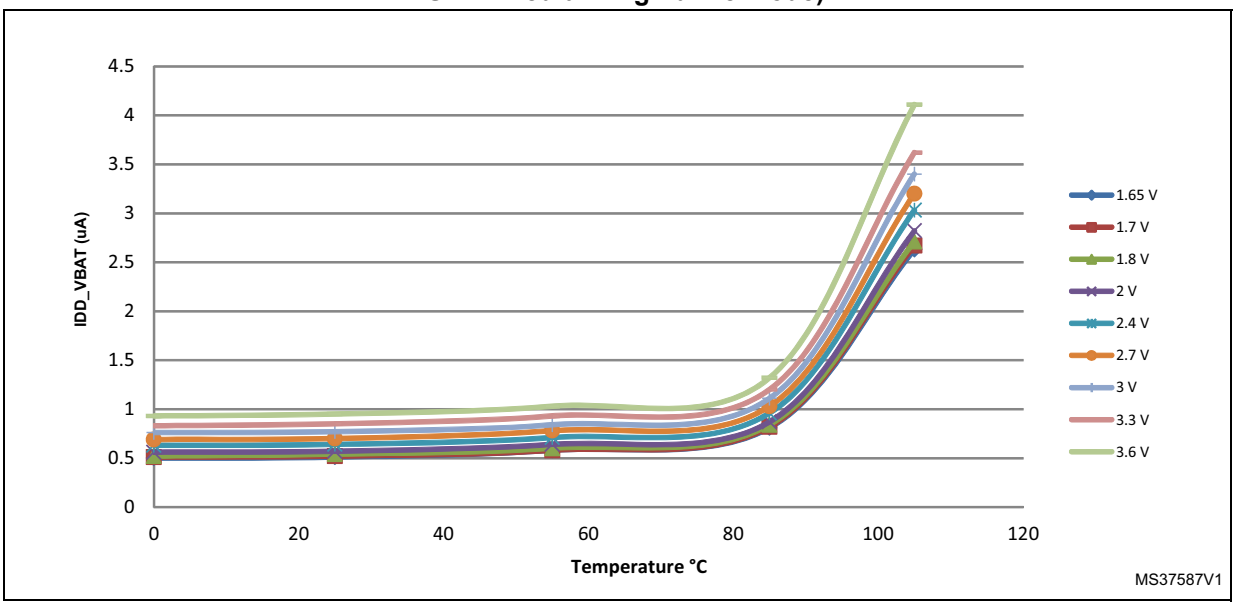


Figure 36. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in high drive mode)

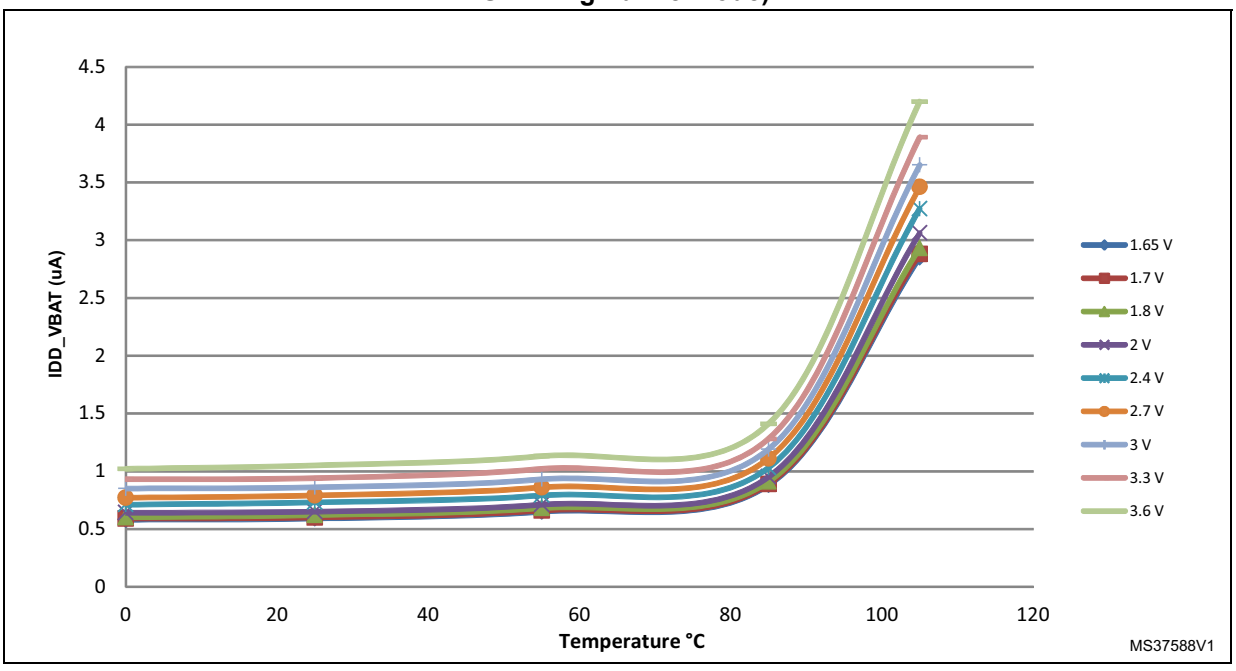
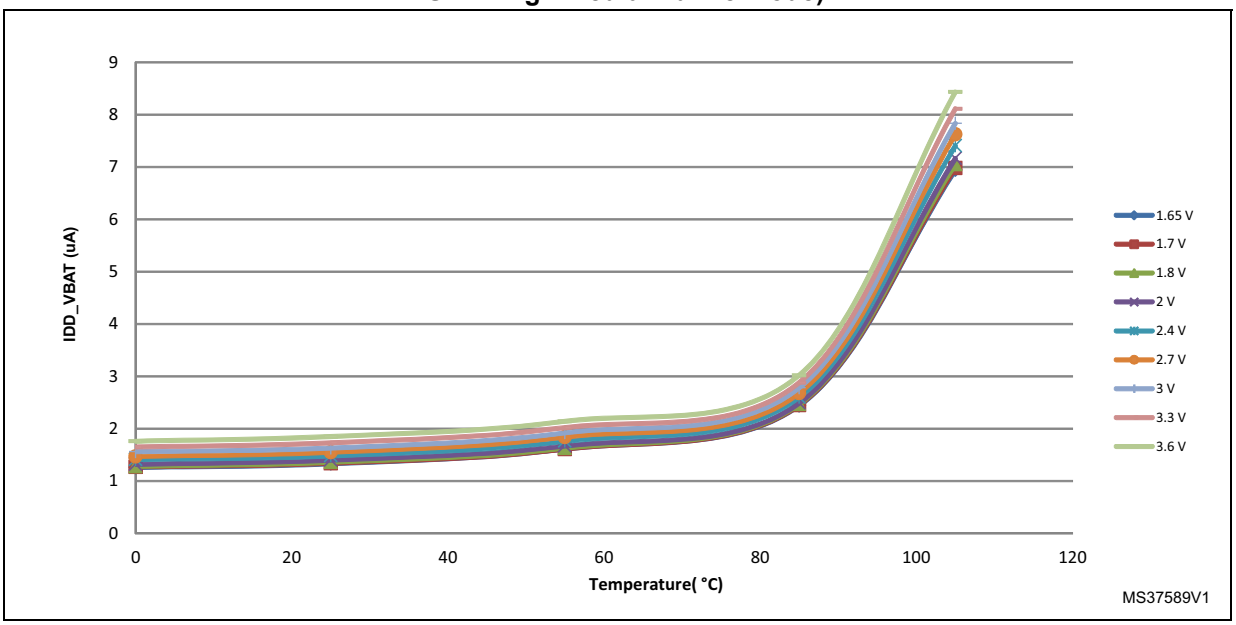


Figure 37. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in high medium drive mode)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as input with pull-up or pull-down generate current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 61: I/O static characteristics*.

For the output pins, any internal or external pull-up or pull-down and external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which must be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 35: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O

pin circuitry and to charge/discharge the capacitive load internal and external connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

Where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load.

V_{DD} is the MCU supply voltage.

f_{SW} is the I/O switching frequency.

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 34. Switching output I/O current consumption(1)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ V_{DD} = 3.3 V	Typ V_{DD} = 1.8 V	Unit
I_{DDIO}	I/O switching current	C_{EXT} = 0 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.1	0.1	mA
			8	0.4	0.2	
			25	1.1	0.7	
			50	2.4	1.3	
			60	3.1	1.6	
			84	4.3	2.4	
			90	4.9	2.6	
			100	5.4	2.8	
			108	5.6	-	
		C_{EXT} = 10 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.2	0.1	
			8	0.6	0.3	
			25	1.8	1.1	
			50	3.1	2.3	
			60	4.6	3.4	
			84	9.7	3.6	
			90	10.12	5.2	
			100	14.92	5.4	
			108	18.11	-	

Table 34. Switching output I/O current consumption(1) (continued)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ V_{DD} = 3.3 V	Typ V_{DD} = 1.8 V	Unit
I_{DDIO}	I/O switching current	C_{EXT} = 22 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.1	mA
			8	1.0	0.5	
			25	3.5	1.6	
			50	5.9	4.2	
			60	10.0	4.4	
			84	19.12	5.8	
			90	19.6	-	
		C_{EXT} = 33 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.2	
			8	1.3	0.7	
			25	3.5	2.3	
			50	10.26	5.19	
			60	16.53	-	

1. CINT + $C_{S,}$ PCB board capacitance including the pad pin is estimated to15 pF.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled
- The ART/L1-cache is ON.
- Scale 1 mode selected, internal digital voltage V_{12} = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - f_{HCLK} = 216 MHz (Scale 1 + over-drive ON), f_{HCLK} = 168 MHz (Scale 2), f_{HCLK} = 144 MHz (Scale 3)
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 35. Peripheral current consumption

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1 (up to 216 MHz)	GPIOA	3.6	3.4	2.9	µA/MHz
	GPIOB	3.7	3.6	3.1	
	GPIOC	3.7	3.4	3.0	
	GPIOD	3.7	3.6	3.0	
	GPIOE	3.6	3.4	2.9	
	GPIOF	3.5	3.4	2.9	
	GPIOG	3.5	3.3	2.8	
	GPIOH	3.5	3.4	2.9	
	GPIOI	3.5	3.3	2.9	
	CRC	1.2	1.1	0.9	
	BKPSRAM	0.8	0.7	0.6	
	DMA1	3.07 x N + 8.7	2.98 x N + 8.4	2.52 x N + 7.02	
	DMA2	3.01 x N + 7.98	2.95 x N + 7.95	2.48 x N + 6.69	
	OTG_HS+ULPI	54.4	53.2	44.6	
AHB2 (up to 216 MHz)	RNG	1.9	1.8	1.6	µA/MHz
	USB_OTG_FS	28.7	27.9	23.5	
AHB3 (up to 216 MHz)	FMC	16.2	15.8	13.3	µA/MHz
	QSPI	16.9	16.3	13.8	
Bus matrix(2)		15.8	12.8	8.5	µA/MHz

Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)[1]			Unit
		Scale 1	Scale 2	Scale 3	
APB1 (up to 54 MHz)	TIM2	19.3	18.2	15.6	µA/MHz
	TIM3	15	14	12.2	
	TIM4	15.7	15.1	12.8	
	TIM5	18	16.9	14.4	
	TIM6	3.7	3.1	2.8	
	TIM7	3.5	2.9	2.5	
	TIM12	8.1	7.8	6.4	
	TIM13	6.1	5.1	4.7	
	TIM14	6.3	5.6	4.7	
	LPTIM1	9.4	9.8	8.3	
	WWDG	2.4	1.3	1.4	
	SPI2/I2S2[3]	6.7	6	5.3	
	SPI3/I2S3[3]	4.8	3.8	3.3	
	USART2	13.3	12	10.6	
	USART3	12.8	12	10.3	
	UART4	11.7	10.7	9.2	
	UART5	11.7	10.2	8.9	
	I2C1	10.6	9.6	8.3	
	I2C2	10.6	9.6	8.3	
	I2C3	10.7	9.8	8.3	
	CAN1	8.9	8	6.9	
	PWR	11.3	11.3	8.9	
	DAC[4]	6.1	5.1	4.4	
	UART7	13.3	12	10.3	
	UART8	12.6	11.6	9.7	

Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 108 MHz)	TIM1	24.9	23.8	20	µA/MHz
	TIM8	24.5	23.7	20	
	USART1	12.4	11.6	10	
	USART6	12.3	11.7	10	
	ADC1(5)	6.3	5.8	4.9	
	ADC2(5)	6.3	5.6	4.9	
	ADC3(5)	6.4	5.8	5	
	SDMMC1	9.1	8.3	7.1	
	SDMMC2	7	7.2	6	
	SPI1/I2S1(3)	3.2	3.2	2.6	
	SPI4	2.9	2.9	2.2	
	SYSCFG	1	1	0.7	
	TIM9	9.9	9.1	7.8	
	TIM10	7	6.4	5.6	
	TIM11	7.2	6.8	5.7	
	SPI5	4.8	4.1	3.6	
	SAI1	5.6	4.9	4.2	
	SAI2	5.4	4.7	4	
	USB PHY HS Controller	8.3	7.9	6.7	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.75 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

USB OTG HS and USB OTG HS PHY current consumption (on STM32F723xx devices)

The MCU is placed under the following conditions:

- STM32 MCU is enumerated as a HID device.
- f_{HCLK} = 216 MHz (Scale 1 + over-drive ON), f_{HCLK} = 168 MHz (Scale 2), f_{HCLK} = 144 MHz (Scale 3)
  The given value is calculated by measuring the difference of current consumption in case:
  - USB is configured but no transfer is done.
  - USB is configured and there is a transmission on going.
- Ambient operating temperature is 25 °C, V_{DD} = V_{DDUSB} = 3.3 V.

Table 36. USB OTG HS and USB OTG PHY HS current consumption

-	I_{DD} (Typ)			Unit
	Scale 1	Scale 2	Scale 3	
USB OTG HS and USB OTG HS PHY current consumption	50.16	44.92	38.98	mA

6.3.8 Wakeup time from low-power modes

The wakeup times given in *Table 37* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.3 V.

Table 37. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep mode	-	13	13	CPU clock cycles
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	14	14.9	µs
		Main regulator is ON and Flash memory in Deep power down mode	104.1	107.6	
		Low power regulator is ON	21.4	24.2	
		Low power regulator is ON and Flash memory in Deep power down mode	111.5	116.5	

Table 37. Low-power mode wakeup timings (continued)

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	107.4	113.2	µs
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	112.7	120	
$t_{WUSTDBY}$(2)	Wakeup from Standby mode	Exit Standby mode on rising edge	308	313	µs
		Exit Standby mode on falling edge	307	313	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 61: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 38*.

The characteristics given in *Table 38* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 16*.

Table 38. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)	-	1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 61: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 39*.

The characteristics given in *Table 39* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 16*.

Table 39. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 38. High-speed external clock source AC timing diagram

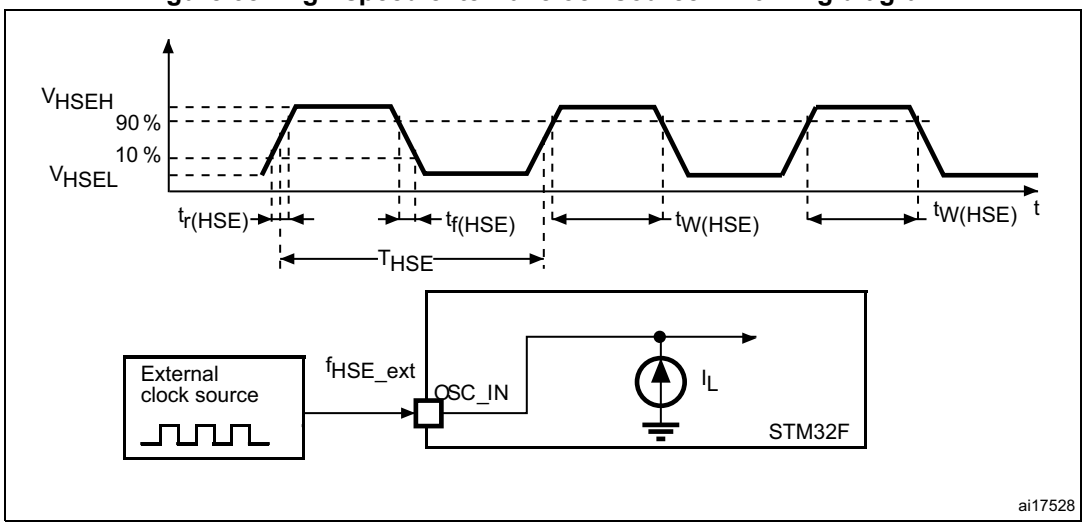
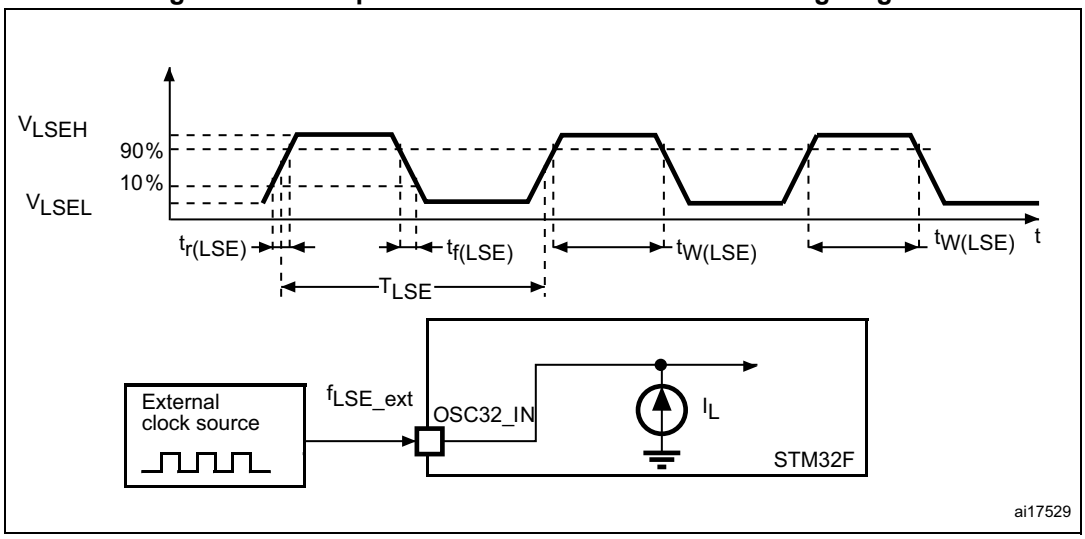


Figure 39. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. HSE 4-26 MHz oscillator characteristics(1)

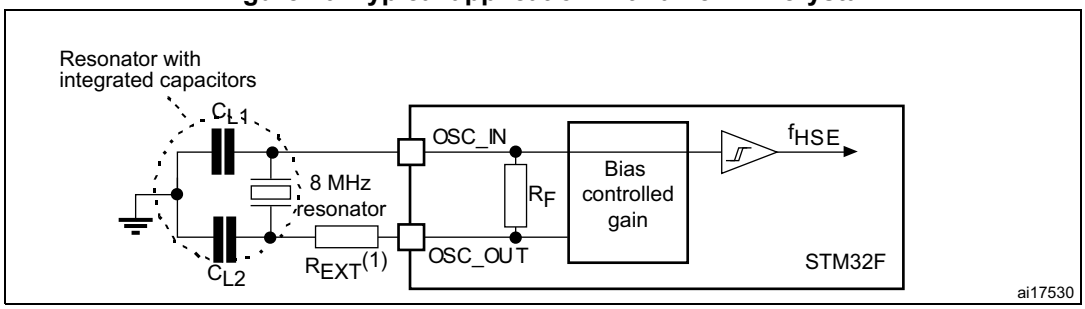
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	26	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	V_{DD}=3.3 V, ESR= 30 Ω, C_L=5 pF@25 MHz	-	450	-	µA
		V_{DD}=3.3 V, ESR= 30 Ω, C_L=10 pF@25 MHz	-	530	-	
ACC_{HSE}(2)	HSE accuracy	-	− 500	-	500	ppm
G_m_crit_max	Maximum critical crystal g_m	Startup	-	-	1	mA/V
$t_{SU(HSE}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is based on characterization results. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 40*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 40. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 Low drive capability	-	250	-	nA
		LSEDRV[1:0]=10 Medium low drive capability	-	300	-	
		LSEDRV[1:0]=01 Medium high drive capability	-	370	-	
		LSEDRV[1:0]=11 High drive capability	-	480	-	

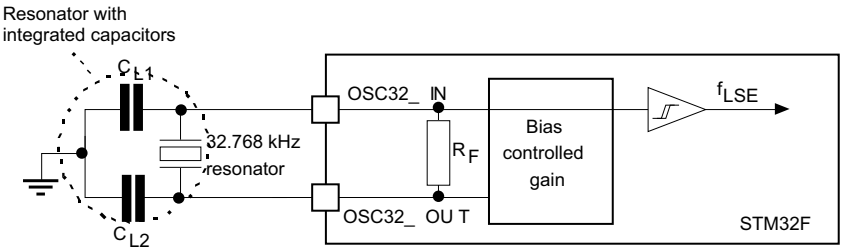
Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_m_crit_max	Maximum critical crystal g_m	LSEDRV[1:0]=00 Low drive capability	-	-	0.48	µA/V
		LSEDRV[1:0]=10 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0]=01 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0]=11 High drive capability	-	-	2.7	
t_{SU}(2)	start-up time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Guaranteed by characterization results. t_{SU} is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST Microelectronics website www.st.com.

Figure 41. Typical application with a 32.768 kHz crystal



6.3.10 Internal clock source characteristics

The parameters given in *Table 42* and *Table 43* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics (1)

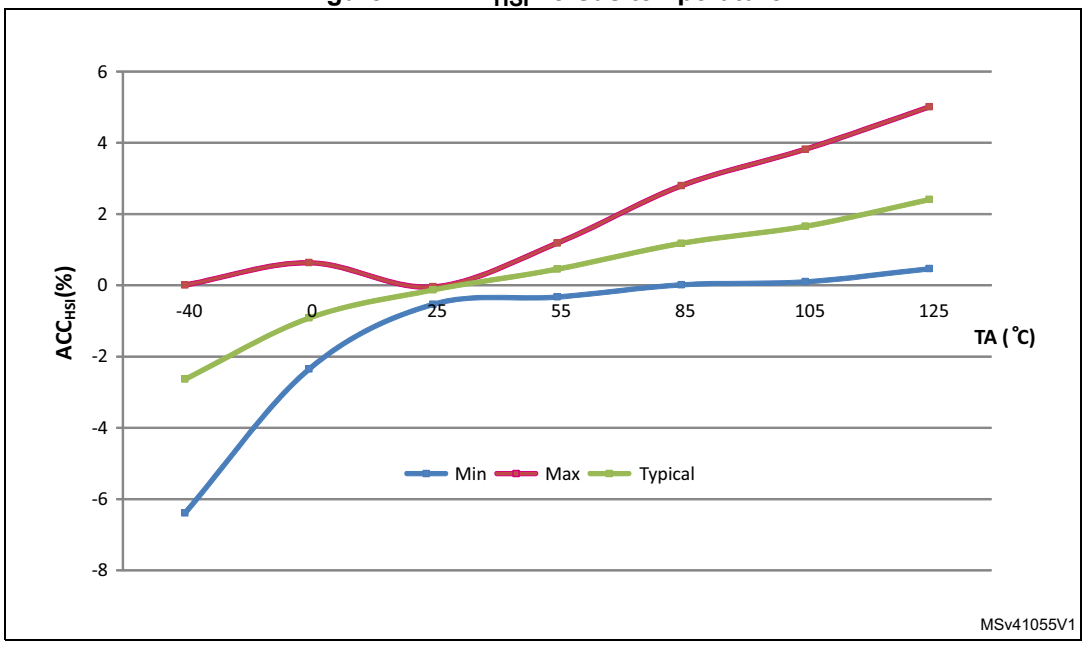
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	− 8	-	4.5	%
		T_A = –10 to 85 °C(3)	− 4	-	4	%
		T_A = 25 °C(4)	− 1	-	1	%

Table 42. HSI oscillator characteristics (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, PLL OFF, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 42. ACC_{HSI} versus temperature



1. Guaranteed by characterization results.

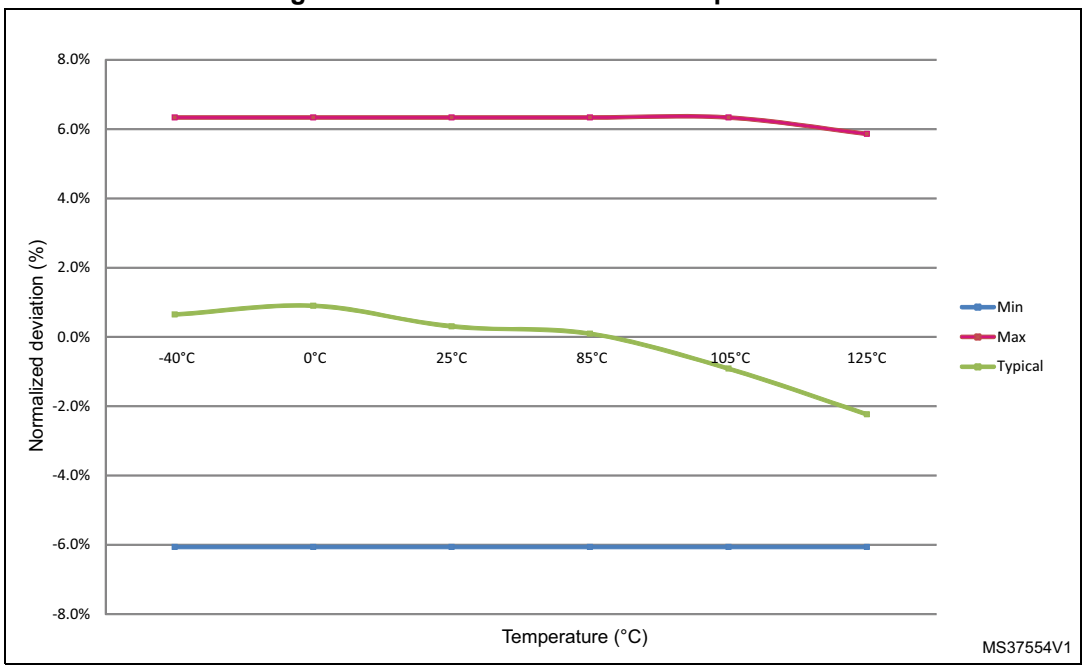
Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Figure 43. LSI deviation versus temperature



6.3.11 PLL characteristics

The parameters given in *Table 44* and *Table 45* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 44. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	216	
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	
f_{VCO_OUT}	PLL VCO output	-	100	-	432	
t_{LOCK}	PLL lock time	VCO freq = 100 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Table 44. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Cycle-to-cycle jitter	System clock 216 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

Table 45. PLLI2S characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)	-		0.95(2)	1	2.10	MHz
$f_{PLLI2SQ_OUT}$	PLLI2S multiplier output clock for SAI	-		-	-	216	
$f_{PLLI2SR_OUT}$	PLLI2S multiplier output clock for I2S	-		-	-	216	
f_{VCO_OUT}	PLLI2S VCO output	-		100	-	432	
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 kHz on 1000 samples		-	400	-	ps

Table 45. PLLI2S characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 46. PLLISAI characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLSAI_IN}	PLLSAI input clock(1)	-		0.95(2)	1	2.10	MHz
$f_{PLLSAIP_OUT}$	PLLSAI multiplier output clock for 48 MHz	-		-	48	75	
$f_{PLLSAIQ_OUT}$	PLLSAI multiplier output clock for SAI	-		-	-	216	
f_{VCO_OUT}	PLLSAI VCO output	-		100	-	432	
t_{LOCK}	PLLSAI lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	FS clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLSAI)}$(4)	PLLSAI power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLSAI)}$(4)	PLLSAI power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

6.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature is used to reduce electromagnetic interferences (see *Table 57: EMI characteristics for fHSE = 25 MHz and fHCLK = 250 MHz*). It is available only on the main PLL.

Table 47. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	kHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15} - 1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 calculates the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(peak)$$

Figure 44 and *Figure 45* show the main PLL output clock waveforms in center spread and down spread modes, where:

- F0 is f_{PLL_OUT} nominal.
- T_{mode} is the modulation period.
- md is the modulation depth.

Figure 44. PLL output clock waveforms in center spread mode

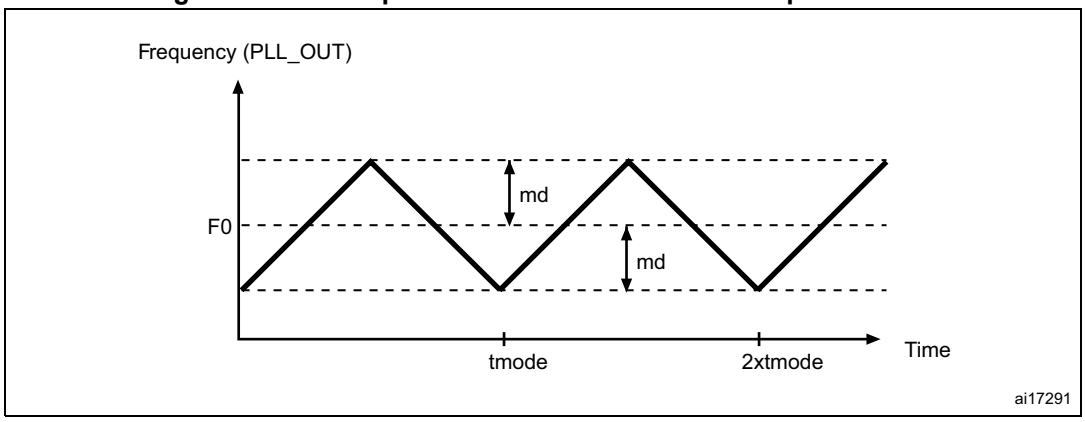
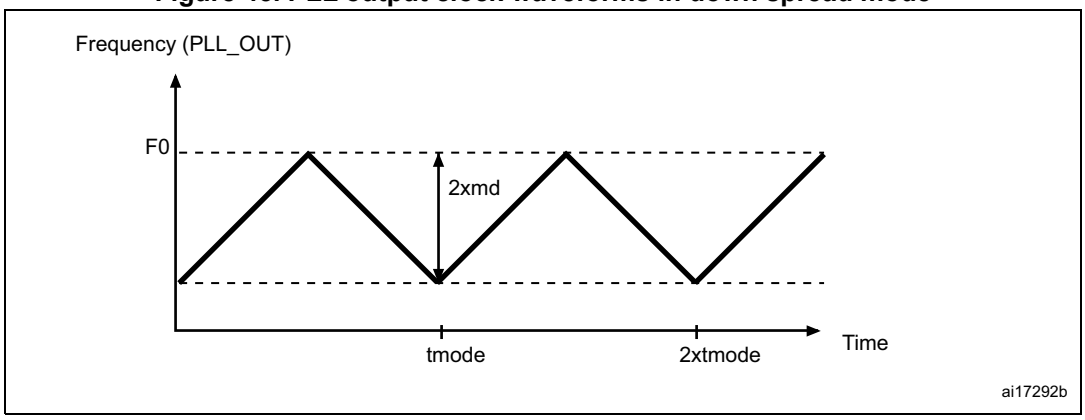


Figure 45. PLL output clock waveforms in down spread mode



6.3.13 USB OTG HS PHY PLLs characteristics (on STM32F723xx devices)

The parameters given in *Table 48* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 48. USB OTG HS PLL1 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL1_IN}	PLL1 input clock	-	12, 12.5, 16, 24, 25			MHz
f_{PLL1_OUT}	PLL1 output clock(2)	-	-	60	-	
f_{VCO_OUT}	PLL1 VCO output	-	600	-	720	
t_{LOCK}	PLL1 lock time(2)	-	-	-	22	µs
$I_{DD(PLL1)}$	PLL1 digital power consumption	-	-	-	1.8	mA
$I_{DDA(PLL1)}$	PLL1 analog power consumption	-	-	-	2.75	

1. Guaranteed by design.
2. Based on test during characterization.

Table 49. USB OTG HS PLL2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL2_IN}	PLL2 input clock	-	-	60	-	MHz
f_{PLL2_OUT}	PLL2 output clock(2)	-	-	480	-	
f_{VCO_OUT}	PLL2 VCO output	-	-	480	-	
t_{LOCK}	PLL2 lock time(2)	-	-	-	91	µs
$I_{DD(PLL2)}$	PLL2 digital power consumption	-	-	-	2.1	mA
$I_{DDA(PLL2)}$	PLL2 analog power consumption	-	-	-	1.5	

1. Guaranteed by design.
2. Based on test during characterization.

6.3.14 USB OTG HS PHY regulator characteristics

The parameters given in *Table 50* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 50. USB OTG HS PHY regulator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD12OTGHS}$	1.2 V internal voltage on $V_{DD12OTGHS}$	-	1.18	1.2	1.24	V
CEXT	External capacitor on $V_{DD12OTGHS}$	-	1.1	2.2	3.3	µF
$I_{DDPHYHSREG}$	Regulator power consumption	-	100	120	125	µA

1. Based on test during characterization.

6.3.15 USB HS PHY external resistor characteristics (on STM32F723xx devices)

Table 51. USB HS PHY external resistor characteristics (on STM32F723xx devices)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
REXT	External calibration resistor connected (to GND) from OTG_HS_REXT	Required if using USB HS PHY	2.97	3.00	3.03	kΩ

6.3.16 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 52. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write/erase 8-bit mode, V_{DD} = 1.7 V	-	6.7	-	mA
		Write/erase 16-bit mode, V_{DD} = 2.1 V	-	9.2	-	
		Write/erase 32-bit mode, V_{DD} = 3.3 V	-	12.6	-	

Table 53. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 Kbytes) erase time	Program/erase parallelism (PSIZE) = x 8	-	346	418	ms
		Program/erase parallelism (PSIZE) = x 16	-	252	312	
		Program/erase parallelism (PSIZE) = x 32	-	208	265	
$t_{ERASE128KB}$	Sector (128 Kbytes) erase time	Program/erase parallelism (PSIZE) = x 8	-	1953	2500	ms
		Program/erase parallelism (PSIZE) = x 16	-	1252	1639	
		Program/erase parallelism (PSIZE) = x 32	-	927	1322	
$t_{ERASE64KB}$	Sector (64 Kbytes) erase time	Program/erase parallelism (PSIZE) = x 8	-	1027	1298	ms
		Program/erase parallelism (PSIZE) = x 16	-	675	840	
		Program/erase parallelism (PSIZE) = x 32	-	505	682	

Table 53. Flash memory programming (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	7718	9883	ms
		Program/erase parallelism (PSIZE) = x 16	-	4869	6379	
		Program/erase parallelism (PSIZE) = x 32	-	3503	5180	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10 K erase operations.

Table 54. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 Kbytes) erase time		-	180	-	ms
$t_{ERASE128KB}$	Sector (128 Kbytes) erase time		-	900	-	
$t_{ERASE64KB}$	Sector (64 Kbytes) erase time		-	450	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 10 K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 55. Flash memory endurance and data retention

Symbol	Parameter	Conditions(1)	Value	Unit
			Min(2)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles

Table 55. Flash memory endurance and data retention (continued)

Symbol	Parameter	Conditions[1]	Value	Unit
			Min[2]	
t_{RET}	Data retention	1 kcycle[3] at T_A = 85 °C	30	Years
		1 kcycle[3] at T_A = 105 °C	10	
		10 kcycles[3] at T_A = 55 °C	20	

1. Tj can not go above 125°C (current consumption limitation).
2. Guaranteed by characterization results.
3. Cycling performed over the whole temperature range.

6.3.17 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 56*. They are based on the EMS levels and classes defined in application note AN1709.

Table 56. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 216 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A =+25 °C, f_{HCLK} = 216 MHz, conforms to IEC 61000-4-2	5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 57. EMI characteristics for f_{HSE} = 25 MHz and f_{HCLK} = 250 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/200 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, conforming to IEC61967-2 ART/L1-cache OFF, over-drive ON, all peripheral clocks enabled, clock dithering disabled.	0.1 MHz to 30 MHz	23	dBµV
			30 MHz to 130 MHz	20	
			130 MHz to 1 GHz	34	
			1 GHz to 2 GHz	24	
			EMI Level	4	-

6.3.18 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size

depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

Table 58. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001-2012	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1-2009, all the packages excepted WLCSP100	3	250	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 59. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.19 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 60*.

Table 60. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0, PDR_ON, BYPASS_REG, OTG_HS_REXT	-0	0	mA
	Injected current on NRST	-0	NA(1)	
	Injected current on PF9, PF10, PH0_OSCIN, PH1_OSCOUT, PC0, PC1, PC2, PC3, PB14(2), PB15(2)	-0	NA(1)	
	Injected current on any other FT or FTf pins	-5	NA(1)	
	Injected current on any other pins	-5	+5	

1. Injection is not possible.
2. PB14 and PB15 in the STM32F723xx devices.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.20 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 61: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 16*. All I/Os are CMOS and TTL compliant.

Note: For information on GPIO configuration, refer to the application note AN4899 "STM32 GPIO configuration for hardware settings and low-power consumption" available from www.st.com.

Table 61. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.35V_{DD}-0.04$(1)	V
					$0.3V_{DD}$(2)	
	BOOT I/O input low level voltage	1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤105 °C	-	-	$0.1V_{DD}+0.1$(1)	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	-	-		
V_{IH}	FT, TTa and NRST I/O input high level voltage(5)	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3$(1)	-	-	V
			$0.7V_{DD}$(2)			
	BOOT I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤105 °C	$0.17V_{DD}+0.7$(1)	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				

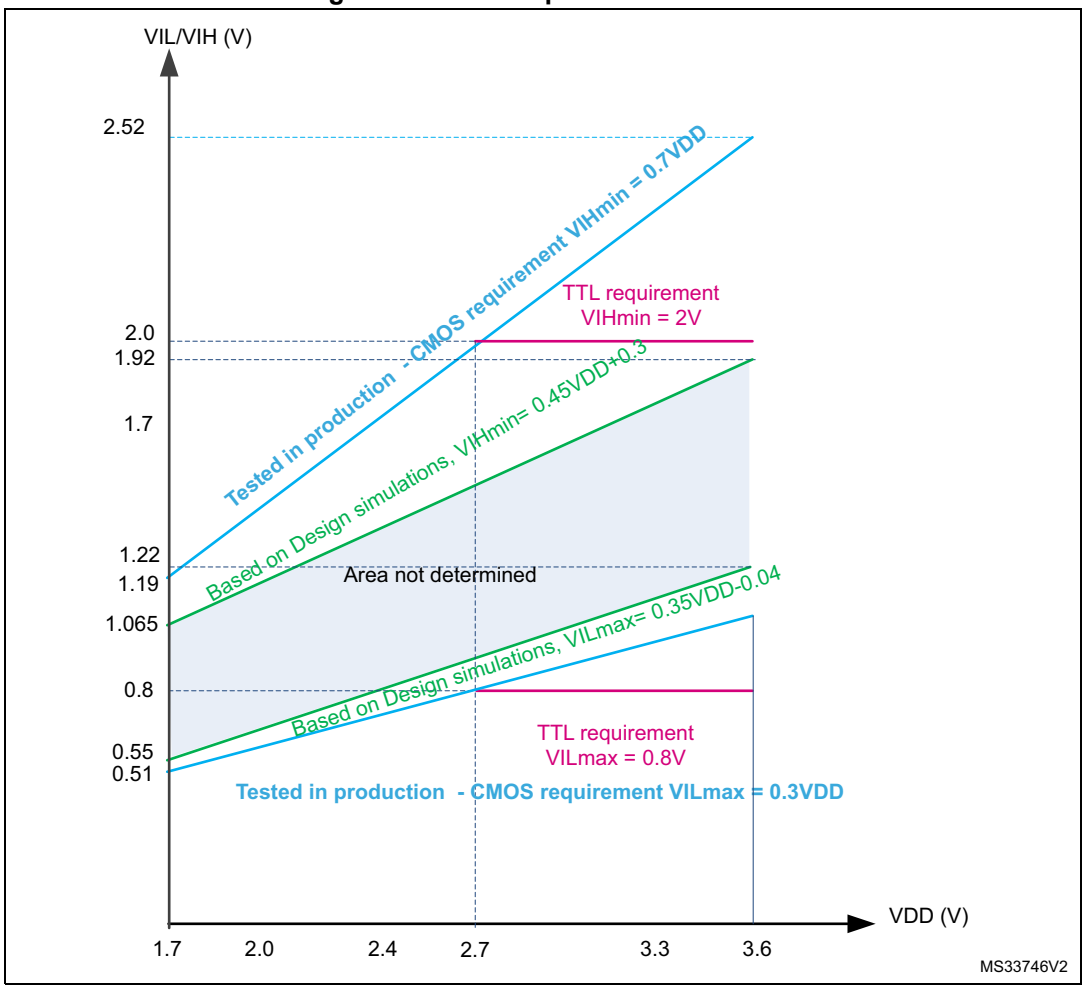
Table 61. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{HYS}	FT, TTa and NRST I/O input hysteresis		1.7 V≤V_{DD}≤3.6 V	10%V_{DD}(3)	-	-	V
	BOOT I/O input hysteresis		1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤105 °C	0.1	-	-	
			1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
I_{lkg}	I/O input leakage current (4)		V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	V_{IN} = V_{DD}	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 60: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 60: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 46*.

Figure 46. FT I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14, PC15 and PI8 which can sink or source up to ±3 mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed must not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 14*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 14*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 62* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*. All I/Os are CMOS and TTL compliant.

Table 62. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	CMOS port(2) I_{IO} = -8 mA 2.7 V ≤V_{DD} ≤3.6 V	V_{DD} − 0.4	-	
V_{OH}(3)	Output high level voltage for PC14	CMOS port(2) I_{IO} = -2 mA 2.7 V ≤V_{DD} ≤3.6 V	V_{DD} − 0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+8mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin except PC14	TTL port(2) I_{IO} =-8mA 2.7 V ≤V_{DD} ≤3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -20 mA 2.7 V ≤V_{DD} ≤3.6 V	V_{DD}−1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -6 mA 1.8 V ≤V_{DD} ≤3.6 V	V_{DD}−0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -4 mA 1.7 V ≤V_{DD} ≤3.6V	V_{DD}−0.4(5)	-	
V_{OH}(3)	Output high level voltage for PC14	I_{IO} = -1 mA 1.7 V ≤V_{DD} ≤3.6V	V_{DD}−0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 14*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 14* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 47* and *Table 63*, respectively.

Unless otherwise specified, the parameters given in *Table 63* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 63. I/O AC characteristics(1)(2)

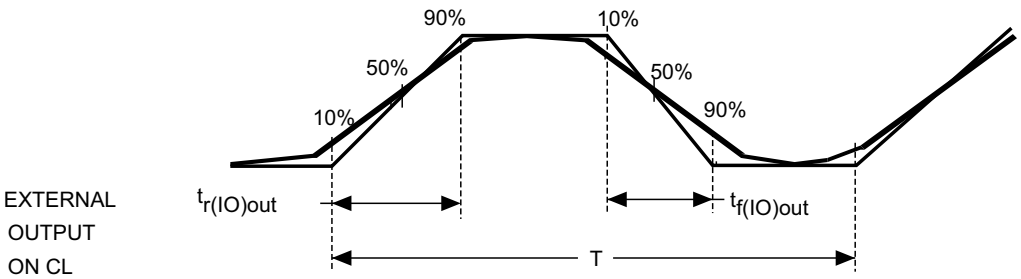
OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.7 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	4	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	3	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD}≥ 2.7 V	-	-	25	MHz
			C_L = 50 pF, V_{DD}≥ 1.8 V	-	-	12.5	
			C_L = 50 pF, V_{DD}≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	50	
			C_L = 10 pF, V_{DD}≥ 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	12.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} ≥ 2.7 V	-	-	10	ns
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	6	
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	20	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} ≥ 2.7 V	-	-	50(4)	MHz
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	25	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} ≥2.7 V	-	-	6	ns
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	4	
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	6	

Table 63. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
			C_L = 10 pF, V_{DD}≥ 2.7 V	-	-	180(4)	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	100	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	72.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥1.8 V	-	-	6	
			C_L = 30 pF, V_{DD} ≥1.7 V	-	-	7	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	2.5	
			C_L = 10 pF, V_{DD} ≥1.8 V	-	-	3.5	
			C_L = 10 pF, V_{DD} ≥1.7 V	-	-	4	
-	tEXTIpw	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F72xxx and STM32F73xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 47*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

Figure 47. I/O AC characteristics definition



Maximum frequency is achieved with a duty cycle at (45-55%) when loaded by the specified capacitance.

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6.3.21 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 61: I/O static characteristics*).

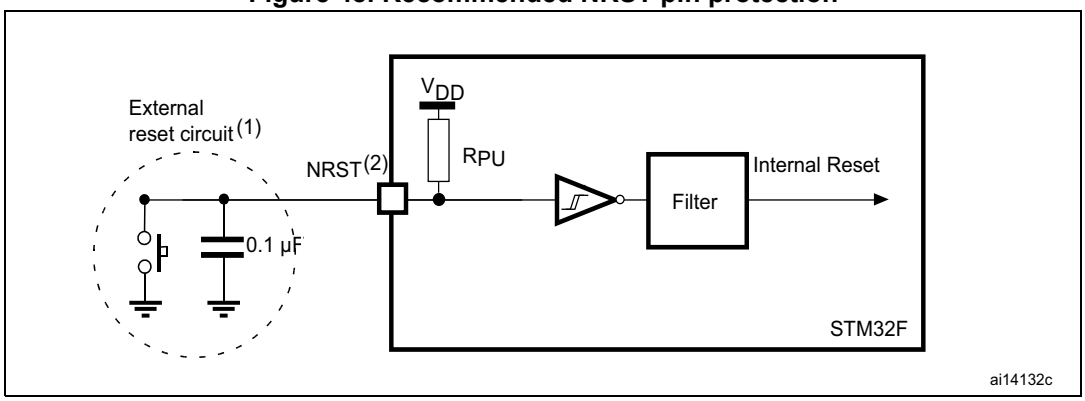
Unless otherwise specified, the parameters given in *Table 64* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 64. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 48. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets. 0.1 uF capacitor must be placed as close as possible to the chip.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 61*. Otherwise the reset is not taken into account by the device.

6.3.22 TIM timer characteristics

The parameters given in *Table 65* are guaranteed by design.

Refer to *Section 6.3.20: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 65. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 216 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 108 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 216 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1 to TIM12 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 216 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCLK, otherwise TIMxCLK = 4x PCLKx.

6.3.23 RTC characteristics

Table 66. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

6.3.24 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 67* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 16*.

Table 67. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	$V_{DDA} - V_{REF+} < 1.2$ V	1.7(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.7(1)	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	0	-	V
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz

Table 67. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance	-	1.5	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$
f_S(2)	Sampling rate (f_{ADC} = 36 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2.4	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	4.5	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	7.2	Msps

Table 67. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD} = 1.7 V, and minimum value for V_{DD} = 3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 67*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 68. ADC static accuracy at f_{ADC} = 18 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Guaranteed by characterization results.

Table 69. ADC static accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, V_{DDA} –V_{REF} < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Guaranteed by characterization results.

Table 70. ADC static accuracy at f_{ADC} = 36 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Guaranteed by characterization results.

Table 71. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz V_{DDA} = V_{REF+}= 1.7 V Input Frequency = 20 kHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		− 67	− 72	-	

1. Guaranteed by characterization results.

Table 72. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions(1)

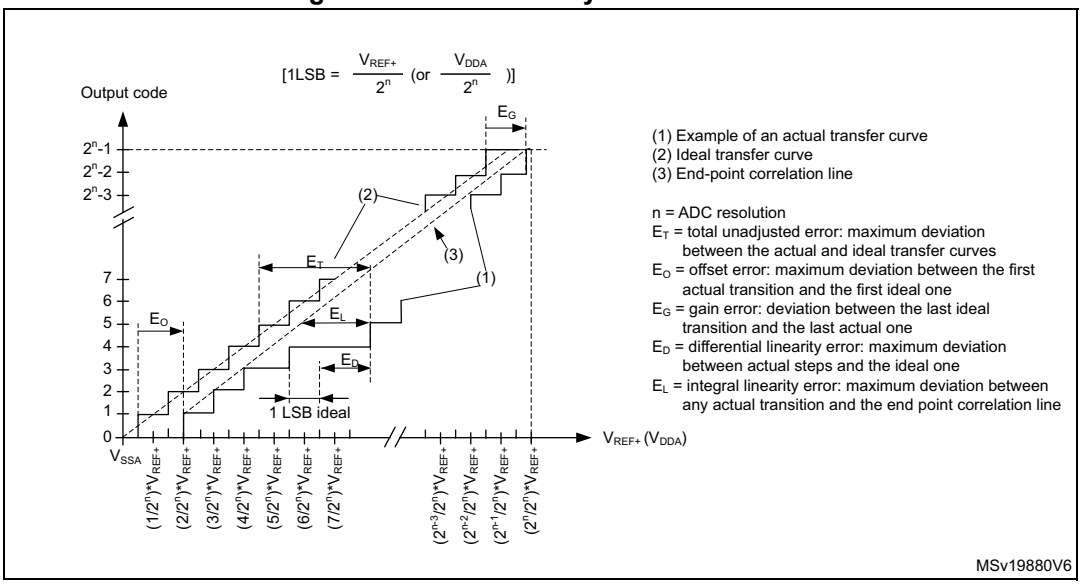
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =36 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		− 70	− 72	-	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

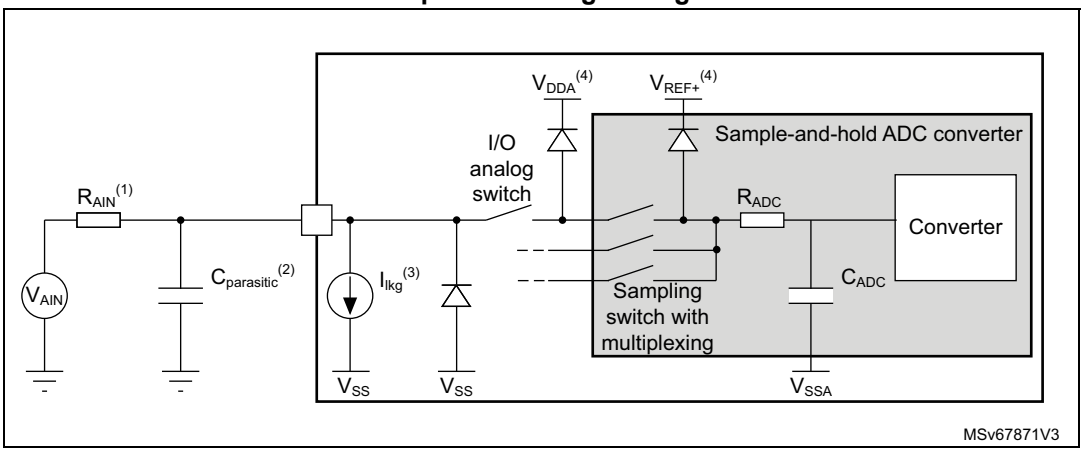
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.20 does not affect the ADC accuracy.

Figure 49. ADC accuracy characteristics



1. See also *Table 69*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 50. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function

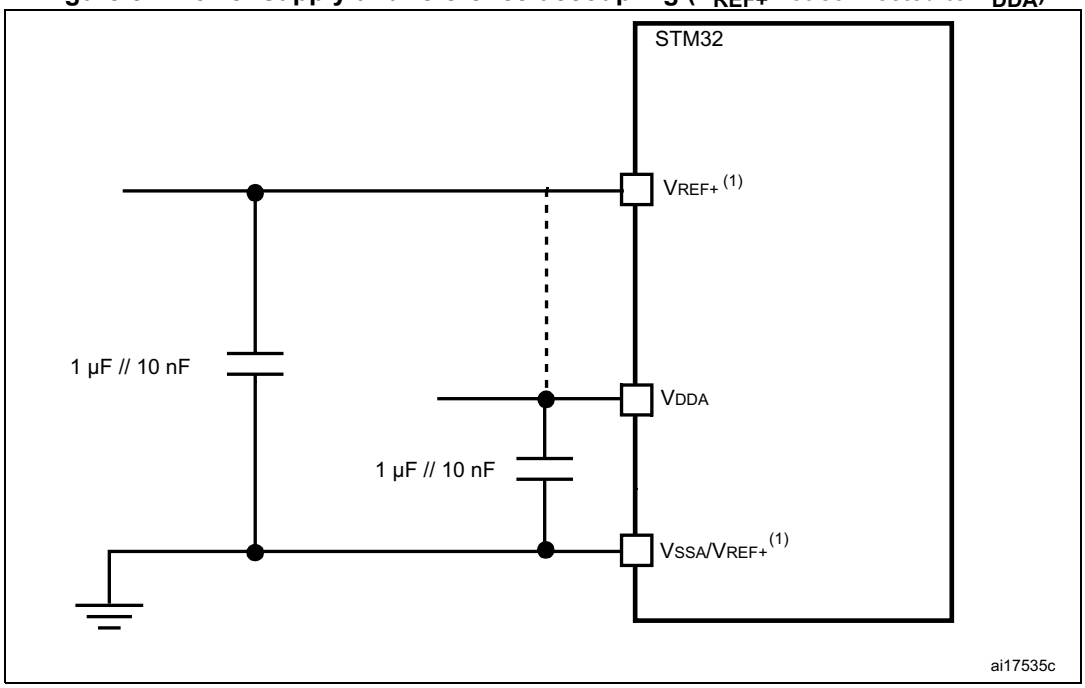


1. Refer to *Table 67* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 61: I/O static characteristics*). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 61: I/O static characteristics*.
4. Refer to *Figure 51: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})* and *Figure 52: Power supply and reference decoupling (V_{REF+} connected to V_{DDA})*.

General PCB design guidelines

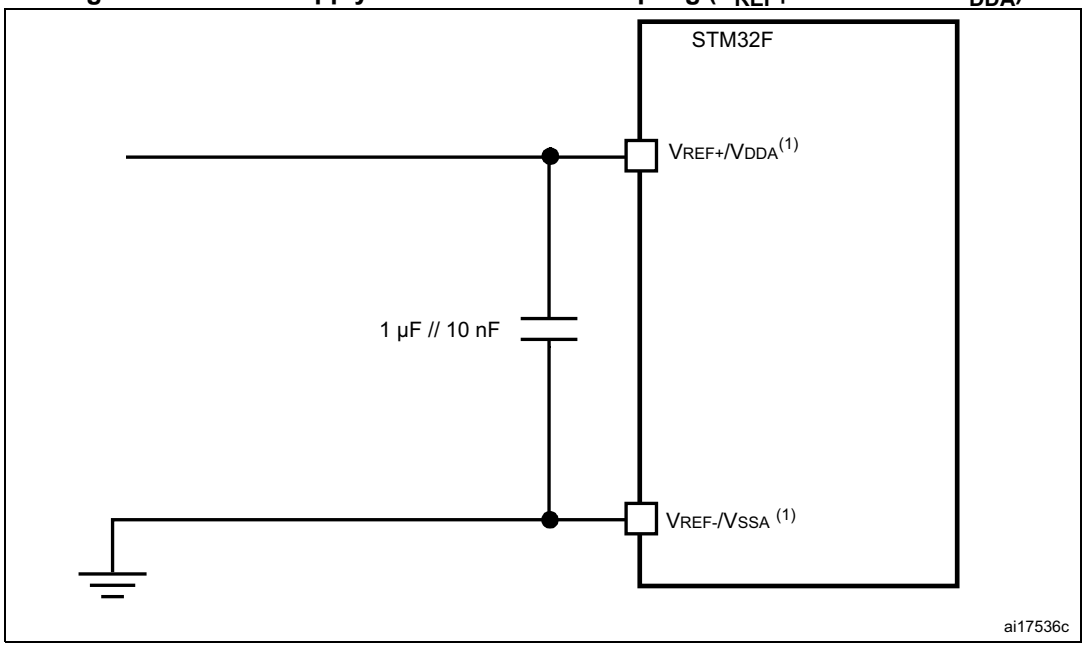
Power supply decoupling should be performed as shown in *Figure 51* or *Figure 52*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 51. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is available on all the packages except LQFP64, whereas the V_{REF-} is available only on UFBGA176 and UFBGA144. When V_{REF-} is not available, it is internally connected to V_{SSA}.

Figure 52. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is available on all the packages except LQFP64, whereas the V_{REF-} is available only on UFBGA176 and UFBGA144. When V_{REF-} is not available, it is internally connected to V_{SSA}.

6.3.25 Temperature sensor characteristics

Table 73. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 74. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FF0 7A2C - 0x1FF0 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FF0 7A2E - 0x1FF0 7A2F

6.3.26 V_{BAT} monitoring characteristics

Table 75. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.27 Reference voltage

The parameters given in *Table 76* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 76. internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV

Table 76. internal reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 77. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C $_{VDDA}$ = 3.3 V	0x1FF0 7A2A - 0x1FF0 7A2B

6.3.28 DAC electrical characteristics

Table 78. DAC characteristics

Symbol	Parameter		Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage		1.7(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage		1.7(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground		0	-	0	V	-
R_{LOAD}(2)	Resistive load with buffer ON	Connected to V_{SSA}	5	-	-	kΩ	-
		Connected to V_{DDA}	25	-	-	kΩ	-
R_O(2)	Impedance output with buffer OFF		-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load		-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON		0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON		-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF		-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF		-	-	V_{REF+} – 1LSB	V	

Table 78. DAC characteristics (continued)

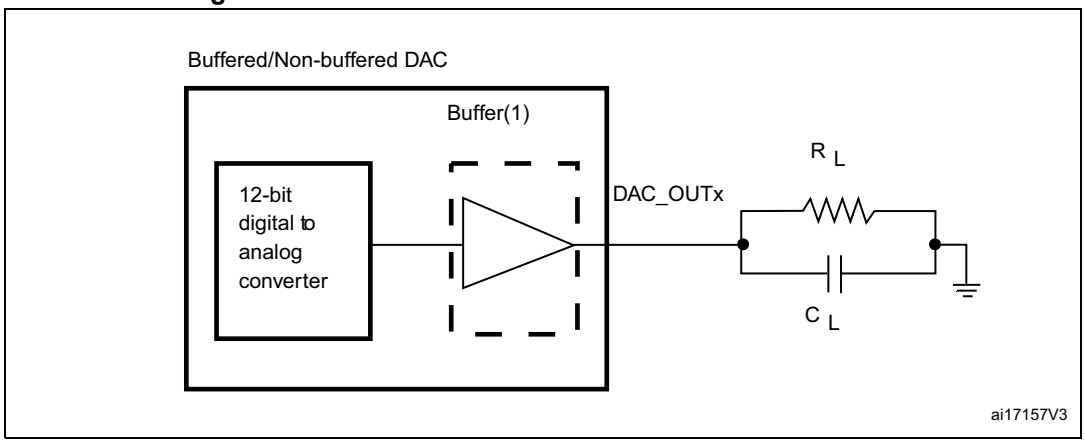
Symbol	Parameter	Min	Typ	Max	Unit	Comments
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}(4)	DAC DC V_{DDA} current consumption in quiescent mode(3)	-	280	380	µA	With no load, middle code (0x800) on the inputs
		-	475	625	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(4)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(4)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(4)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(4)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(4)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB	-	3	6	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
THD(4)	Total Harmonic Distortion Buffer ON	-	-	-	dB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ

Table 78. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t_{WAKEUP} (4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

Figure 53. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.29 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0431 reference manual) and when the I2CCLK frequency is greater than the minimum shown in the table below:

Table 79. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog Filter ON DNF=0	10	
			Analog Filter OFF DNF=1	9	
		Fast-mode Plus	Analog Filter ON DNF=0	22.5	
			Analog Filter OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The 20mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{load} supported in Fm+, which is given by these formulas:

- $Tr(SDA/SCL)=0.8473 \times R_p \times C_{load}$
- $R_p(min)= (V_{DD} - V_{OL}(max))/I_{OL}(max)$

Where Rp is the I2C lines pull-up. Refer to *Section 6.3.20: I/O port characteristics* for the I2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 80. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 81* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 81. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode SPI1,4,5 2.7≤VDD≤3.6	-	-	54(2)	MHz
		Master mode SPI1,4,5 1.71≤VDD≤3.6	-	-	27	
		Master transmitter mode SPI1,4,5 1.71≤VDD≤3.6	-	-	54	
		Slave receiver mode SPI1,4,5 1.71≤VDD≤3.6	-	-	54	
		Slave mode transmitter/full duplex SPI1,4,5 2.7≤VDD≤3.6	-	-	50(3)	
		Slave mode transmitter/full duplex SPI1,4,5 1.71≤VDD≤3.6	-	-	37(3)	
		Master & Slave mode SPI2,3 1.71≤VDD≤3.6	-	-	27	
tsu(NSS)	NSS setup time	Slave mode, SPI presc = 2	4xTpclk	-	-	ns
th(NSS)	NSS hold time	Slave mode, SPI presc = 2	2xTpclk	-	-	
tw(SCKH) tw(SCKL)	SCK high and low time	Master mode	Tpclk-1	Tpclk	Tpclk+1	

Table 81. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tsu(MI)	Data input setup time	Master mode	5	-	-	ns
tsu(SI)		Slave mode	2	-	-	
th(MI)	Data input hold time	Master mode	3	-	-	
th(SI)		Slave mode	1	-	-	
ta(SO)	Data output access time	Slave mode	7	9	21	
tdis(SO)	Data output disable time	Slave mode	5	7	12	
tv(SO)	Data output valid time	Slave mode 2.7≤VDD≤3.6V	-	6.5	10	
		Slave mode 1.71≤VDD≤3.6V	-	6.5	13.5	
tv(MO)		Master mode	-	2	3	
th(SO)	Data output hold time	Slave mode 1.71≤VDD≤3.6V	4.5	-	-	
th(MO)		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Excepting SPI1 with SCK IO=PA5. In this configuration, the maximum achievable frequency is 40 MHz.
3. Maximum frequency of the slave transmitter is determined by sum of Tv(SO) and Tsu(MI) intervals which has to fit into SCK level phase preceding the SCK sampling edge.This value can be achieved when it communicates with a Master having Tsu(MI) = 0 while signal Duty(SCK) = 50%.

Figure 54. SPI timing diagram - slave mode and CPHA = 0

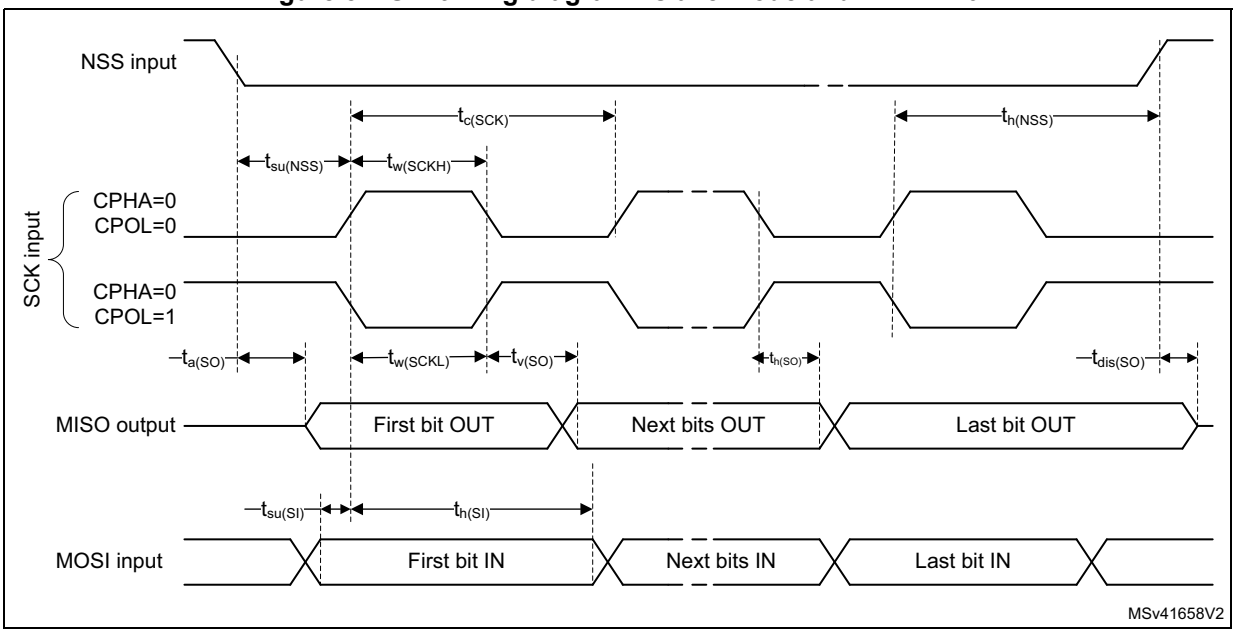


Figure 55. SPI timing diagram - slave mode and CPHA = 1

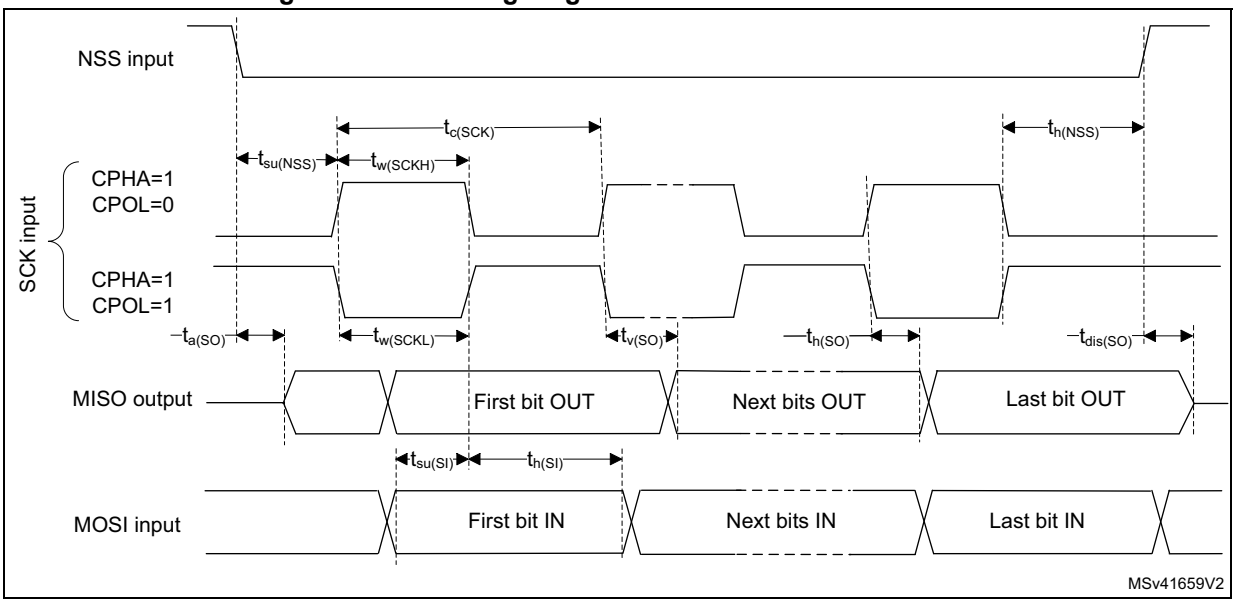
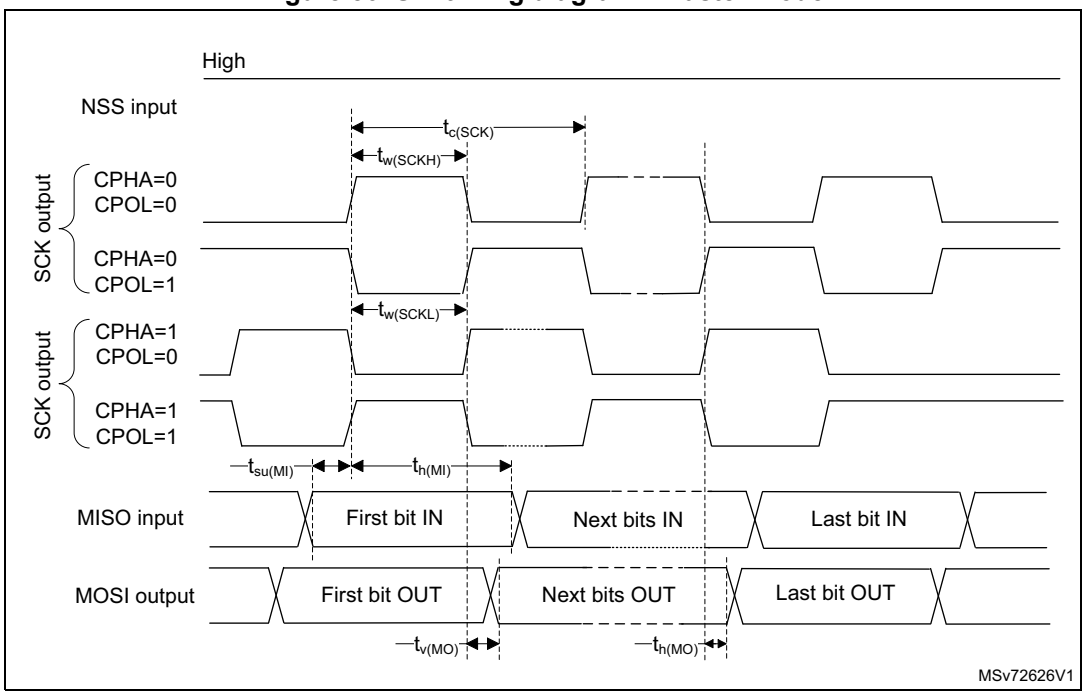


Figure 56. SPI timing diagram - master mode



I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 82* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 82. I²S dynamic characteristics(1)

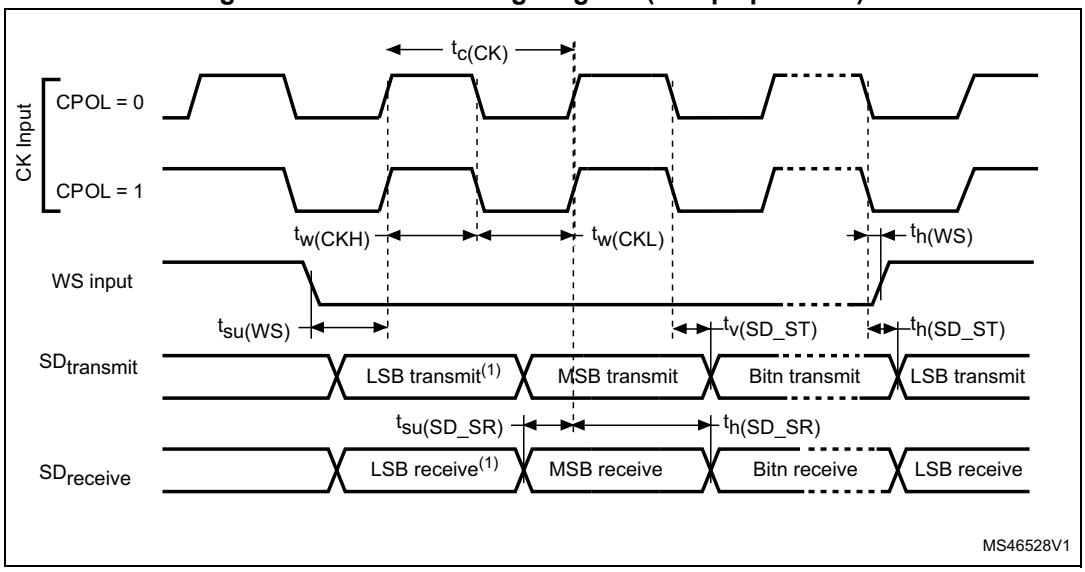
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	5	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD_SR)}$		Slave receiver	2.5	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD_SR)}$		Slave receiver	2	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	12	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.
2. 256xFs maximum is 49.152 MHz (APB1 Maximum frequency).

Note: Refer to RM0431 reference manual I2S section for more details on the sampling frequency (F_S).

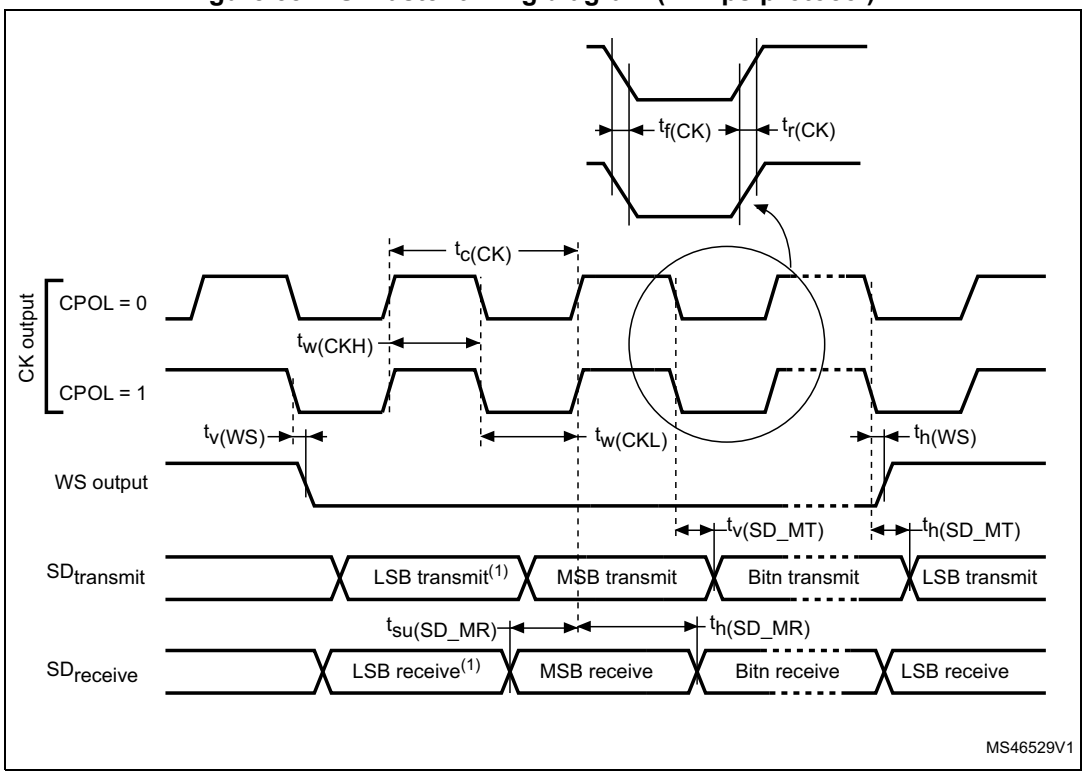
*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Figure 57. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 58. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 83* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 83. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCKL}	SAI main clock output	-	256x8K	256xFs	MHz
F_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128xFs(3)	
		Slave data: 32 bits	-	128xFs(3)	
$t_{v(FS)}$	FS valid time	Master mode 2.7≤VDD≤3.6V	-	18	ns
		Master mode 1.71≤VDD≤3.6V	-	20	
$t_{su(FS)}$	FS setup time	Slave mode	1	-	
$t_{h(FS)}$	FS hold time	Master mode	7	-	
		Slave mode	0.5	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD_B_SR)}$		Slave receiver	2.5	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD_B_SR)}$		Slave receiver	0.5	-	
$t_{v(SD_B_MT)}$	Data output valid time	Slave transmitter (after enable edge) 2.7≤VDD≤3.6V	-	11	
		Slave transmitter (after enable edge) 1.71≤VDD≤3.6V	-	18	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7≤VDD≤3.6V	-	16	
		Master transmitter (after enable edge) 1.71≤VDD≤3.6V	-	18.5	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	7.5	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With Fs = 192 kHz.

Figure 59. SAI master timing waveforms

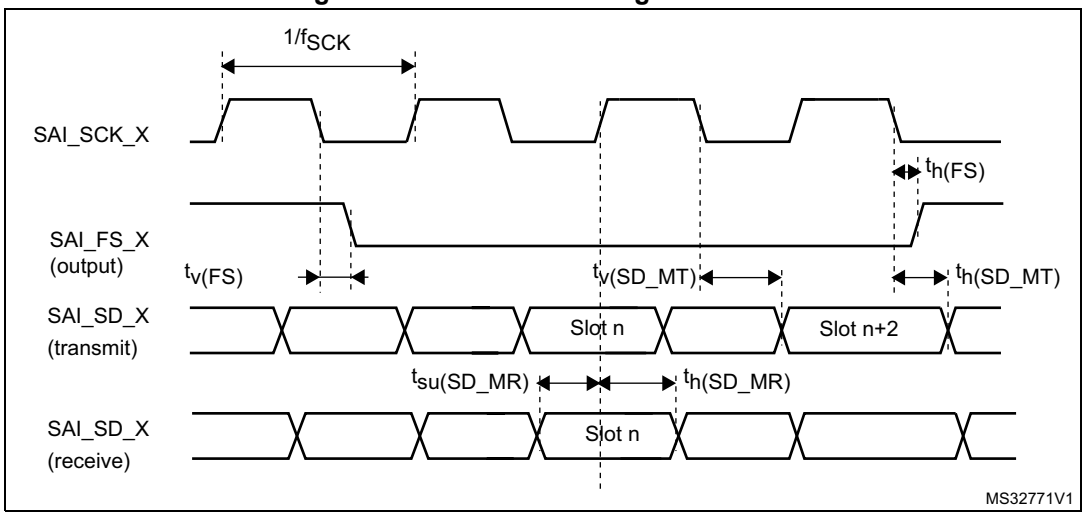
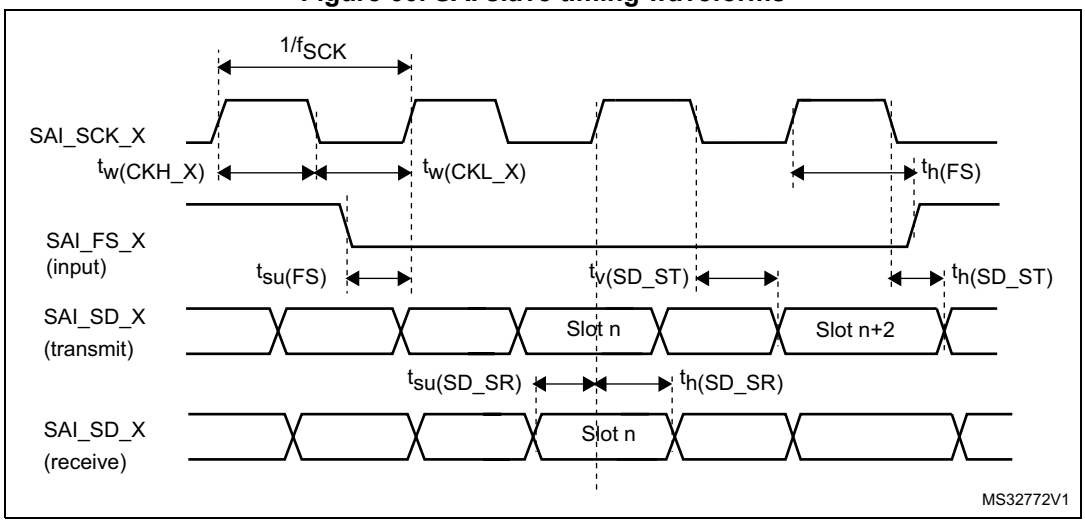


Figure 60. SAI slave timing waveforms



USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 84. USB OTG full speed startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG full speed transceiver startup time	1	µs

1. Guaranteed by design.

Table 85. USB OTG full speed DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DDUSB}	USB OTG full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12 (USB_FS_DP/DM)	V_{IN} = V_{DD}	14.25	-	24.8	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	V_{IN} = V_{DD}	2.4	5.2	8	
R_{PU}		PA12 (USB_FS_DP)	V_{IN} = $V_{SS, during\ idle}$	0.9	1.25	1.575	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	V_{IN} = $V_{SS, during\ reception}$	0.55	0.95	1.35	

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DDUSB} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.

Figure 61. USB OTG full speed timings: definition of data signal rise and fall time

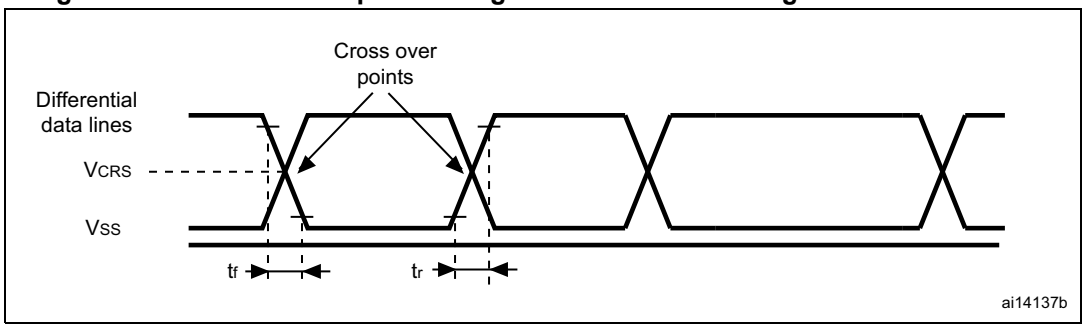


Table 86. USB OTG full speed electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	111	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

USB high speed (HS) characteristics (through ULPI in STM32F722xx devices)

Unless otherwise specified, the parameters given in *Table 89* for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 88* and V_{DD} supply voltage conditions summarized in *Table 87*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11, unless otherwise specified
- Capacitive load C = 20 pF, unless otherwise specified
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output characteristics.

Table 87. USB HS DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	USB OTG HS operating voltage	1.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 88. USB HS clock timing parameters(1)

Symbol	Parameter		Min	Typ	Max	Unit
-	f_{HCLK} value to guarantee proper operation of USB HS interface		30	-	-	MHz
F_{START_8BIT}	Frequency (first transition)	8-bit ±10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm		59.97	60	60.03	MHz
D_{START_8BIT}	Duty cycle (first transition)	8-bit ±10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm		49.975	50	50.025	%
t_{STEADY}	Time to reach the steady state frequency and duty cycle after the first transition		-	-	1.4	ms
t_{START_DEV}	Clock startup time after the de-assertion of SuspendM	Peripheral	-	-	5.6	ms
t_{START_HOST}		Host	-	-	-	
t_{PREP}	PHY preparation time after the first transition of the input clock		-	-	-	µs

1. Guaranteed by design.

Figure 62. ULPI timing diagram

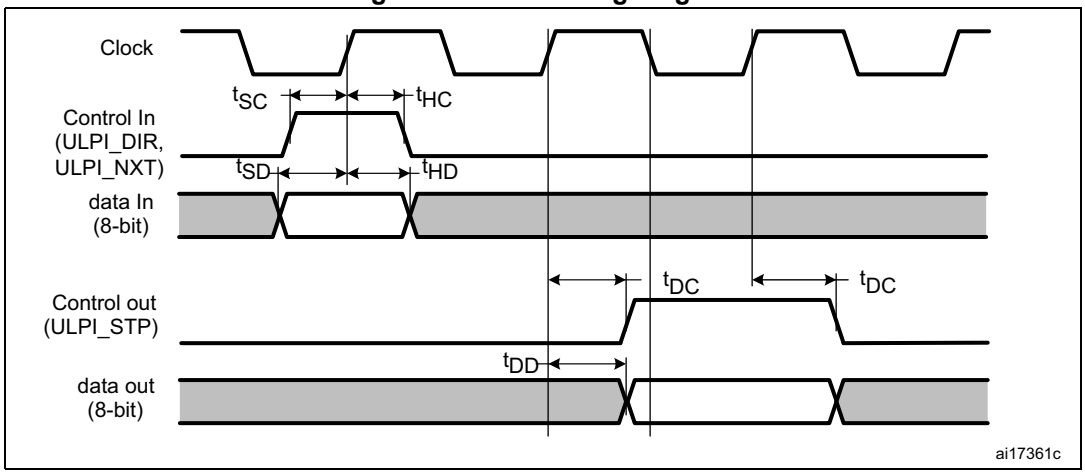


Table 89. Dynamic characteristics: USB ULPI(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	1.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	1	-	-	
t_{SD}	Data in setup time	-	1.5	-	-	
t_{HD}	Data in hold time	-	1	-	-	
t_{DC}/t_{DD}	Data/control output delay	2.7 V < V_{DD} < 3.6 V, C_L = 20 pF and OSPEEDRy[1:0] = 11	-	6	7.5	
		-	-	9.5	11	
		1.7 V < V_{DD} < 3.6 V, C_L = 15 pF and OSPEEDRy[1:0] = 11	-			

1. Guaranteed by characterization results.

USB high speed (HS) characteristics (embedded PHY High speed on STM32F723xx devices)

Table 90. USB OTG high speed DC electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hssq}	High speed squelch detection threshold	-	100	-	150	mV
V_{hsdsc}	High speed disconnect detection threshold	-	525	-	625	mV
V_{hsdif}	High speed differential detection threshold	-	100	-	-	mV
V_{hscm}	High speed data signaling common mode voltage range	-	-50	-	500	mV
V_{hsoi}	High speed idle level	-	-10	-	10	mV
V_{hsoh}	High speed data signaling high	-	360	-	440	mV
V_{hsol}	High speed data signaling low	-	-10	-	10	mV
V_{chirpj}	Chirp J level	-	700	-	1100	mV
V_{chirpk}	Chirp K level	-	-900	-	-500	mV

Table 91. USB OTG high speed electrical characteristics

Parameter	Comments	Conditions	Min	Typ	Max	Unit
t_{lr}	Rise time	-	0.5	-	-	ns
t_{lf}	Fall time	-	0.5	-	-	ns
t_{lrfm}	Setup time from INHSDRIVERENABLE=1 to the transition on INHSDATAP/INHSDATAN	-	10	-	-	ns
Z_{drv}	Driver output impedance	-	40.5	-	49.5	Ω

Table 92. USB FS PHY BCD electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDUSB}	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-	300	
R_{DAT_LKG}	Data line leakage resistance	-	300	-	-	kΩ
V_{DAT_LKG}	Data line leakage voltage	-	0.0	-	3.6	V
R_{DCP_DAT}	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
V_{LGC_HI}	Logic high	-	2.0	-	3.6	V
V_{LGC_LOW}	Logic low	-	-	-	0.8	
VL_{GC}	Logic threshold	-	0.8	-	2.0	
V_{DAT_REF}	Data detect voltage	-	0.25	-	3.6	
V_{DP_SRC}	D+ source voltage	-	0.5	-	3.6	
V_{DM_SRC}	D- source voltage	-	0.5	-	3.6	
I_{DM_SINK}	D- sink current	-	25	-	175	µA
I_{DP_SINK}	D+ sink current	-	25	-	175	
I_{DP_SRC}	Data contact detect current source	-	7	-	30	

CAN (controller area network) interface

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

6.3.30 FMC characteristics

Unless otherwise specified, the parameters given in *Table 93* to *Table 106* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output characteristics.

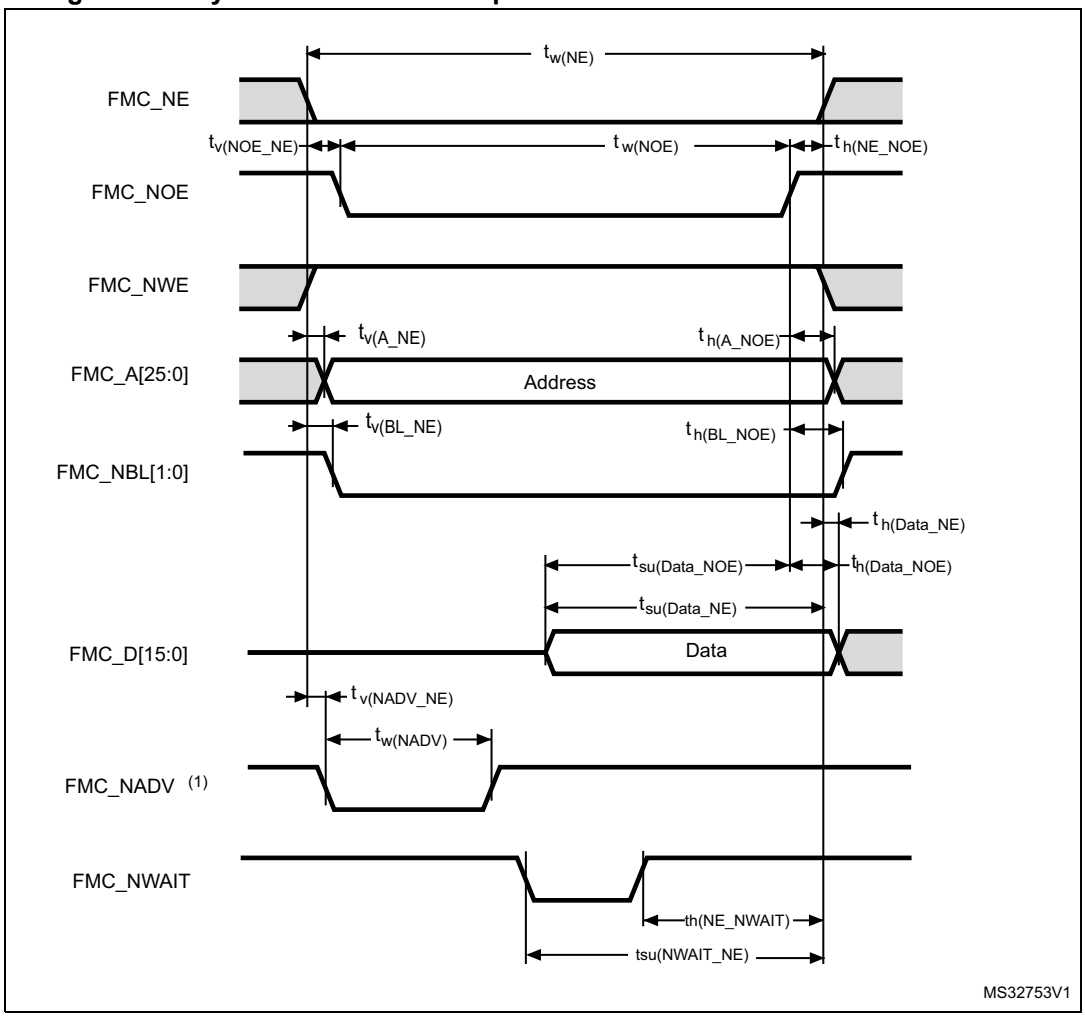
Asynchronous waveforms and timings

Figure 63 through *Figure 66* represent asynchronous waveforms and *Table 93* through *Table 100* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load CL = 30 pF

In all timing tables, the T_{HCLK} is the HCLK clock period

Figure 63. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 93. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	2Thclk -1	2Thclk +1	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	2Thclk -1	2Thclk +1	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	Thclk -1.5	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	Thclk -1.5	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	Thclk -0.5	

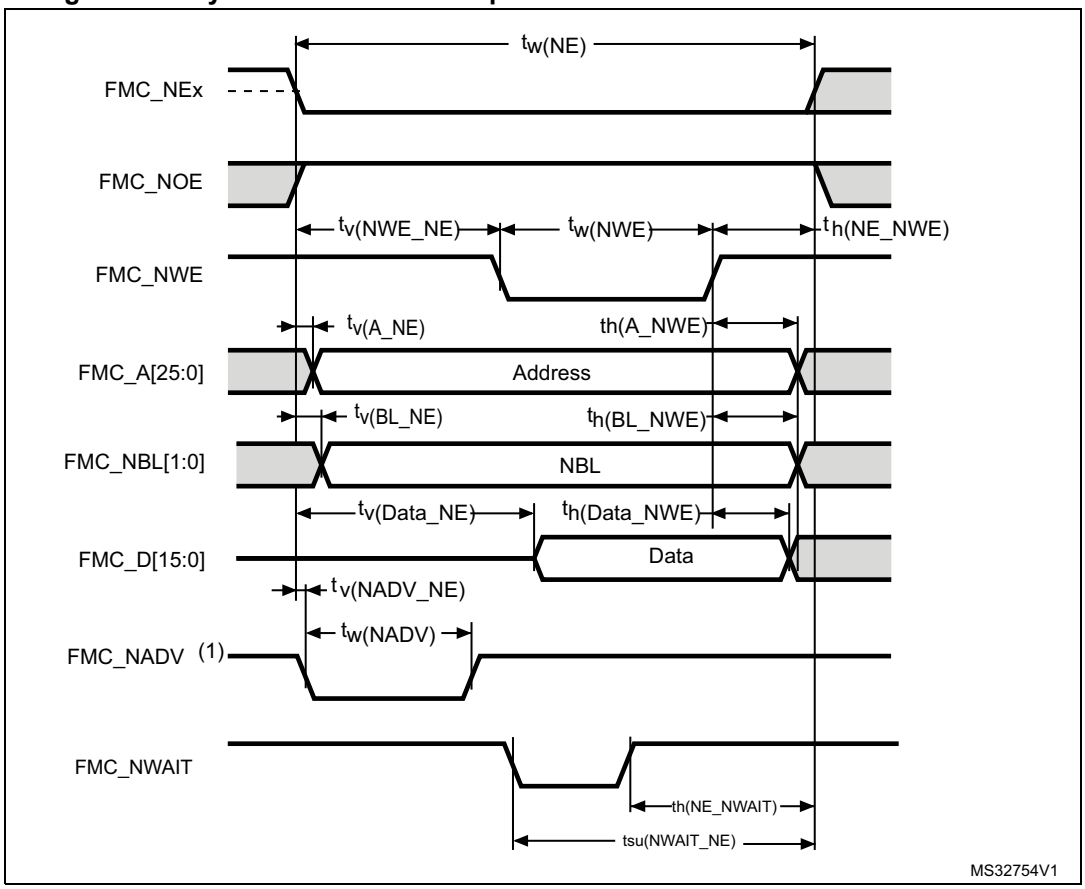
1. C_L = 30 pF.

Table 94. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	7Thclk +1	7Thclk +1	ns
$t_{w(NOE)}$	FMC_NWE low time	5Thclk -1	5Thclk +1	
$t_{w(NWAIT)}$	FMC_NWAIT low time	Thclk -0.5	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	5Thclk +1.5	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk +1	-	

1. Guaranteed by characterization results.

Figure 64. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 95. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3Thclk +1	3Thclk +1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	Thclk - 0.5	Thclk +0.5	
$t_{w(NWE)}$	FMC_NWE low time	Thclk - 1.5	Thclk +0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	Thclk	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	Thclk - 0.5	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	Thclk - 0.5	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	Thclk +1.5	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	Thclk +0.5	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	Thclk - 0.5	

1. Guaranteed by characterization results.

Table 96. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8Thclk -1	8Thclk +1	ns
$t_{w(NWE)}$	FMC_NWE low time	6Thclk -1.5	6Thclk +0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	6Thclk -1	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk + 2	-	

1. Guaranteed by characterization results.

Figure 65. Asynchronous multiplexed PSRAM/NOR read waveforms

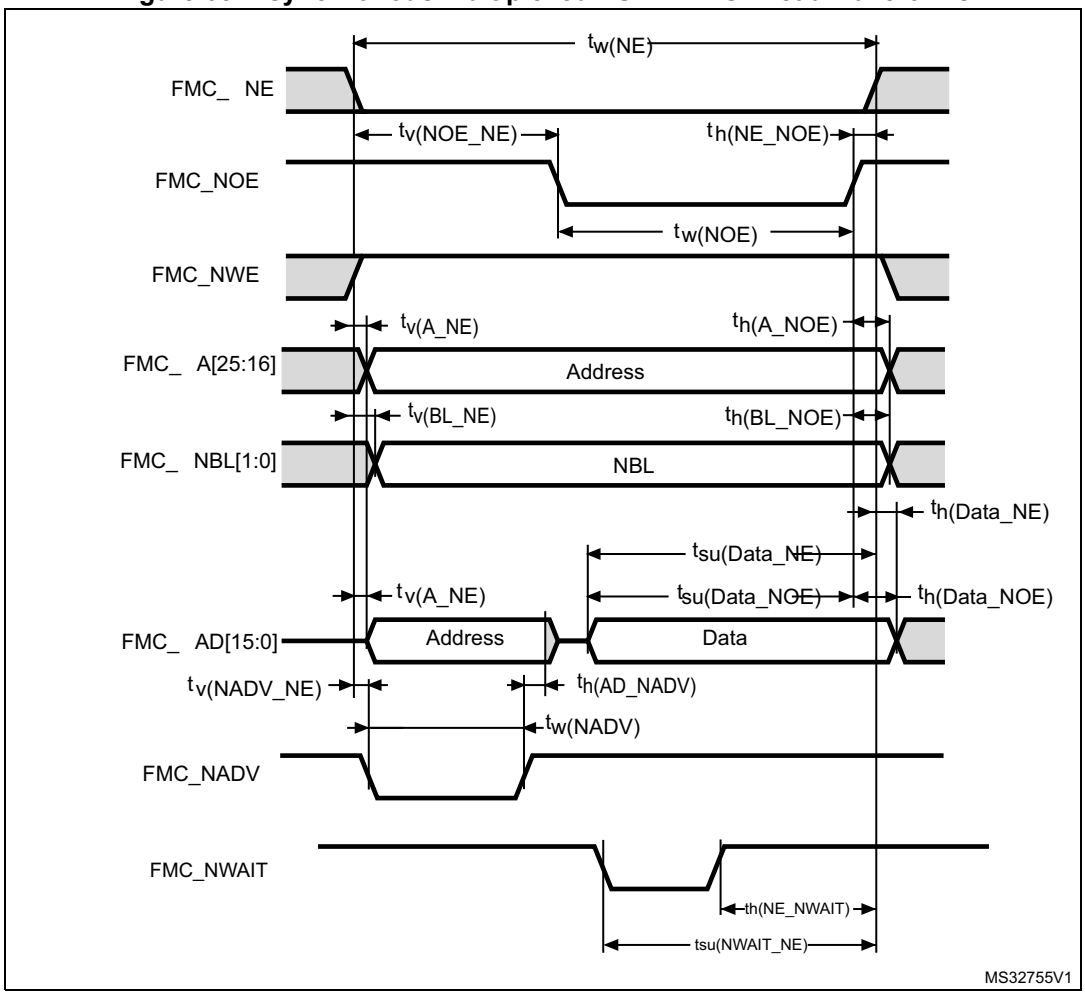


Table 97. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3Thclk -1	3Thclk +1	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	2Thclk	2Thclk +0.5	
$t_{tw(NOE)}$	FMC_NOE low time	Thclk -1	Thclk +1	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	Thclk -0.5	Thclk +1	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	Thclk +0.5	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	Thclk -0.5	-	
$t_{h(BL_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	Thclk -1.5	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	Thclk -1.5	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results.

Table 98. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8Thclk -1	8Thclk +1	ns
$t_{w(NOE)}$	FMC_NWE low time	5Thclk -1.5	8Thclk +0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	5Thclk +1.5	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk +1	-	

1. Guaranteed by characterization results.

Figure 66. Asynchronous multiplexed PSRAM/NOR write waveforms

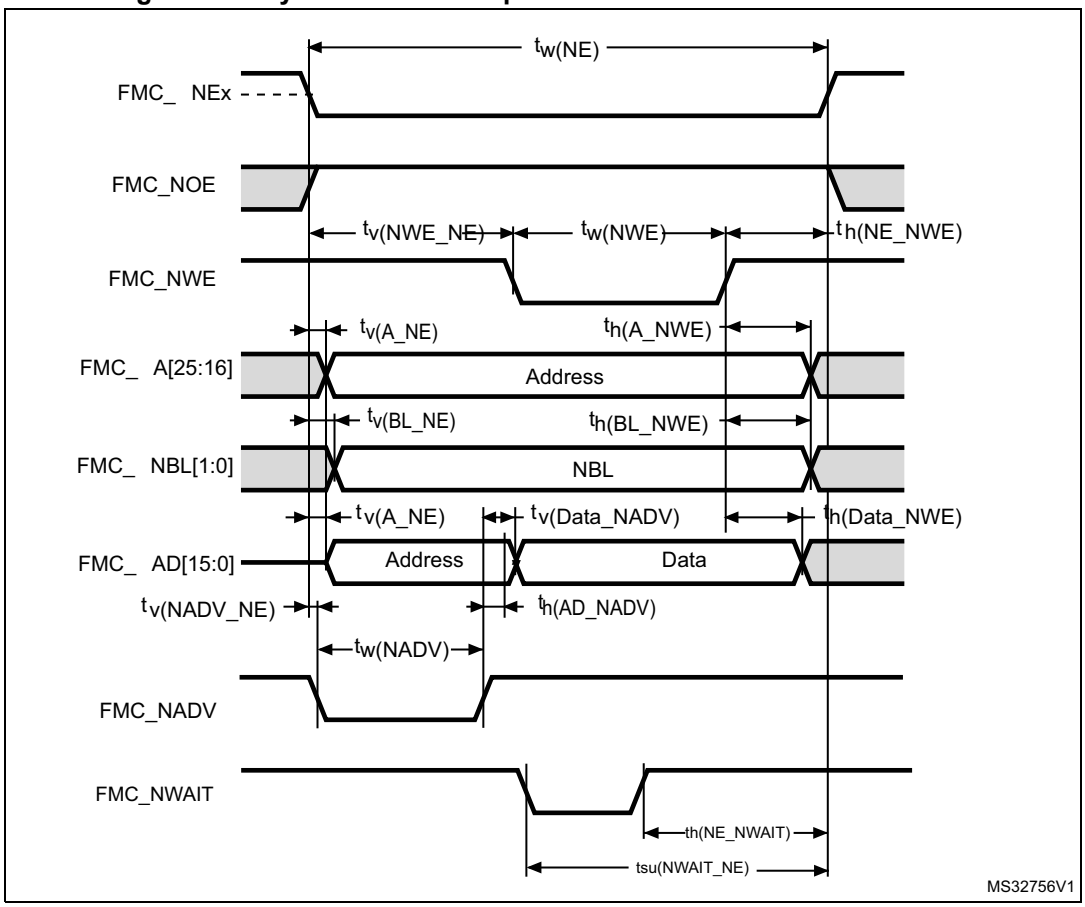


Table 99. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	4Thclk -1	4Thclk +1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	Thclk -0.5	Thclk +0.5	
$t_{w(NWE)}$	FMC_NWE low time	2Thclk -0.5	2Thclk +0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	Thclk -0.5	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	Thclk	Thclk +1	
$t_{h(AD_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	Thclk +0.5	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	Thclk +0.5	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	Thclk -0.5	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	Thclk +1.5	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	Thclk +0.5	-	

1. Guaranteed by characterization results.

Table 100. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9Thclk - 1	9Thclk + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	7Thclk -0.5	7Thclk + 0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	6Thclk + 2	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk - 1	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 67 through *Figure 70* represent synchronous waveforms and *Table 101* through *Table 104* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).
- For 1.71 V≤V_{DD}<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

Figure 67. Synchronous multiplexed NOR/PSRAM read timings

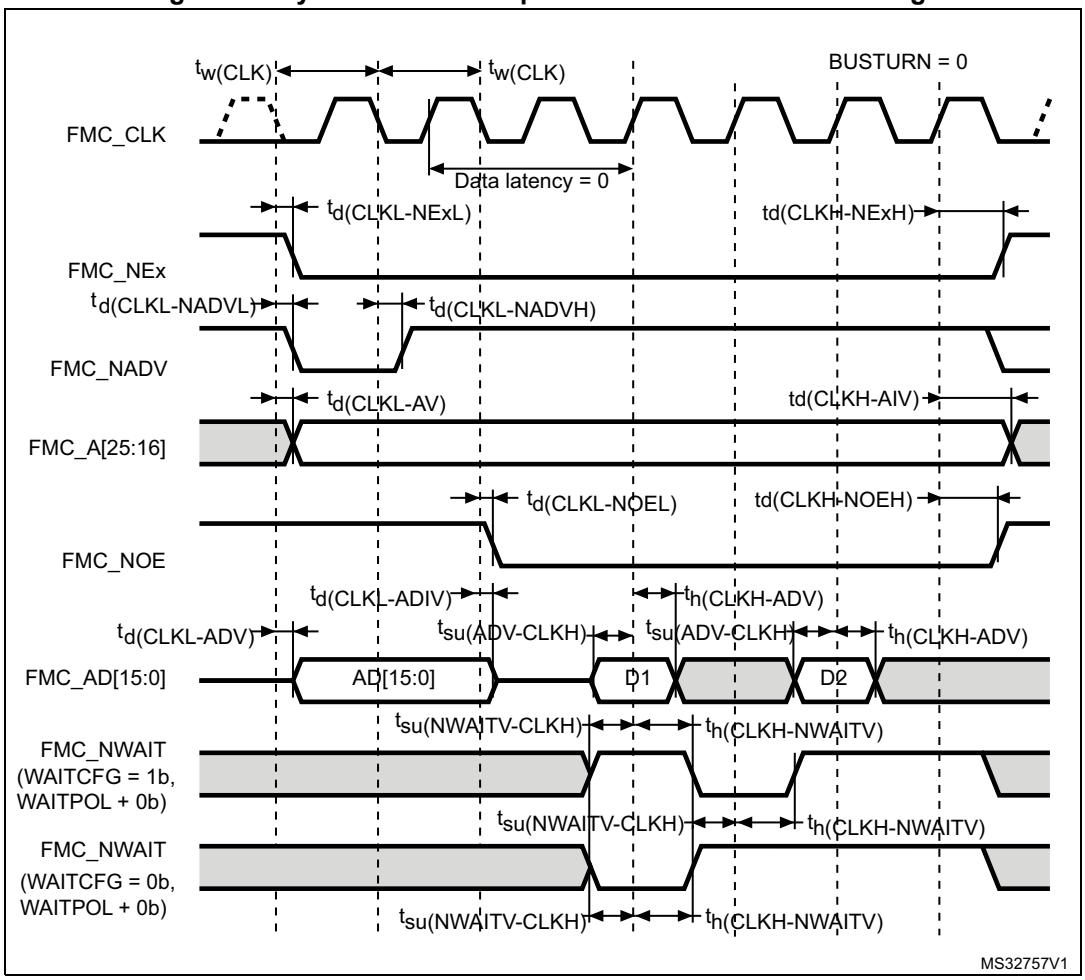


Table 101. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2Thclk - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	Thclk + 0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	Thclk	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	Thclk - 0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	2	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	1.5	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	3	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Figure 68. Synchronous multiplexed PSRAM write timings

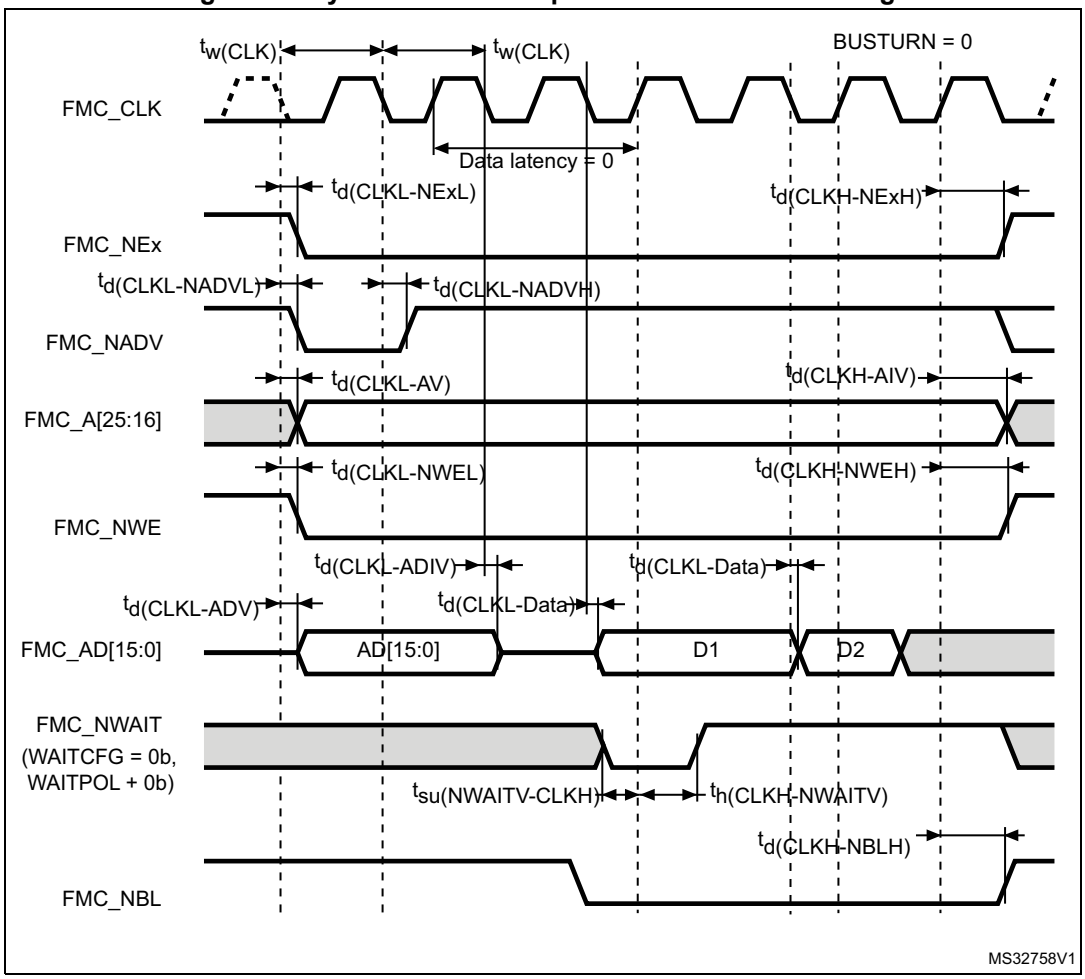


Table 102. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2Thclk - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	Thclk +0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	Thclk	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	Thclk +0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	Thclk +0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3	-	

1. Guaranteed by characterization results.

Figure 69. Synchronous non-multiplexed NOR/PSRAM read timings

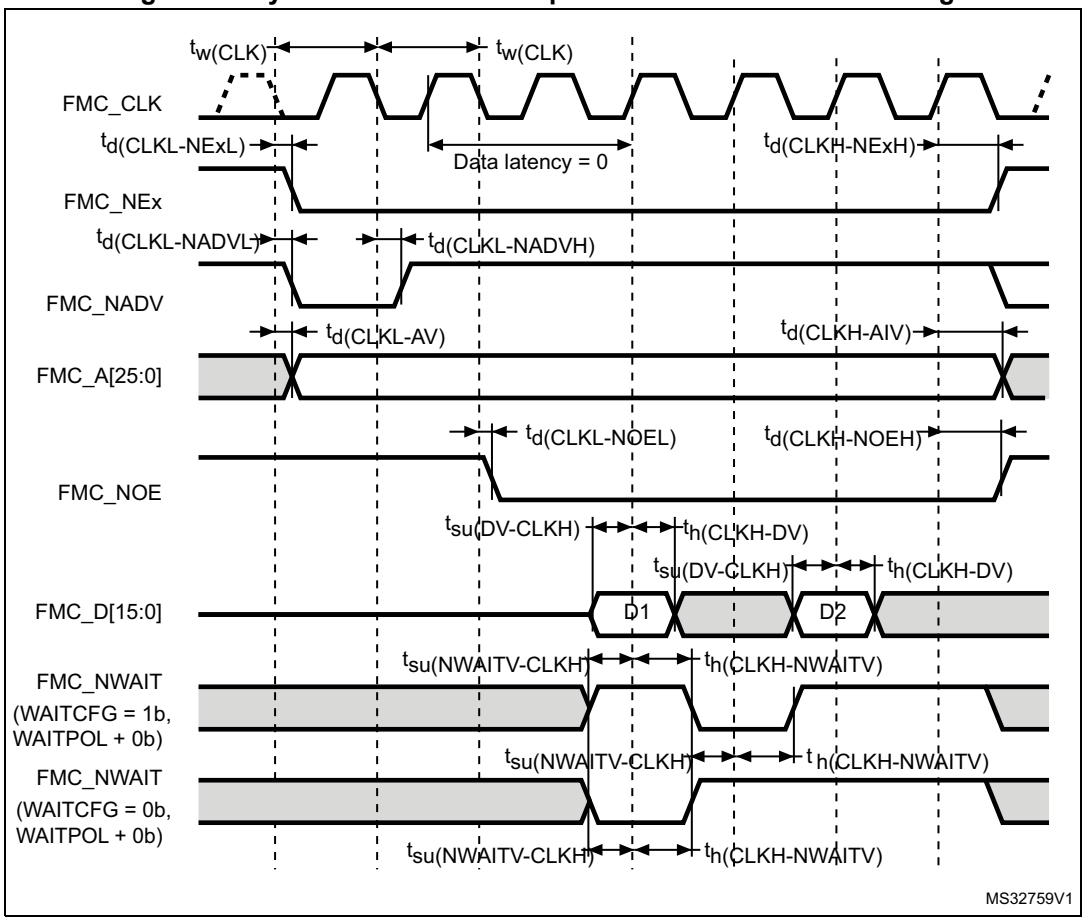


Table 103. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2Thclk - 0.5	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	Thclk +0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	Thclk	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	Thclk -0.5	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	1.5	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	3	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Figure 70. Synchronous non-multiplexed PSRAM write timings

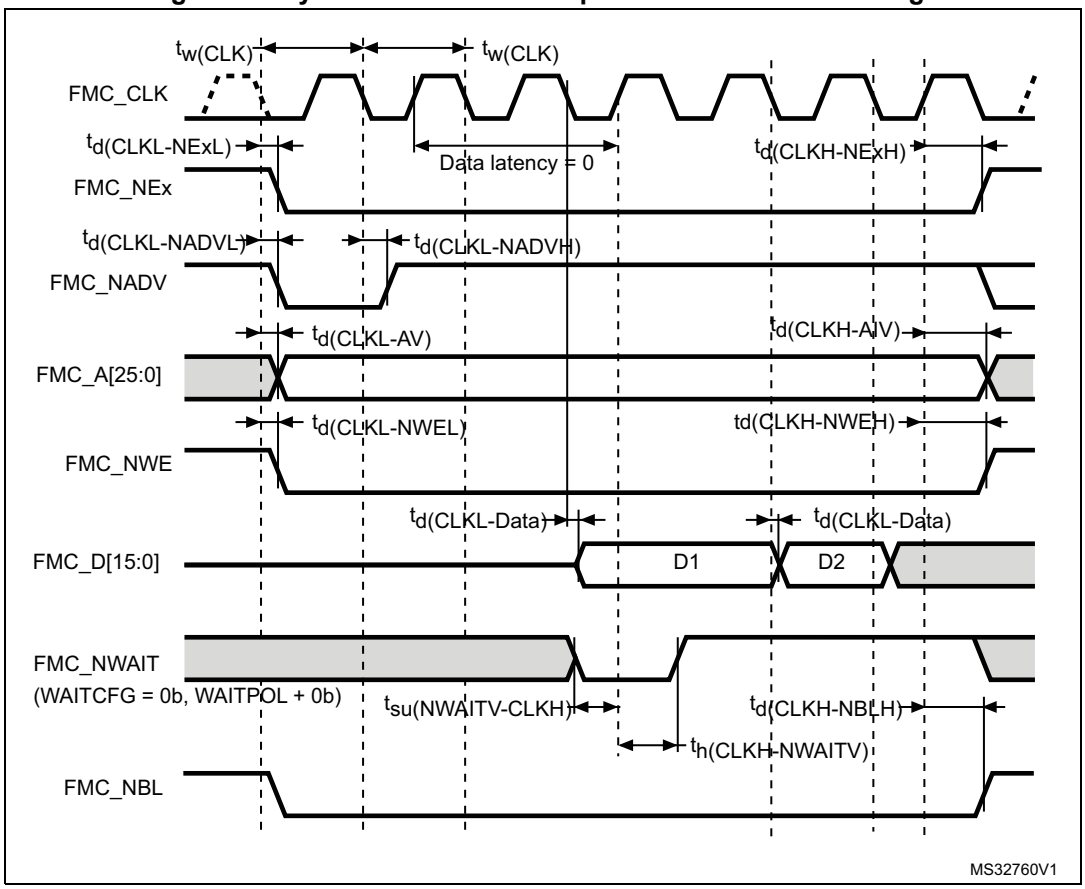


Table 104. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	2Thclk - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	Thclk +0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	Thclk	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	Thclk +1	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	Thclk +1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 71 represents synchronous waveforms, and *Table 105* and *Table 106* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 71. NAND controller waveforms for read access

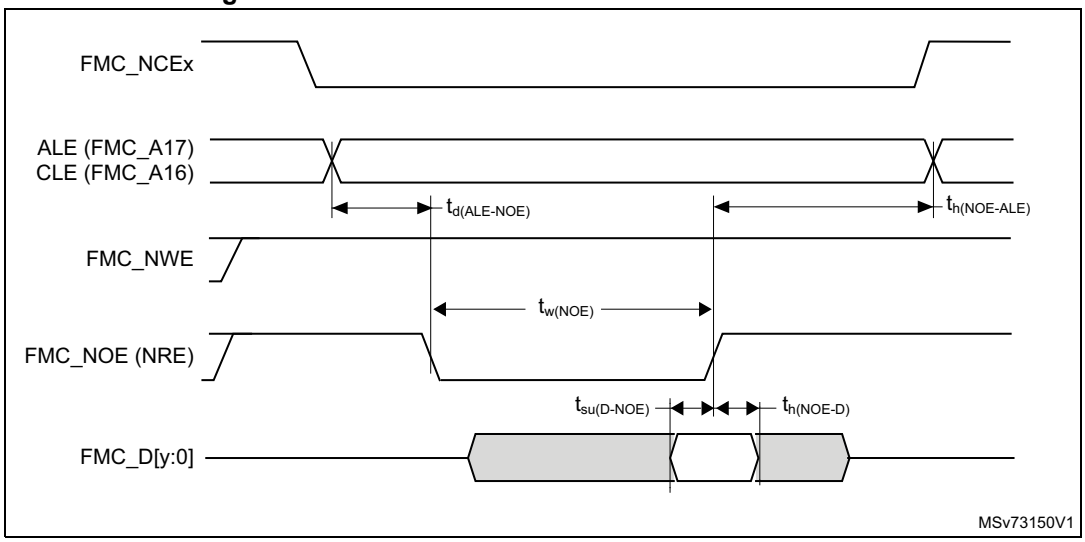


Figure 72. NAND controller waveforms for write access

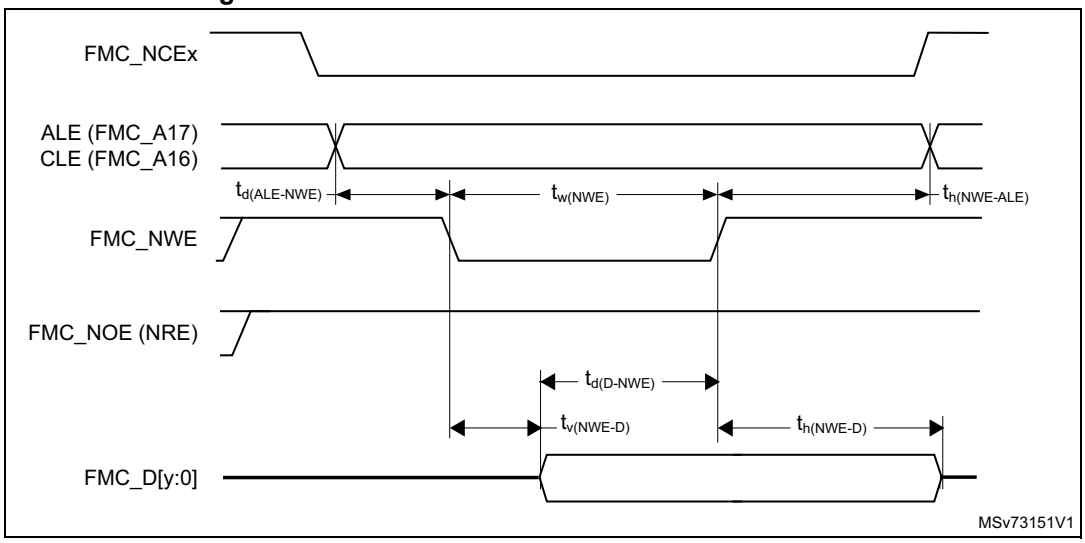


Table 105. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	4Thclk -0.5	4Thclk +0.5	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	11	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	3Thclk +1.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	4Thclk - 2	-	

1. Guaranteed by characterization results.

Table 106. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	4Thclk -0.5	4Thclk +0.5	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	2Thclk - 1	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	5Thclk - 1	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	3Thclk +1.5	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	2Thclk - 2	-	

1. Guaranteed by characterization results.

SDRAM waveforms and timings

- CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 3.0 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK= 100 MHz at CL=20 pF (on FMC_SDCLK).
- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For 1.71 V≤V_{DD}<1.9 V, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

Figure 73. SDRAM read access waveforms (CL = 1)

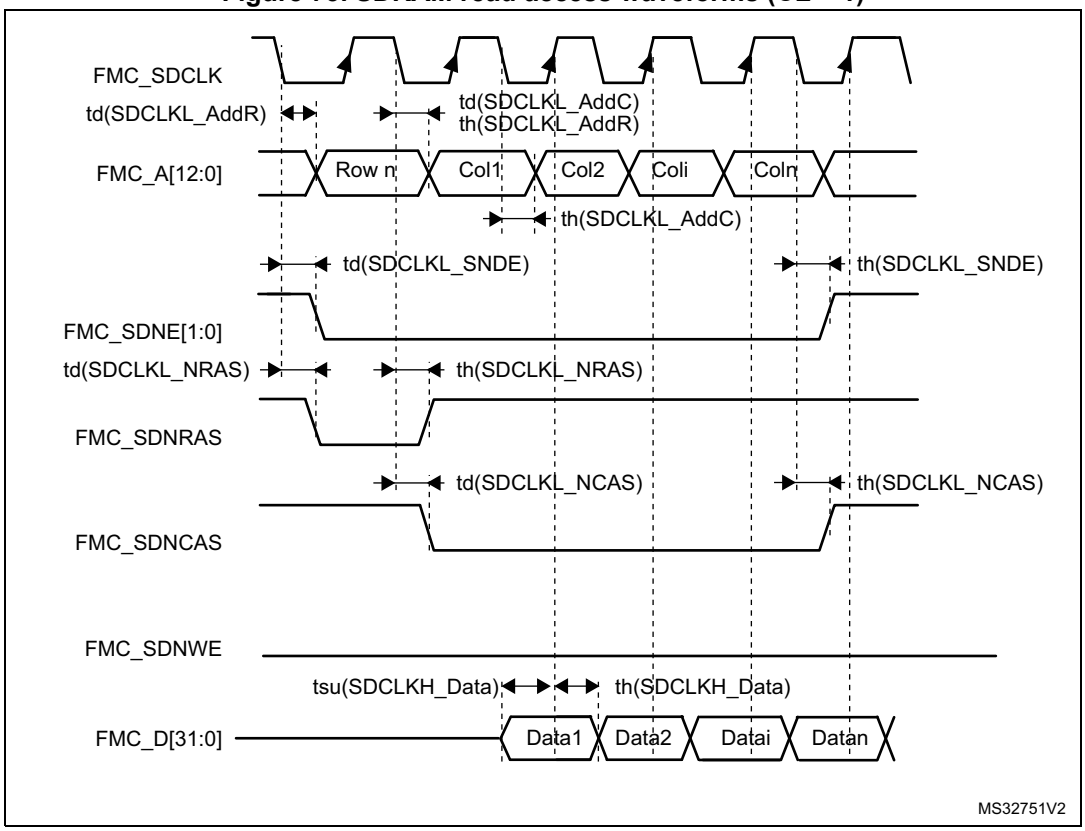


Table 107. SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2Thclk -0.5	2Thclk +0.5	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	2.5	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	1	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL- SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 108. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	2Thclk -0.5	2Thclk +0.5	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	1	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	3.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Figure 74. SDRAM write access waveforms

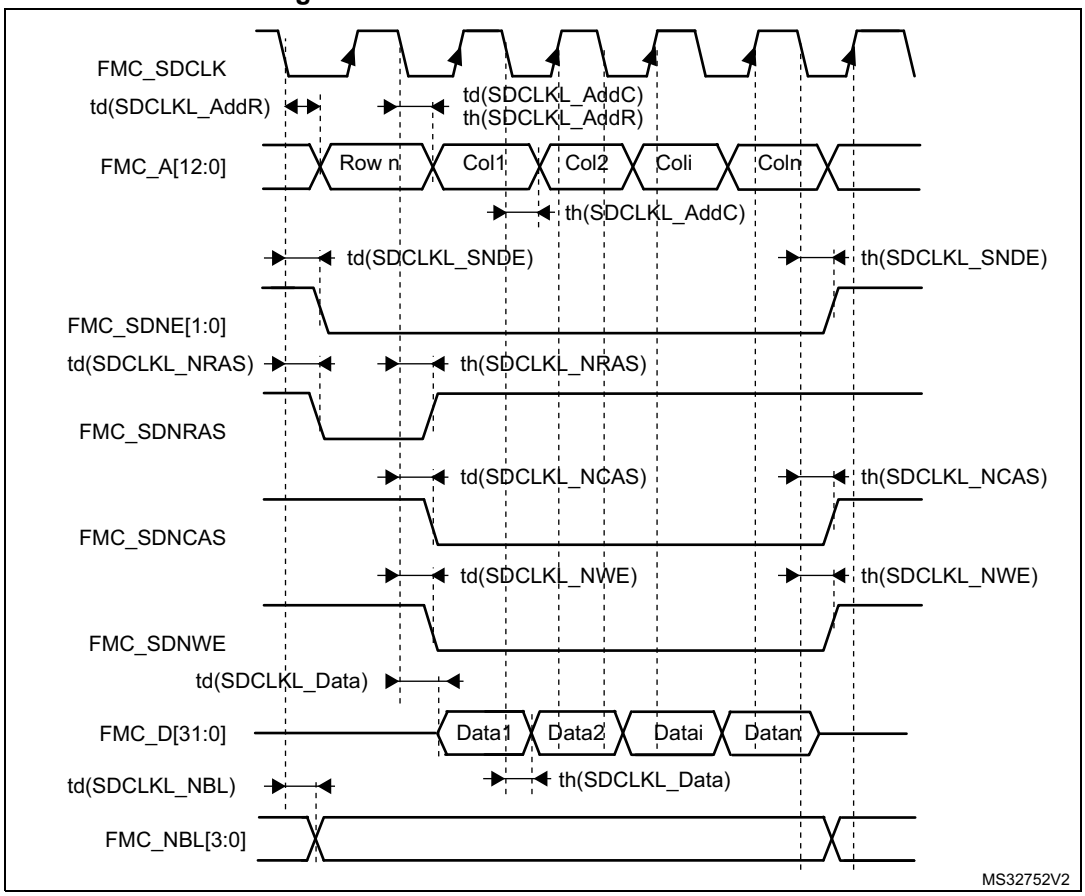


Table 109. SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2Thclk -0.5	2Thclk +0.5	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	1.5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.

Table 110. LPSDR SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2Thclk -0.5	2Thclk +0.5	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	2	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL- SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL- SDNE)}$	Chip select hold time	0.	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	2	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	2	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

6.3.31 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 111* and *Table 112* for Quad-SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 111. Quad-SPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V≤V_{DD}<3.6 V CL=20 pF	-	-	108	MHz
		1.71 V<V_{DD}<3.6 V CL=15 pF	-	-	100	

Table 111. Quad-SPI characteristics (continued)in SDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	ns
tw(CKL)			t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	
ts(IN)	Data input setup time	2.7 V<V_{DD}<3.6 V	2	-	-	
		1.71 V<V_{DD}<3.6 V	2	-	-	
th(IN)	Data input hold time	2.7 V<V_{DD}<3.6 V	1	-	-	
		1.71 V<V_{DD}<3.6 V	2	-	-	
tv(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	1.5	2.5	
		1.71 V<V_{DD}<3.6 V	-	1.5	3	
th(OUT)	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results.

Table 112. Quad-SPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	80	MHz
		1.8 V<V_{DD}<3.6 V CL=15 pF	-	-	80	
		1.71 V<V_{DD}<3.6 V CL=10 pF	-	-	80	
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	ns
tw(CKL)			t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	
ts(IN), tsf(IN)	Data input setup time	2.7 V<V_{DD}<3.6 V	2	-	-	
		1.71 V<V_{DD}<2 V	1.5	-	-	
thr(IN), thf(IN)	Data input hold time	2.7 V<V_{DD}<3.6 V	1.25	-	-	
		1.71 V<V_{DD}<2 V	1.75	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	9.5	11.5	
		1.71 V<V_{DD}<3.6 V DHHC=0	-	9.5	12.25	
		DHHC=1 Pres=1, 2...	-	Thclk/2 +2	Thclk/2 +2.5	
thr(OUT), thf(OUT)	Data output hold time	DHHC=0	5.5	-	-	
		DHHC=1 Pres=1, 2...	Thclk/2 +0.75	-	-	

1. Guaranteed by characterization results.

Figure 75. Quad-SPI timing diagram - SDR mode

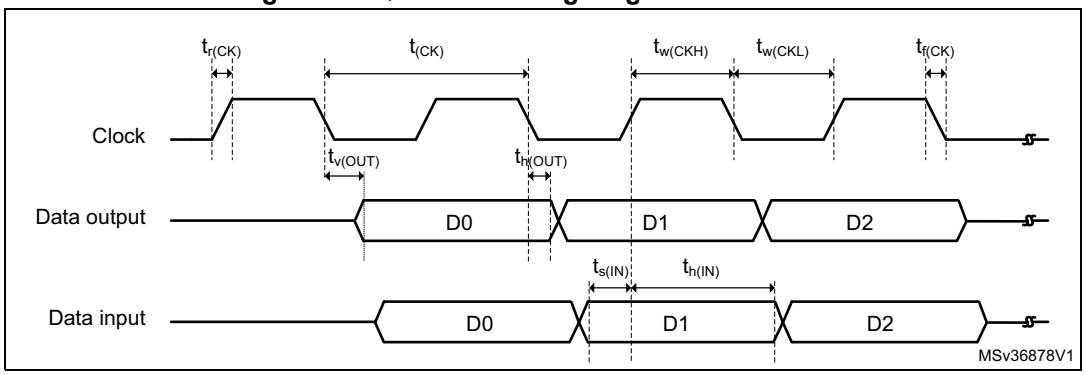
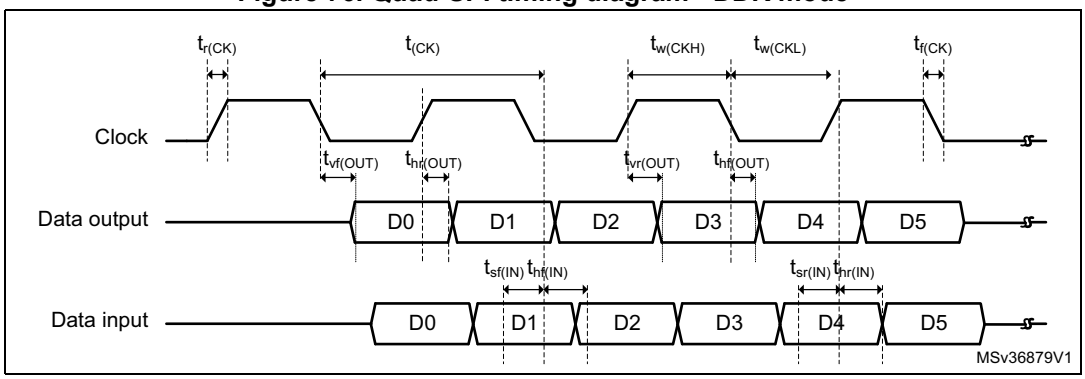


Figure 76. Quad-SPI timing diagram - DDR mode



6.3.32 SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 113* for the SDIO/MMC interface are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output characteristics.

Figure 77. SDIO high-speed mode

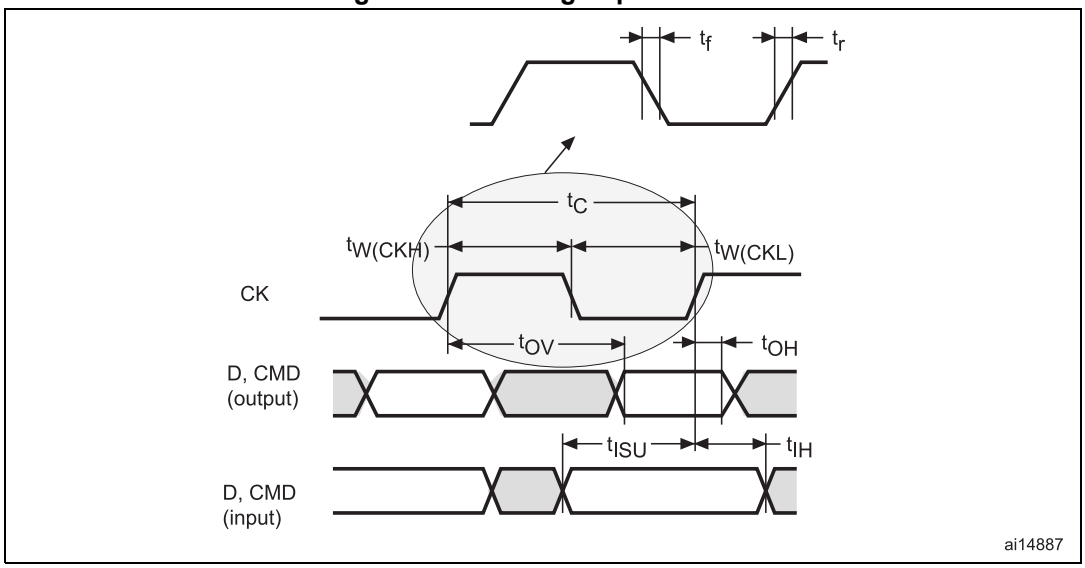


Figure 78. SD default mode

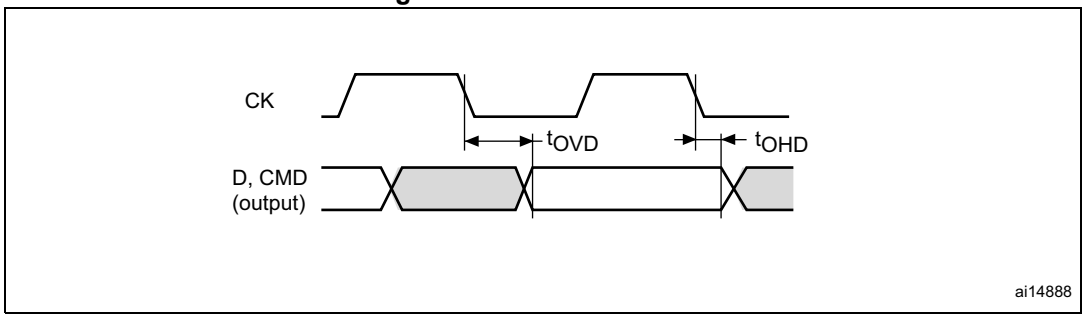


Table 113. Dynamic characteristics: SD / MMC characteristics, V_{DD}=2.7V to 3.6V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	9	10	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	9	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	2	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	2	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	11	12	ns
t_{OH}	Output hold time HS	fpp =50 MHz	9	-	-	

Table 113. Dynamic characteristics: SD / MMC characteristics, V_{DD}=2.7V to 3.6V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp =25 MHz	2	-	-	ns
t_{IHD}	Input hold time SD	fpp =25 MHz	2	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =25 MHz	-	2	2.5	ns
t_{OHD}	Output hold default time SD	fpp =25 MHz	0.5	-	-	

1. Guaranteed by characterization results,.

Table 114. Dynamic characteristics: eMMC characteristics, V_{DD}=1.71V to 1.9V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	1	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	3.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	12	14	ns
t_{OH}	Output hold time HS	fpp =50 MHz	10.5	-	-	

1. Guaranteed by characterization results.
2. C_{load} = 20 pF.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 Device marking

Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

7.2 LQFP64 package information (5W)

This LQFP is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 79. LQFP64 - Outline(15)

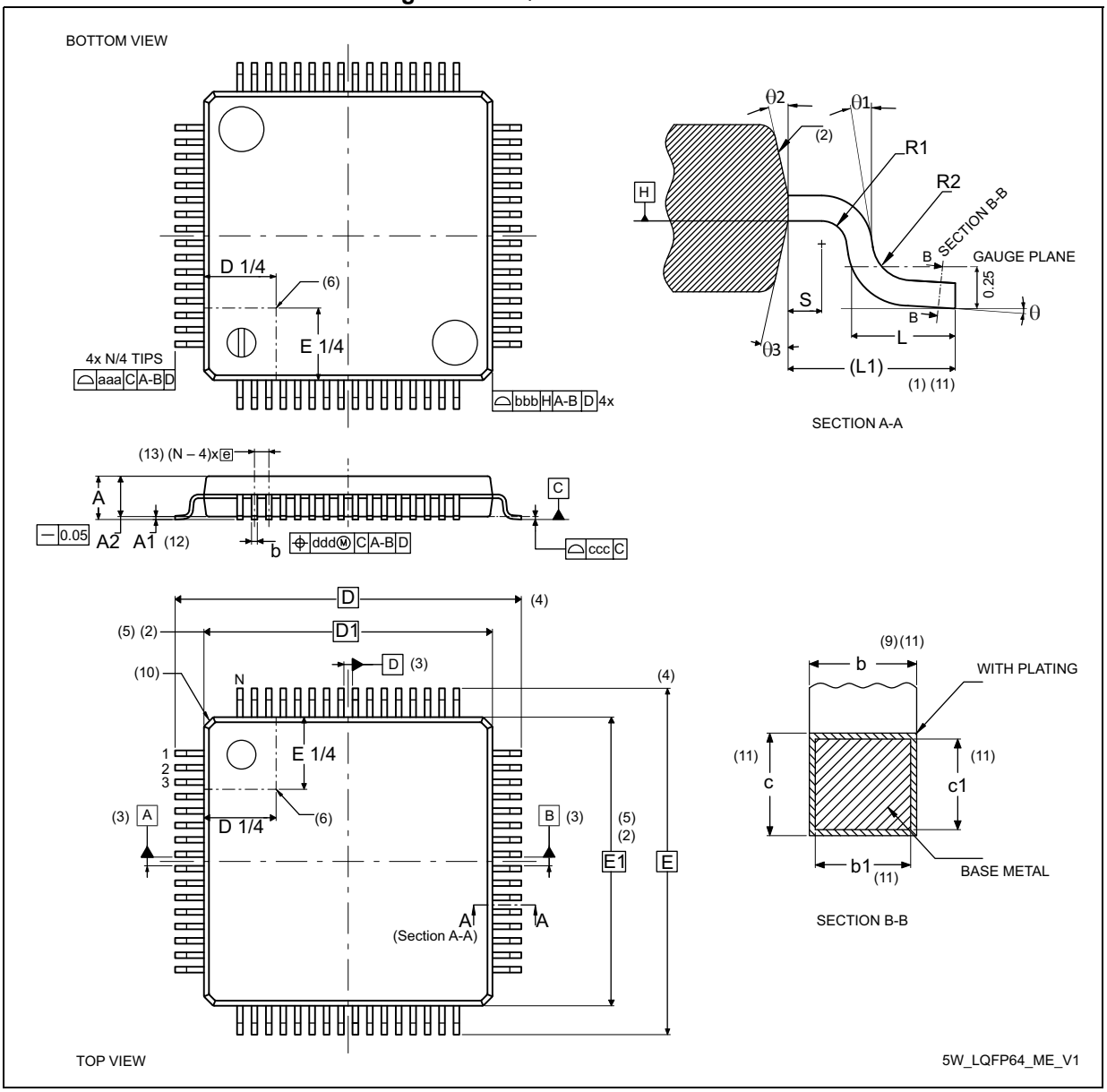


Table 115. LQFP64 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	12.00 BSC			0.4724 BSC		
D1[2][5]	10.00 BSC			0.3937 BSC		
E[4]	12.00 BSC			0.4724 BSC		
E1[2][5]	10.00 BSC			0.3937 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	64					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

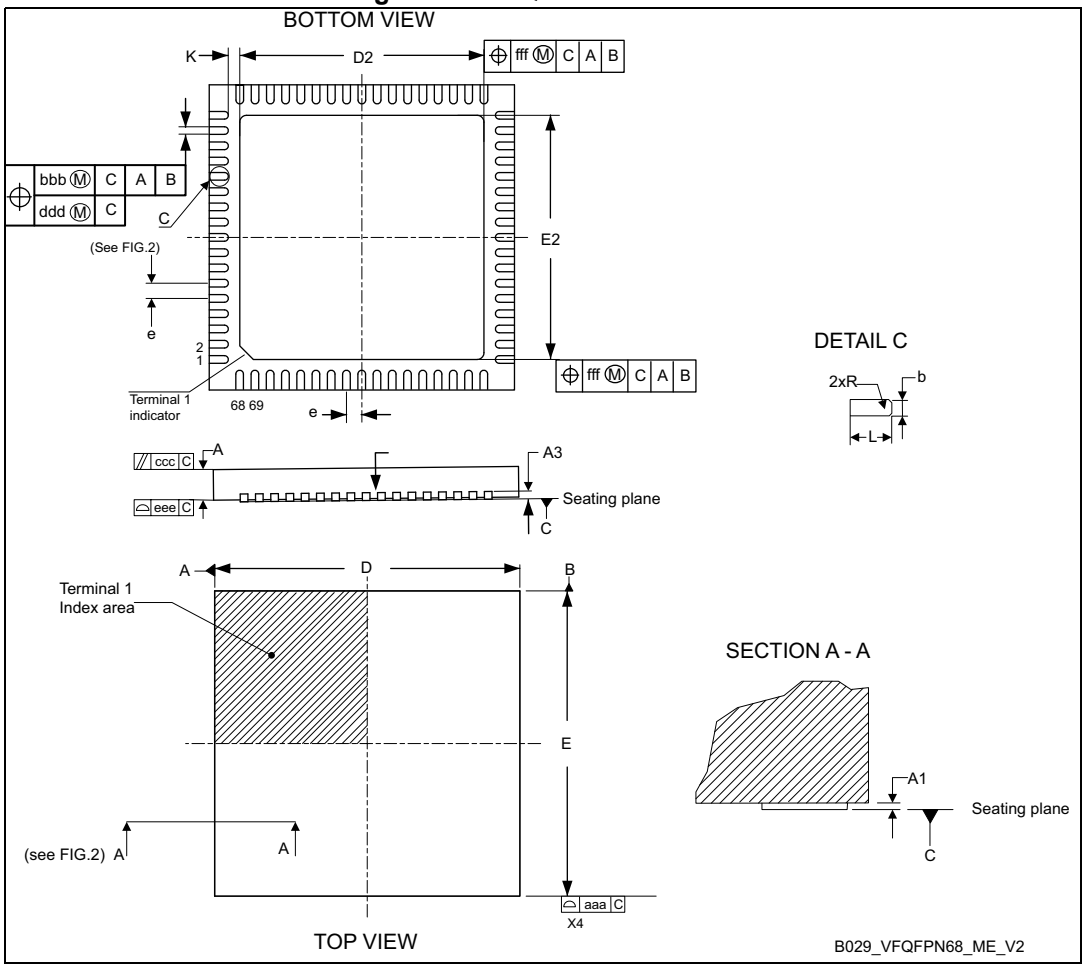
Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

7.3 VFQFPN68 package information (B029)

This VFQFPN is a 68 pins, 8 x 8 mm, 0.4 mm pitch, very thin fine pitch quad flat package.

Figure 80. VFQFPN68 - Outline



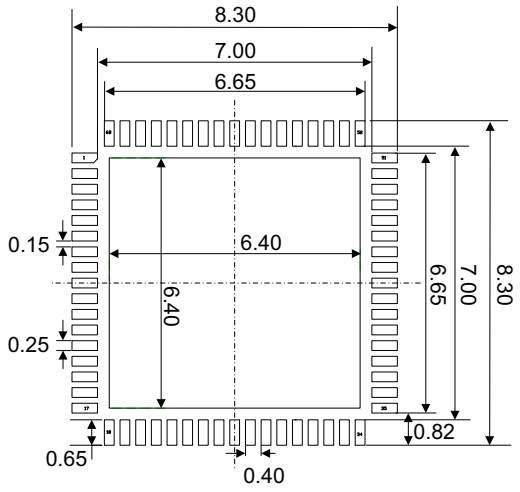
1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Packages No lead. Sawed version. Very thin profile: 0.80 < A ≤ 1.00mm.
2. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

Table 116. VFQFPN68 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	-	0.05	0	-	0.0020
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
D	8.00 BSC			0.3150 BSC		
D2	6.30	6.40	6.50	0.2480	0.2520	0.2559
E	8.00 BSC			0.3150 BSC		
E2	6.30	6.40	6.50	0.2480	0.2520	0.2559
e	0.40 BSC			0.0157 BSC		
L	0.45	-	0.65	0.0177	-	0.0256
R	0.07	-	-	0.0028	-	-
aaa	0.10			0.0039		
bbb	0.07			0.0028		
ccc	0.10			0.0039		
ddd	0.05			0.0020		
eee	0.08			0.0031		
fff	0.10			0.0039		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 81. VFQFPN68 - Footprint example

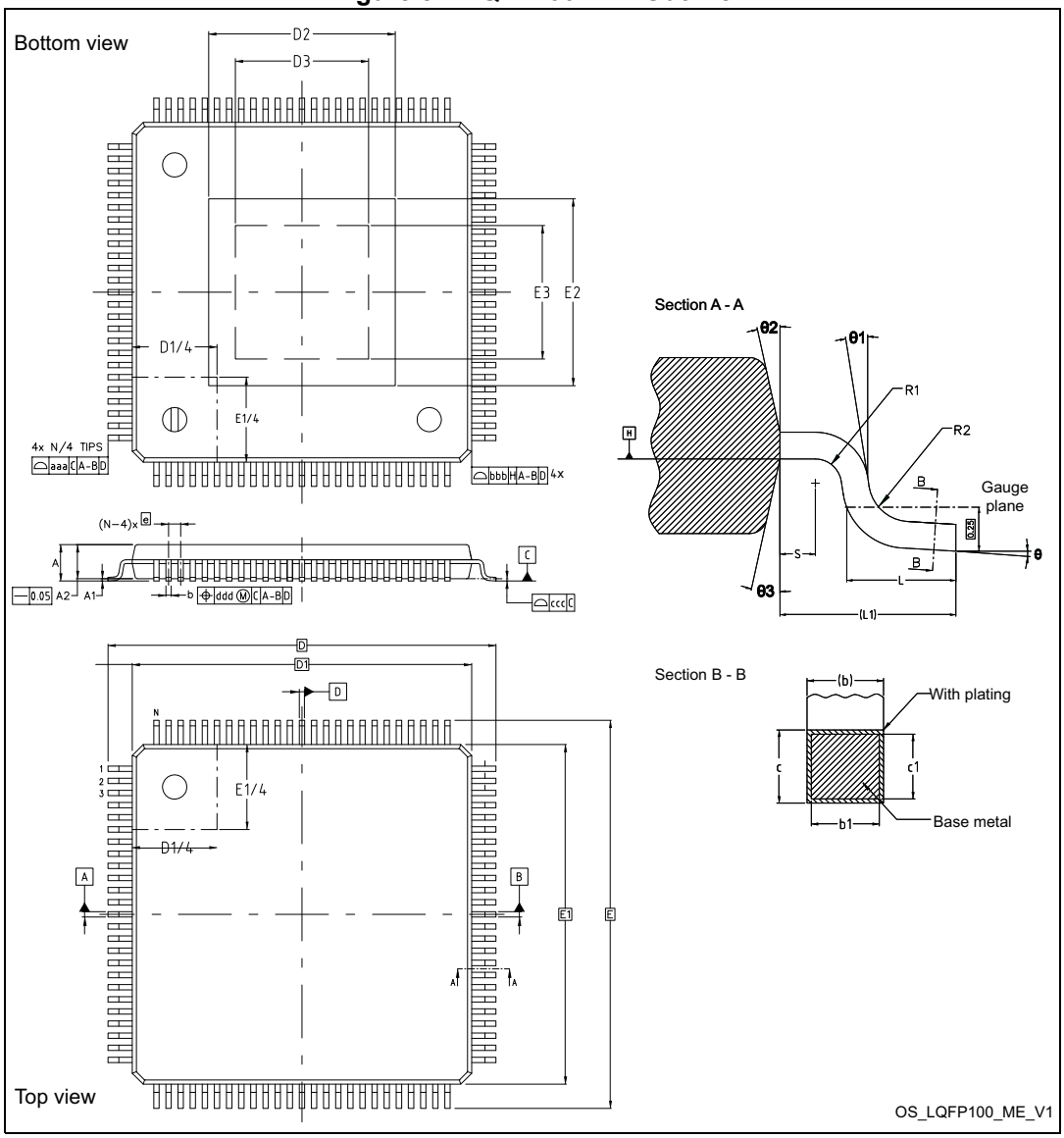


1. Dimensions are expressed in millimeters.

7.4 LQFP100-EP package information (OS_A)

This LQFP is a 100-pin, 14 x 14 mm, low-profile quad flat package with an exposed pad (EP) measuring 5.5 x 5.5 mm.

Figure 82. LQFP100-EP - Outline



1. The drawing is not to scale.

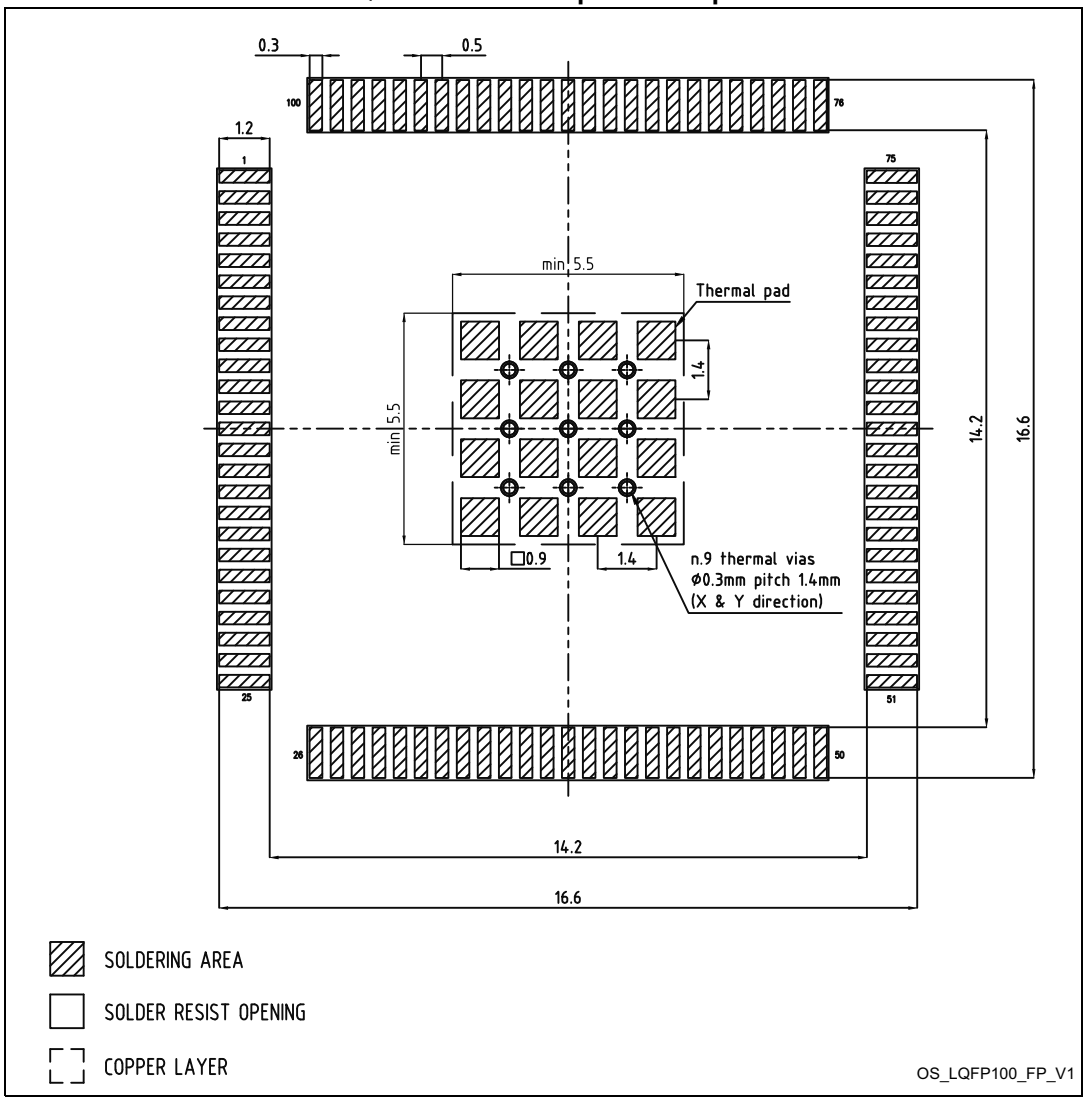
Table 117. LQFP100-EP - Mechanical data

Symbol[1]	Millimeters			Inches[2]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
A[3]	-	-	1.60	-	-	0.0630
A1[4]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[5][6]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[6]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[6]	0.09	-	0.20	0.0035	-	0.0079
c1[6]	0.09	-	0.16	0.0035	-	0.0063
D[7][8]	16.00 BSC			0.6299 BSC		
D1[8][9][10]	14.00 BSC			0.5512 BSC		
D2[11]	-	-	5.55	-	-	0.2185
D3[12]	4.65	-	-	0.1831	-	-
e[8]	0.50 BSC			0.0197 BSC		
E[7][8]	16.00 BSC			0.6299 BSC		
E1[8][9][10]	14.00 BSC			0.5512 BSC		
E2[11]	-	-	5.55	-	-	0.2185
E3[12]	4.65	-	-	0.1831	-	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	100					
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[14]	0.20			0.0079		
bbb[14]	0.20			0.0079		
ccc[14]	0.08			0.0031		
ddd[14]	0.08			0.0031		

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. Values in inches are converted from millimeters and rounded to four decimal digits, except for the θ values, which are provided in degrees.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.

4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
6. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
7. To be determined at seating datum plane C.
8. BSC stands for basic dimensions. It corresponds to the nominal value and has no tolerance.
9. Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
10. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
11. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located. It includes all metal protrusions from exposed pad itself.
12. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
13. N represents the total number of pins on the QFP.
14. Tolerance of form and position.

LQFP100-EP - Footprint example



7.5 LQFP144 package information (1A)

This LQFP is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 83. LQFP144 - Outline(15)

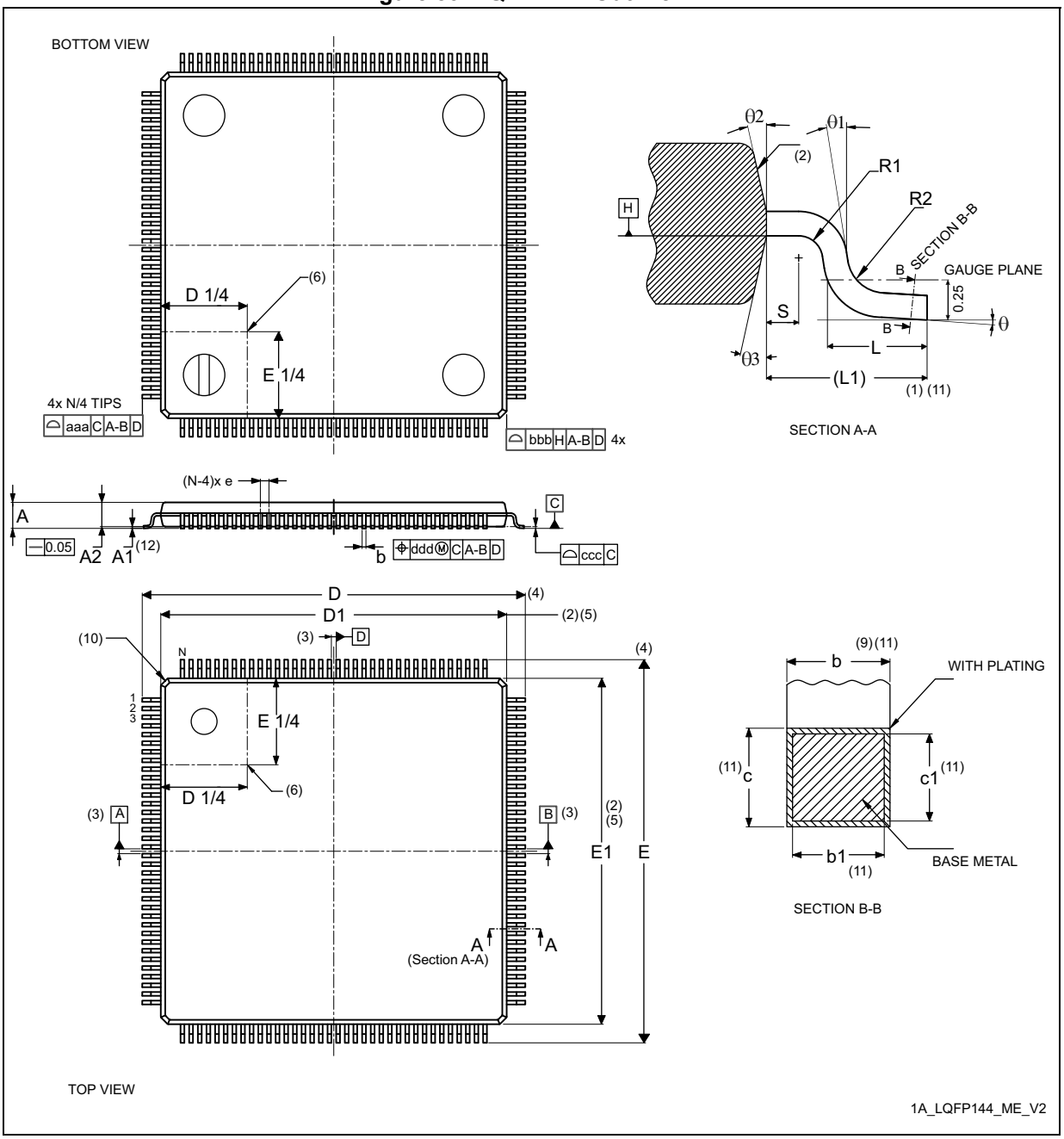


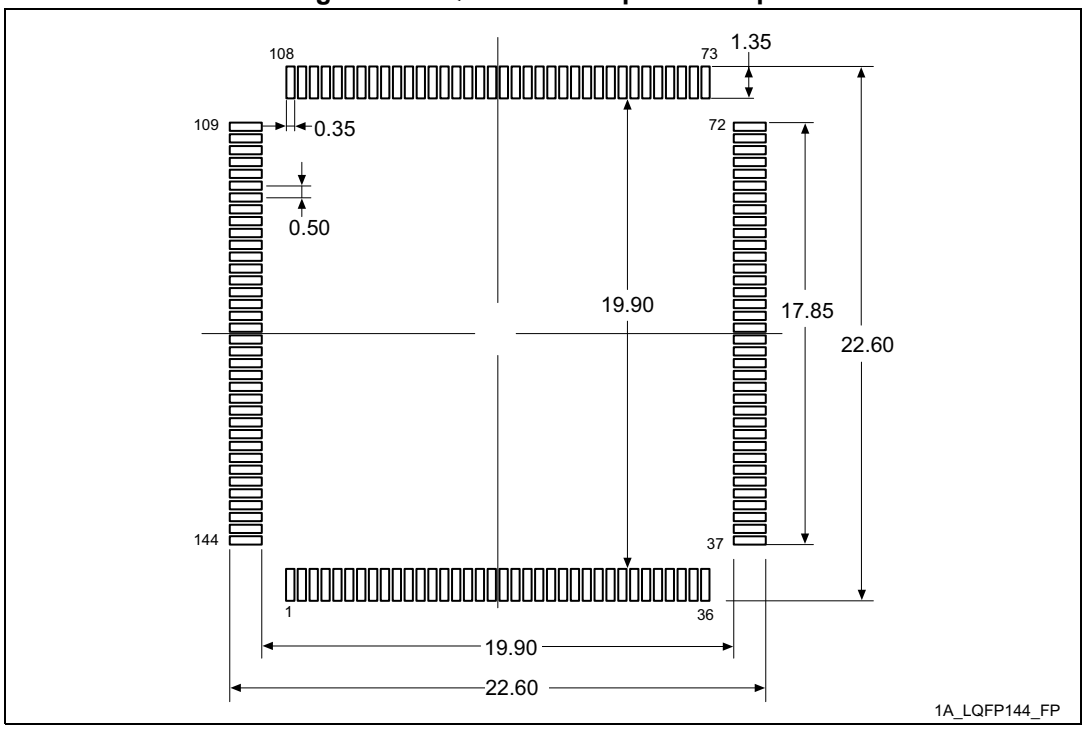
Table 118. LQFP144 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	22.00 BSC			0.8661 BSC		
D1[2][5]	20.00 BSC			0.7874 BSC		
E[4]	22.00 BSC			0.8661 BSC		
E1[2][5]	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	144					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at the seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion is allowed inwards the leads.
9. Dimension b does not include a dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. The dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. The exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead that is between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. N is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to four decimal digits.
15. Drawing is not to scale.

Figure 84. LQFP144 - Footprint example



1. Dimensions are expressed in millimeters.

7.6 LQFP176 package information (1T)

This LQFP is a 176-pin, 24 x 24 mm, 0.5 mm pitch, low profile quad flat package.

Note: See list of notes in the notes section.

Figure 85. LQFP176 - Outline(15)

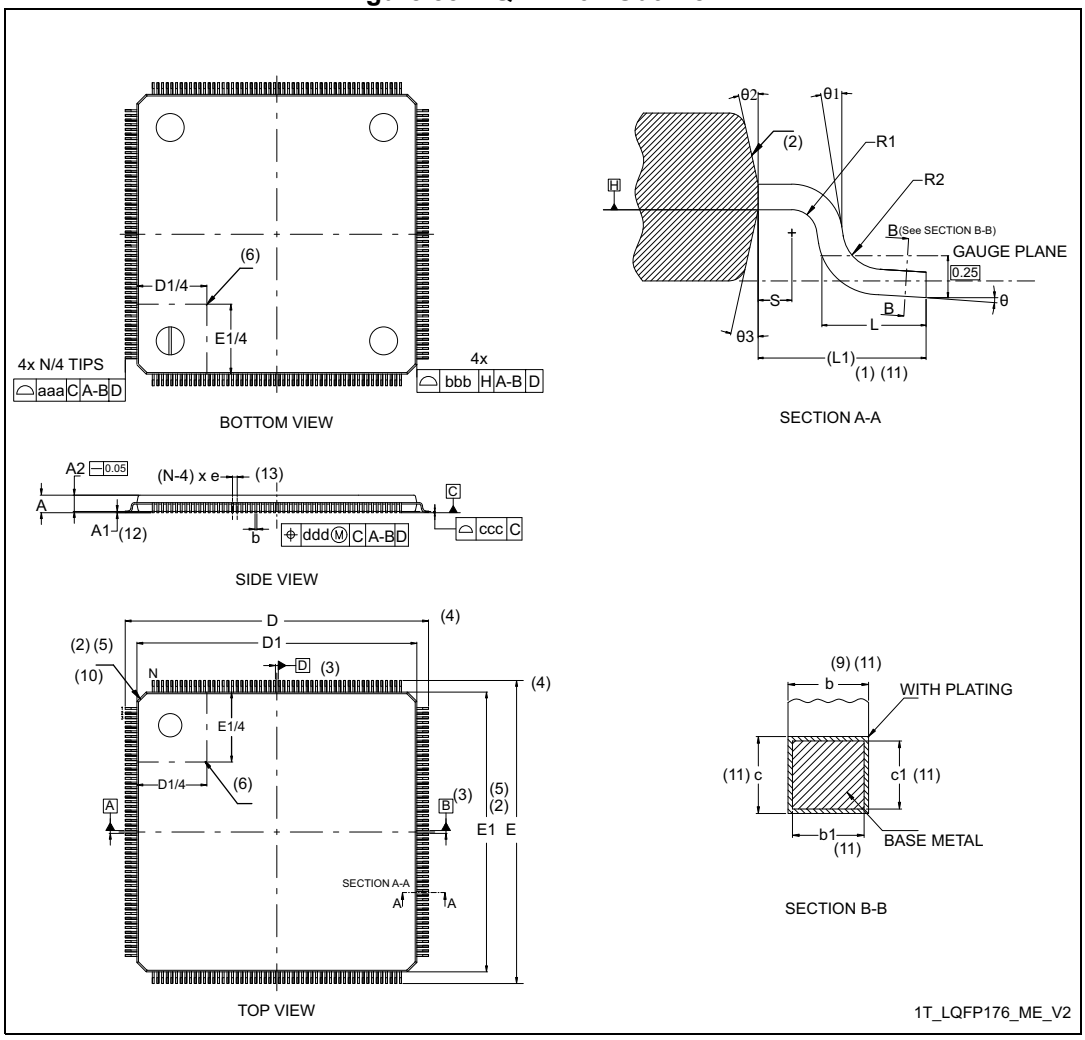


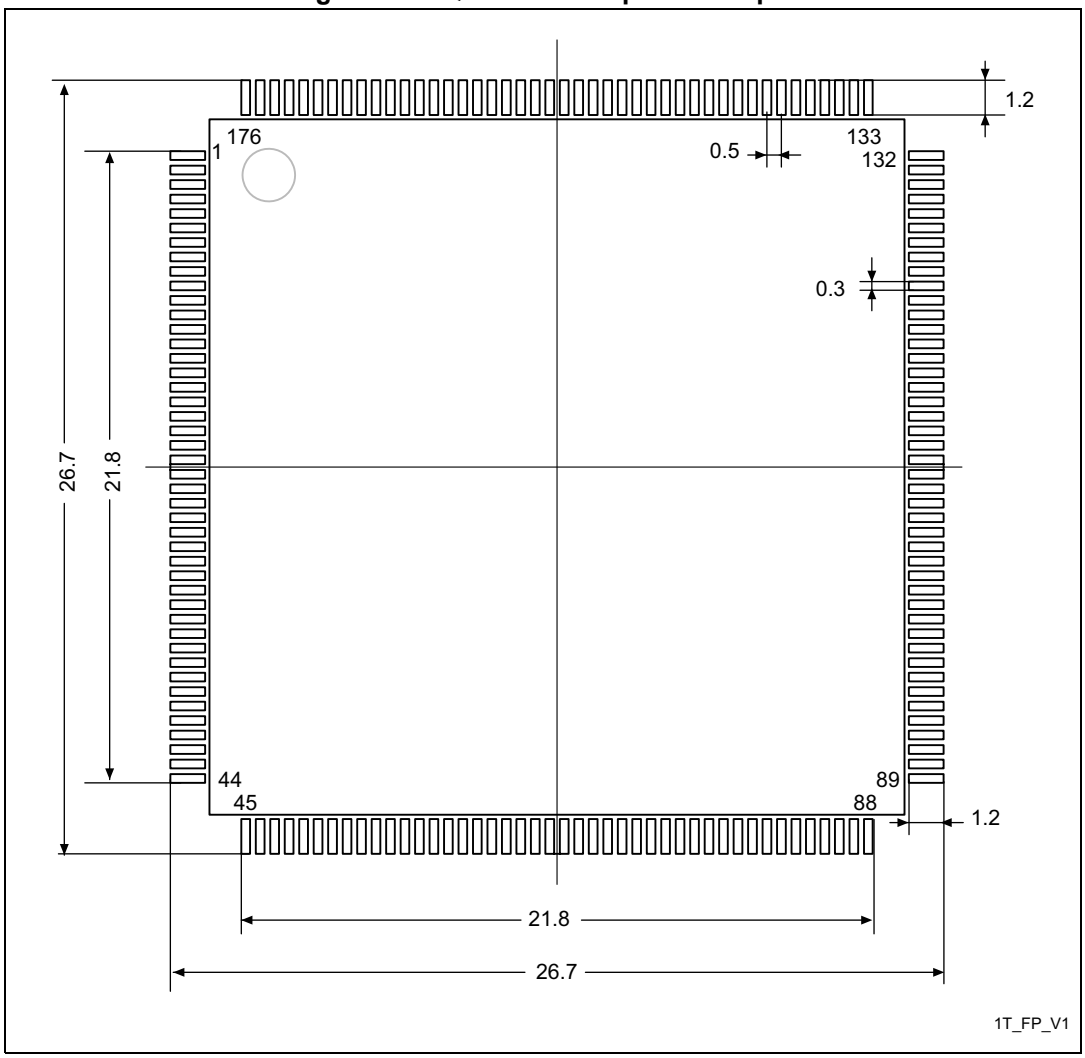
Table 119. LQFP176 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1[12]	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b[9][11]	0.170	0.220	0.270	0.0067	0.0087	0.0106
b1[11]	0.170	0.200	0.230	0.0067	0.0079	0.0091
c[11]	0.090	-	0.200	0.0035	-	0.0079
c1[11]	0.090	-	0.160	0.0035	-	0.063
D[4]	26.000			1.0236		
D1[2][5]	24.000			0.9449		
E[4]	26.000			0.0197		
E1[2][5]	24.000			0.9449		
e	0.500			0.1970		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1[1][11]	1			0.0394 REF		
N[13]	176					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.080	-	-	0.0031	-	-
R2	0.080	-	0.200	0.0031	-	0.0079
S	0.200	-	-	0.0079	-	-
aaa[1]	0.200			0.0079		
bbb[1]	0.200			0.0079		
ccc[1]	0.080			0.0031		
ddd[1]	0.080			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at the seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion is allowed inwards the leads.
9. Dimension b does not include a dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. The dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. The exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead that is between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. N is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to four decimal digits.
15. Drawing is not to scale.

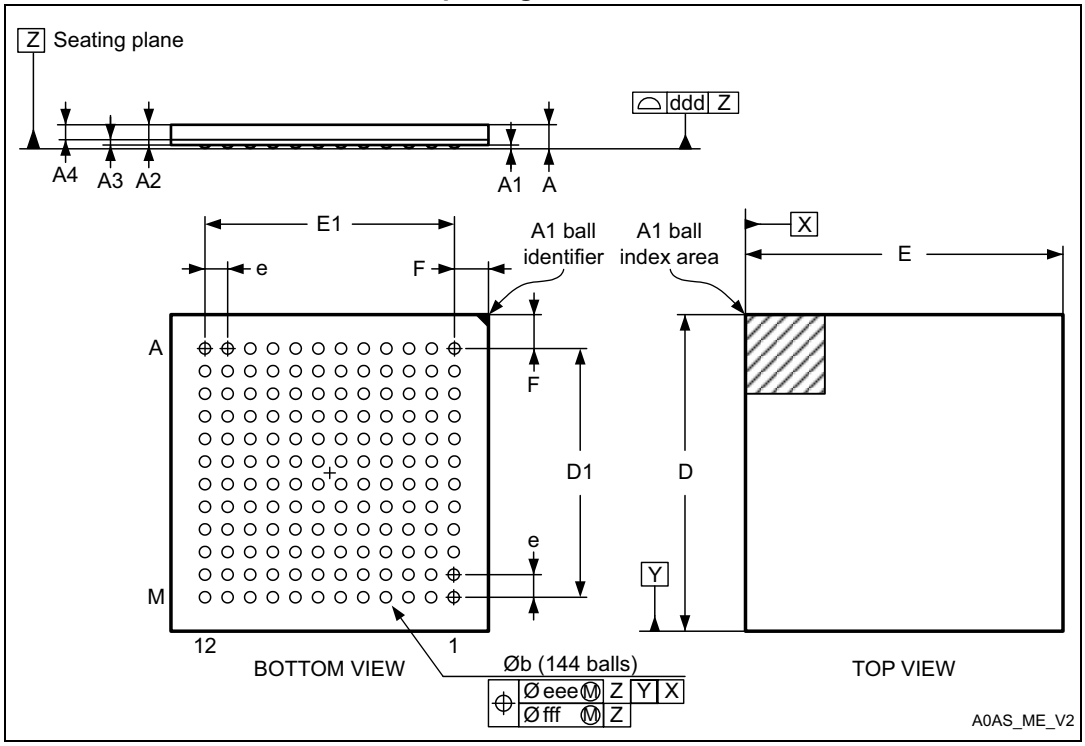
Figure 86. LQFP176 - Footprint example



1. Dimensions are expressed in millimeters.

7.7 UFBGA144 package information (A0AS)

Figure 87. UFBGA - 144 balls, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 120. UFBGA - 144 balls, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.320	0.0091	0.0110	0.0126
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

Table 120. UFBGA - 144 balls, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 88. UFBGA - 144 balls, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

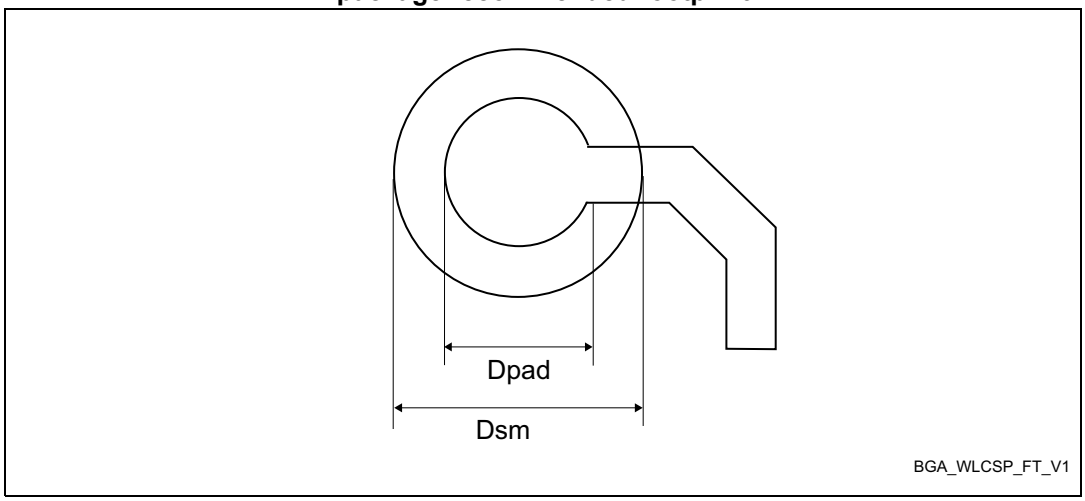


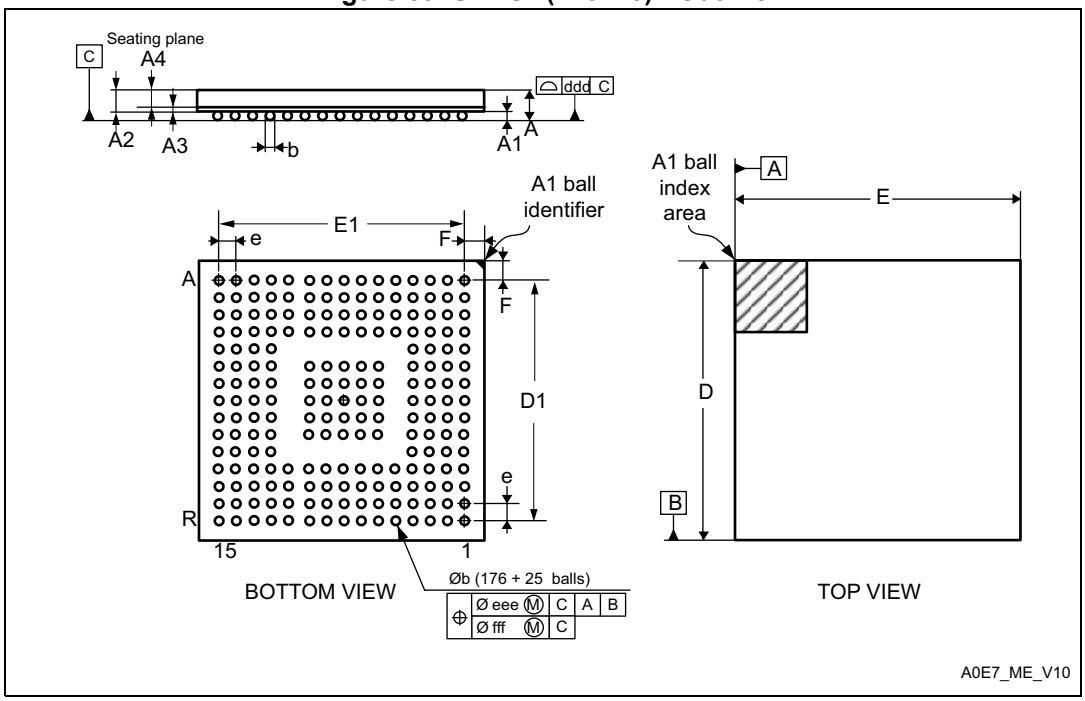
Table 121. UFBGA144 recommended PCB design rules (0.50 mm pitch BGA)

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

7.8 UFBGA(176+25) package information (A0E7)

This UFBGA is a 176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package.

Figure 89. UFBGA(176+25) - Outline



1. Drawing is not to scale.

Table 122. UFBGA(176+25) - Mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
F	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 122. UFBGA(176+25) - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 90. UFBGA(176+25) - Footprint example

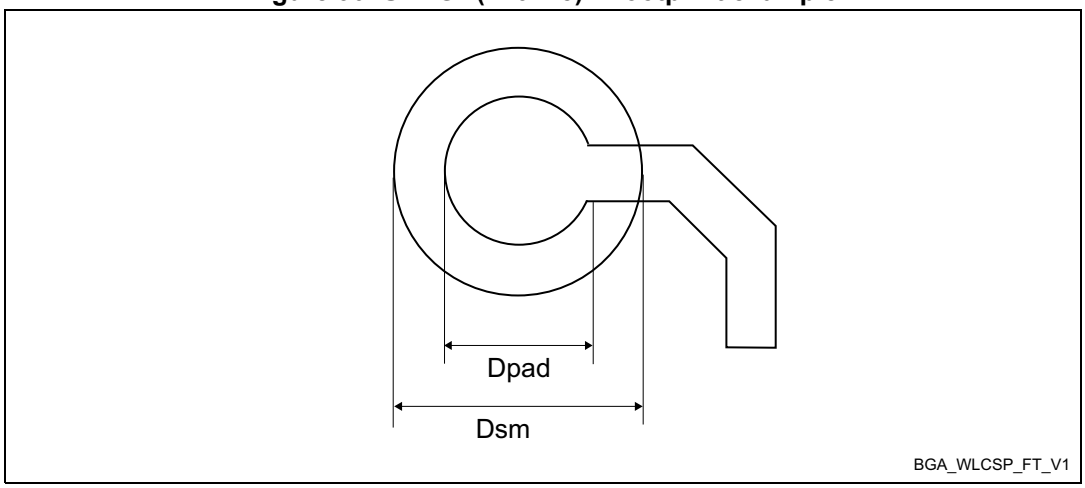


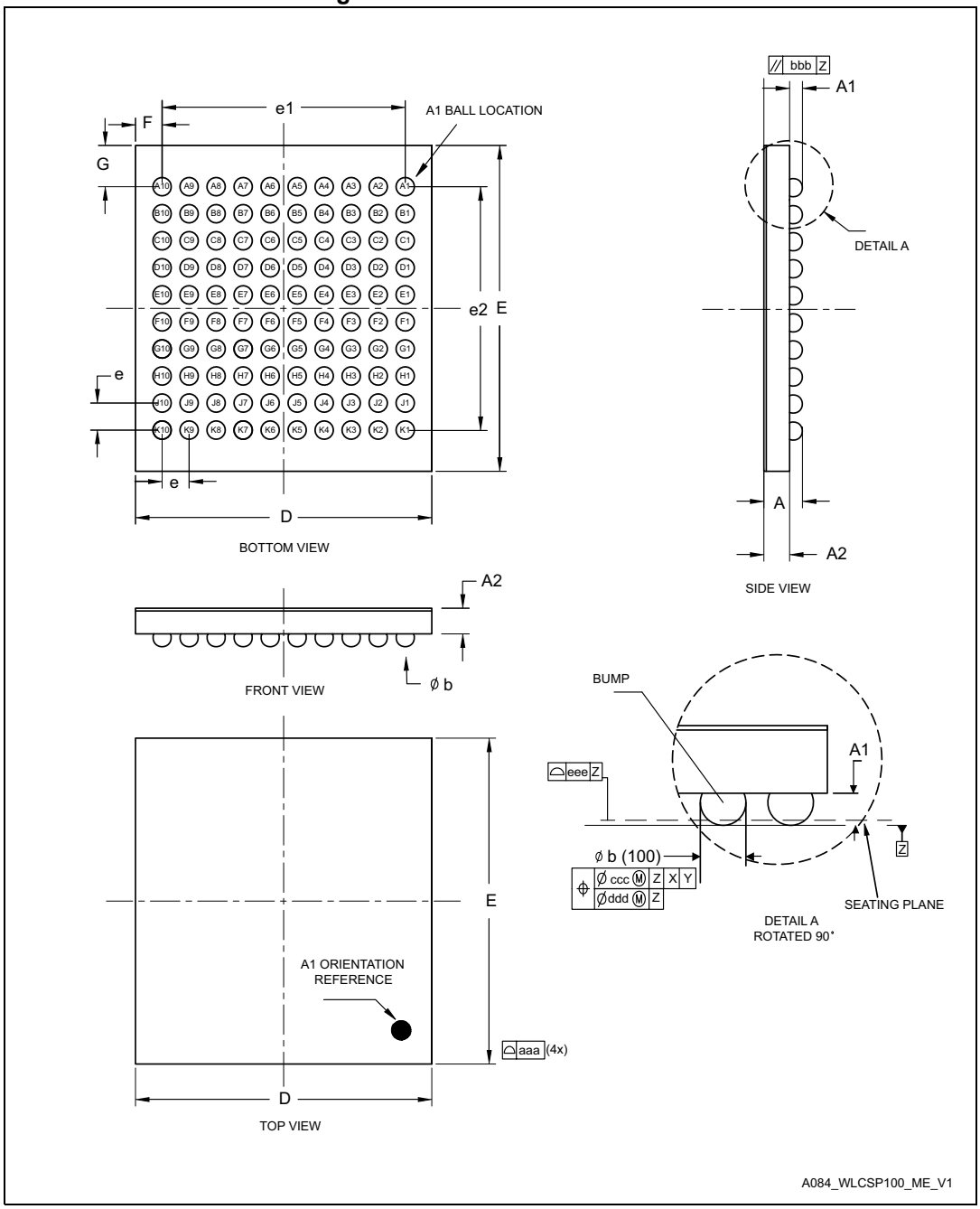
Table 123. UFBGA(176+25) - Example of PCB design rules (0.65 mm pitch BGA)

Dimension	Values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

7.9 WLCSP100 package information (A084)

This WLCSP is a 100-ball, 4.341x4.775 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 91. WLCSP100 - Outline



1. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
2. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
3. Bump position designation per JESD 95-1, SPP-010.

Table 124. WLCSP100 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2[2]	-	0.380	-	-	0.0150	-
A3	-	0.025[3]	-	-	0.0010	-
b	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	4.306	4.341	4.376	0.1695	0.1709	0.1723
E	4.740	4.775	4.810	0.1866	0.1880	0.1894
e	-	0.400	-	-	0.0157	-
e1	-	3.600	-	-	0.1417	-
e2	-	3.600	-	-	0.1417	-
F[4]	-	0.3705	-	-	0.0146	-
G[4]	-	0.5875	-	-	0.0231	-
N	100					
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to the 4rd decimal place.
2. Back side coating.
3. Nominal dimension rounded to the 3rd decimal place results from process capability.
4. Calculated dimensions are rounded to 3rd decimal place.

Figure 92. WLCSP100 - Recommended footprint

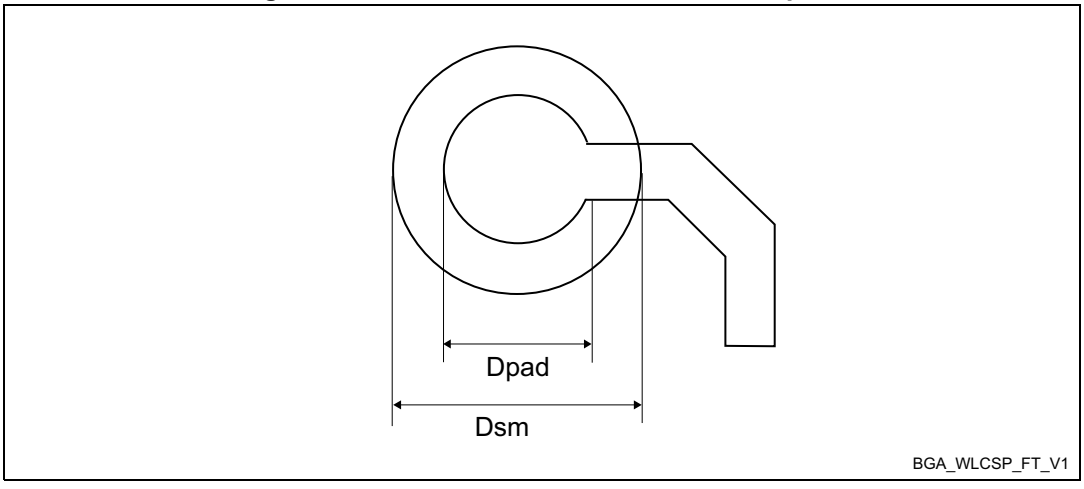


Table 125. WLCSP100 - Recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.250 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.325 mm
Stencil thickness	0.100 mm

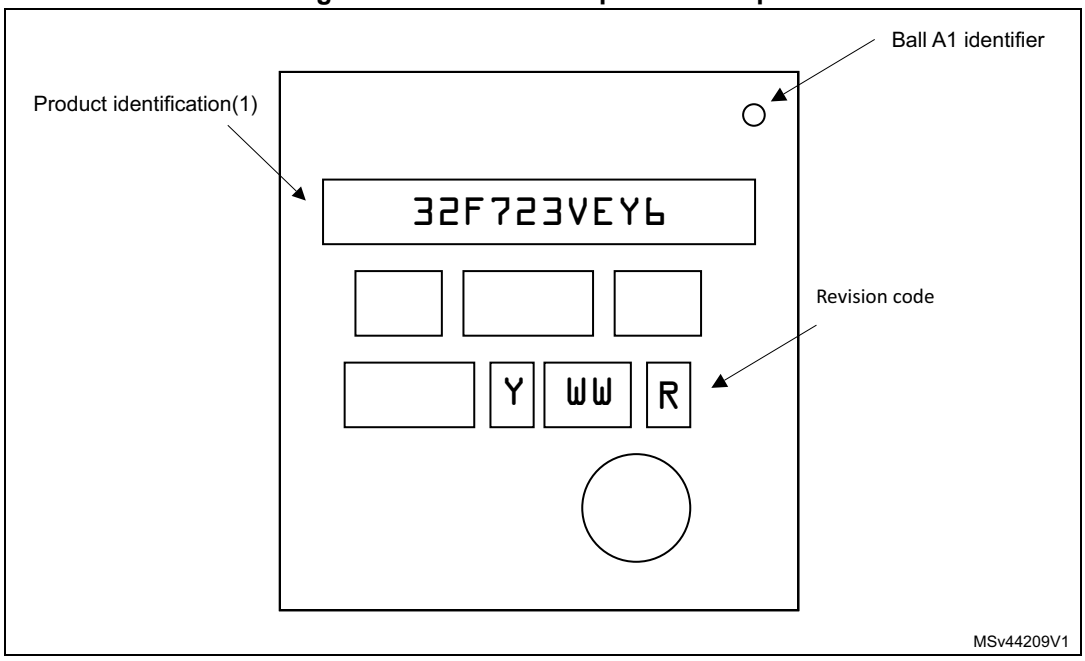
WLCSP100 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 93. WLCSP100 top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.10 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 126. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	48.5	°C/W
	Thermal resistance junction-ambient VFQFPN68 - 8 × 8 mm / 0.5 mm pitch	24.6	
	Thermal resistance junction-ambient LQFP100 - 14× 14 mm / 0.5 mm pitch	47.1	
	Thermal resistance junction-ambient WLCSP100 - 0.4 mm pitch	35.85	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	45.6	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	43.9	
	Thermal resistance junction-ambient UFBGA144 - 7 × 7 mm / 0.5 mm pitch	42	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.65 mm pitch	41.2	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

8 Ordering information

Table 127. Ordering information scheme

Example: STM32 F 722 V C T 6 xxx

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

722 = STM32F722xx, no OTG PHY HS
723 = STM32F723xx, with OTG PHY HS

Pin count

R = 64 pins/68 pins

V = 100 pins

Z = 144 pins

I = 176 pins

Flash memory size

C = 256 Kbytes of Flash memory

E = 512 Kbytes of Flash memory

Package

T = LQFP

V = VFQFPN

K = UFBGA (10 x 10 mm)

I = UFBGA (7 x 7 mm)

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7(1) = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts

TR = tape and reel

1. Range -40° to +105°C is not available for WLCSP packages.

For a list of available options (such as speed or package) or for further information on any aspect of this device, contact the nearest ST sales office.

Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.
- The over-drive mode is not supported.

A.1 Operating conditions

Table 128. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states (1)(2)	I/O operation	Possible Flash memory operations
V_{DD} =1.7 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz	180 MHz with 8 wait states and over-drive OFF	– No I/O compensation	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from the Flash memory since the ART accelerator or L1-cache is used to achieve a performance equivalent to 0-wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.15.1: Internal reset ON*).

9 Important security notice

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10 Revision history

Table 129. Document revision history

Date	Revision	Changes
03-Feb-2017	1	Initial release.
30-Mar-2017	2	Updated cover with the maximum SPI speed at 54 Mbit/s. Updated *Figure 14: STM32F732xx LQFP64 pinout*.
01-Jun-2017	3	Updated *Figure 16: STM32F733xx WLCSP100 ballout (with OTG PHY HS)*. Updated note 1 below all the package device marking figures. Updated *Section 1: Introduction*. Updated *Table 60: I/O current injection susceptibility* note by 'injection is not possible'. Updated *Table 67: ADC characteristics* R_{ADC} min at 1.5 kΩ Updated *Figure 45: Recommended NRST pin protection* note about the 0.1uF capacitor. Updated *Table 78: DAC characteristics* R_{LOAD} feature. Updated *Figure 39: ACCHSI versus temperature*.
10-Apr-2018	4	Added *Section 1: Introduction*. Removed memory mapping, transferred in the reference manual (RM0431). Updated *Table 10: STM32F732xx and STM32F733xx pin and ball definition* footnote 5 only for PC14, PC15, PH0, PH1. Updated *Table 125: Package thermal characteristics* thermal values for LQFP packages.
23-Mar-2020	5	Updated *Table 1: Device summary* adding STM32F723VC. Added LQFP100 package for STM32F723xx devices: – Updated *Table 2: STM32F722xx and STM32F723xx features and peripheral counts*. – Updated *Section 2.2: STM32F723xx versus STM32F722xx LQFP100/ LQFP144/ LQFP176 packages*. – Added *Figure 3: Compatible board design for LQFP100 package*. – Added *Figure 17: STM32F723xx LQFP100 pinout*. – Updated *Table 10: STM32F722xx and STM32F723xx pin and ball definition* Added VDDPHYS – Updated *Figure 6: STM32F722xx and STM32F723xx block diagram*. – Updated *Figure 29: STM32F723xx power supply scheme*. – Updated *Table 13: Voltage characteristics* – Updated *Table 16: General operating conditions* Updated *Section 7: Package information*.
04-Apr-2020	6	Updated *Table 53: Flash memory programming* maximum programming voltage (V_{prog}) for 32-bit Flash program operation at 3.6V (instead of 3V).
05-Nov-2020	7	Updated – *Section 2: Description* – *Section 2.1: Full compatibility throughout the family* – Note 1 of *Table 42: HSI oscillator characteristics*
3-Feb-2022	8	Updated *Section 7.7: WLCSP100 package information*

Table 129. Document revision history (continued)

Date	Revision	Changes
27-Jul-2022	9	Updated: – *Table 81: SPI dynamic characteristics* – *Table 101: Synchronous multiplexed NOR/PSRAM read timings* – *Table 103: Synchronous non-multiplexed NOR/PSRAM read timings* – *Table 107: SDRAM read timings* – *Table 108: LPSDR SDRAM read timings* – *Table 111: Quad-SPI characteristics in SDR mode* – *Table 112: Quad-SPI characteristics in DDR mode* – *Table 113: Dynamic characteristics: SD / MMC characteristics, VDD=2.7V to 3.6V* – *Table 114: Dynamic characteristics: eMMC characteristics, VDD=1.71V to 1.9V* – New *Section 9: Important security notice*
02-Nov-2026	10	Added the VQFPN68 package and updated the entire document to reflect this change. Updated: – *Section 7: Package information* – *Figure 16: STM32F723xx VQFPN68 pinout* – *Table 10: STM32F722xx and STM32F723xx pin and ball definition*

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