High Speed, Dual Driver, Comparator, and Load

AD53564

FEATURES

- 1000 MHz toggle rate
- Driver/comparator/active load and dynamic clamp included
- Inhibit mode function
- 100-lead LQFP package with built-in heat sink driver
  - 48 Ω output resistance
  - 800 ps T_R/T_F for a 3 V step
- Comparator: 1.1 ns propagation delay at 3 V
- Load
  - ±40 mA voltage-programmable current range
  - 50 ns settling time to 15 mV

APPLICATIONS

- Automatic test equipment
- Semiconductor test systems
- Board test systems
- Instrumentation and characterization equipment

GENERAL DESCRIPTION

The AD53564 is a complete, high speed, single-chip solution that performs the pin electronic functions of driver, comparator, and active load (DCL) for automated test equipment (ATE) applications. In addition, the driver contains a dynamic clamp function, and the active load contains an integrated Schottky diode bridge.

The driver is a proprietary design that features three active states: data high mode, data low mode, and term mode, as well as an inhibit state. In conjunction with the integrated dynamic clamp, this facilitates the implementation of a high speed, active termination. The output voltage range is −0.5 V to +6.5 V to accommodate a wide variety of test devices.

The dual comparator, with an input range equal to the driver output range, features PECL-compatible outputs. Signal tracking capability is in the range of 3 V/ns.

The active load can be set for up to 40 mA load current. I_{OH}, I_{OL}, and the buffered VCOM are independently adjustable. On-board Schottky diodes provide high speed switching and low capacitance.

FUNCTIONAL BLOCK DIAGRAM (ONE OF TWO CHANNELS IS SHOWN)

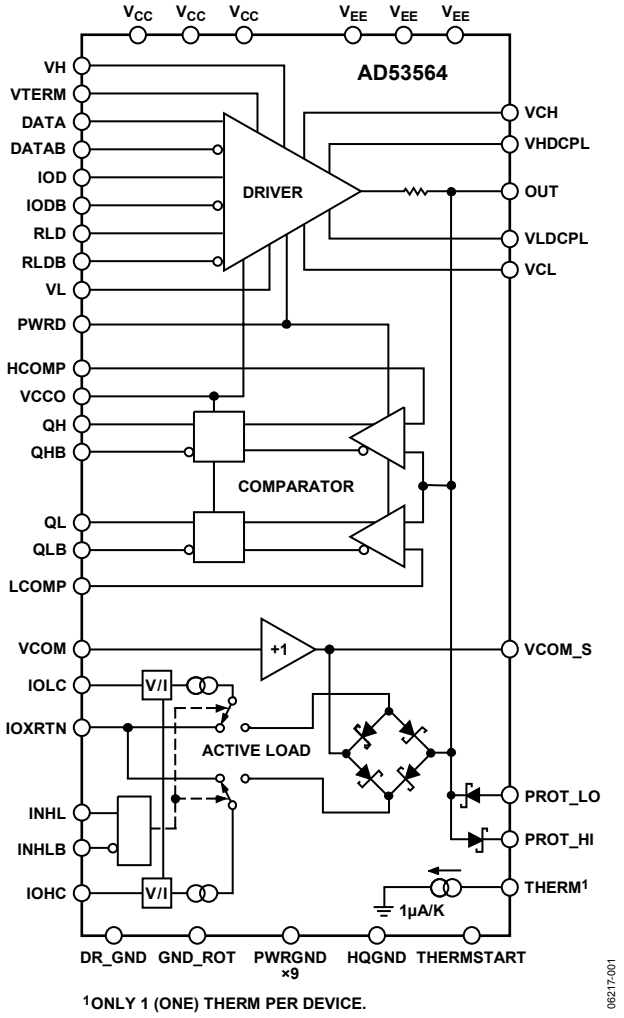


Figure 1.

Also included is an on-board temperature sensor that gives an indication of the silicon surface temperature of the DCL. This information can be used to measure θ_{JC} and θ_{JA} or flag an alarm if proper cooling is lost. Output from the sensor is a current sink that is proportional to absolute temperature. The gain is trimmed to a nominal value of 1 µA/K. As an example, the output current can be sensed by using a 10 kΩ resistor connected from 10 V to the THERM (I_{OUT}) pin. A voltage drop across the resistor will be developed that equals 10 kΩ × 1 µA/K = 10 mV/K = 2.98 V at room temperature.

Rev. Sp0

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REVISION HISTORY

6/06—Revision 0: Initial Version

SPECIFICATIONS

DRIVER[1]

T_J = 85°C ± 5°C, $+V_S$ = 10.5 V ± 1%, $-V_S$ = −4.5 V ± 1%, VCCO = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ[2]	Max	Unit	Specification[3] Performance
DIFFERENTIAL INPUT CHARACTERISTICS (DATA to DATAB, IOD to IODB, RLD to RLDB)						
Voltage Range	Inputs are from the same logic type family	0		3.3	V	N
Differential Voltage with LVPECL Levels	AC tests performed	±400	±600	±1000	mV	P
Bias Current	VIN = 1.5 V, 2.5 V	−250		+250	µA	P
REFERENCE INPUTS						
Bias Currents	Maximum value measured during linearity tests	−50		+50	µA	P
OUTPUT CHARACTERISTICS						
Logic High Range	Data = H, VH = −0.4 V to +6.5 V, VI = −0.5 (V T = 0 V, VH meets driver VH Offset, VH Gain Error, and Linearity Error ABSOLUTE ACCURACY specs below)	−0.4		+6.5	V	P
Logic Low Range	Data = L, VL = −0.5 V to +6.4 V, VH = 6.5 V (VT = 0 V, VL meets VL Offset, VL Gain Error, and Linearity Error ABSOLUTE ACCURACY specs below)	−0.5		+6.4	V	P
Amplitude [VH to VL]	VL = −0.05 V, VH = +0.05 V, VT = 0 V and VL = −0.5 V, VH = +6.5 V, VT = 0 V	0.1		7.0	V	P
ABSOLUTE ACCURACY						
VH Offset	Data = H, VH = 0 V, VL = −0.5 V, VT = +3 V	−50		+50	mV	P
VH Gain Error	Data = H, VH = −0.4 V to +6.5 V, VL = −0.5 V, VT = +3 V	−0.3		+0.3	% of VH	P
Linearity Error	Data = H, VH = −0.4 V to +6.5 V, VL = −0.5 V, VT = +3 V	−5		+5	mV	P
VL Offset	Data = L, VL = 0 V, VH = 6.5 V, VT = 3 V	−50		+50	mV	P
VL Gain Error	Data = L, VL = −0.5 V to +6.4 V, VH = 6.5 V, VT = 3 V	−0.3		+0.3	% of VL	P
Linearity Error	Data = L, VL = −0.5 V to +6.4 V, VH = 6.5 V, VT = 3 V	−5		+5	mV	P
Offset Temperature Coefficient	VL = 0 V, VH = 5 V, VT = 0 V		0.5		mV/°C	N
OUTPUT RESISTANCE						
VH = −0.3 V	VL = −0.5 V, VT = 0 V,	46		50	Ω	N

Parameter	Conditions	Min	Typ[2]	Max	Unit	Specification[3] Performance
	I_{OUT} = +1 mA, +30 mA					
VH = +6.5 V	VL = −0.5 V, VT = 0 V, I_{OUT} = −1 mA, −30 mA	46		50	Ω	P
VL = −0.5 V	VH = +6.5 V, VT = 0 V, I_{OUT} = +1 mA, +30 mA	46		50	Ω	P
VL = +6.4 V	VH = +6.5 V, VT = 0 V, I_{OUT} = −1 mA, −30 mA	46		50	Ω	N
VH = +2.5 V	VL = 0 V, VT = 0 V, I_{OUT} = −30 mA (Trim Point)		47.5		Ω	P
Dynamic Current Limit	C_{BYP} = 39 nF, VH = 6.5 V	100			mA	N
Static Current Limit	Output to −0.5 V, VH = +6.5 V, VL = −0.5 V, VT = 0 V, DATA = H	−120		−60	mA	P
Static Current Limit	Output to 6.5 V, VH = 6.5 V, VL = −0.5 V, VT = 0 V, DATA = L	60		120	mA	P
VTERM						
Voltage Range	Term Mode, VTERM = −0.3 V to +6.3 V, VL = 0 V, VH = 3V (VTERM meets VTERM Offset, VTERM Gain Error, and VTERM Linearity Error specs below)	−0.3		+6.3	V	P
VTERM Offset	Term Mode, VTERM = 0 V, VL = 0 V, VH = 3 V	−50		+50	mV	P
VTERM Gain Error	Term Mode, VTERM = −0.3 V to +6.3 V, VL = 0 V, VH = 3 V	−0.3		+0.3	% of VSET	P
VTERM Linearity Error[4]	Term Mode, VTERM = −0.3 V to +6.3 V, VL = 0 V, VH = 3 V	−5		+5	mV	P
Offset Temperature Coefficient	VTERM = 0 V, VL = 0 V, VH = 3 V		0.5		mV/°C	N
Output Resistance DC	I_{OUT} = +30 mA, −1 mA, VTERM = −0.3 V, VH = 3 V, VL = 0 V	46		50	Ω	N
	I_{OUT} = −30 mA, +1 mA, VTERM = 6.3 V, VH = 3 V, VL = 0 V	46		50	Ω	N
	I_{OUT} = ±30 mA, ±1 mA, VTERM = 2.5 V, VH = 3 V, VL = 0 V	46		50	Ω	P
PSRR, Drive, or Term Mode	+VS , −VS ± 1%		17.8		mV/V	N
Static Current Limit	Output to −0.3 V, VTERM = +6.3 V	−120		−60	mA	P
Static Current Limit	Output to +6.3 V, VTERM = −0.3 V	60		120	mA	P
DYNAMIC PERFORMANCE, DRIVE (VH and VL)						
Propagation Delay Time	Measured at 50%, VL = 0 V, VH = 3 V, into 500 Ω	1.25	1.4	1.55	ns	P
Propagation Delay T.C.	Measured at 50%, VL = 0 V, VH = 3 V, into 500		2		ps/°C	N

Parameter	Conditions	Min	Typ[2]	Max	Unit	Specification[3] Performance
	Ω					
Delay Matching, Edge-to-Edge	Measured at 50%, VL = 0 V, VH = 3 V, into 500 Ω			200	ps	P
RISE AND FALL TIMES						
200 mV Swing	Measured 20% to 80%, VL = −0.1 V, VH = +0.1 V, into 50 Ω		0.25		ns	N
1 V Swing	Measured 20% to 80%, VL = 0 V, VH = 1 V, into 50 Ω		0.3		ns	N
3 V Swing	Measured 10% to 90%, VL = 0 V, VH = 3 V, into 50 Ω		0.8		ns	N
3 V Swing	Measured 10% to 90%, VL = 0 V, VH = 3 V, into 500 Ω		0.8		ns	N
3 V Swing	Measured 20% to 80%, VL = 0 V, VH = 3 V, into 500 Ω	0.450	0.560	0.670	ns	P
5 V Swing	Measured 10% to 90%, VL = 0 V, VH = 5 V, into 500 Ω		1.2	1.5	ns	N
RISE AND FALL TIME TEMPERATURE COEFFICIENT						
1 V Swing	Same as 1V Rise and Fall Time conditions		±2		ps/°C	N
3 V Swing	Same as 3V Rise and Fall Time conditions		±2		ps/°C	N
5 V Swing	Same as 5V Rise and Fall Time conditions		±4		ps/°C	N
Overshoot and Preshoot	VL, VH = −0.1 V, +0.1 V, driver terminated into 50 Ω	0 – 50		0 + 50	% of step + mV	N
	VL, VH = 0.0 V, 3 V, driver terminated into 50 Ω	−6.0 – 50		6.0 + 50	% of step + mV	N
SETTLING TIME						
to 15 mV	VL = 0 V, VH = 0.5 V, driver terminated into 50 Ω		50		ns	N
to 4 mV	VL = 0 V, VH = 0.5 V		10		µs	N
Delay Change vs. Pulse Width	VL/VH = 0 V/3 V, PW = 2.5 ns/7.5 ns, 30 ns/90 ns, DC = 25%		25	75	ps	N
Delay Change vs. Duty Cycle	VL = 0 V, VH = 3 V, duty cycle 5% to 95%, T = 40 ns		25		ps	N
MINIMUM WIDTH PULSE						
1 V Swing	Measured at 50% point width V_{OUT} AC swing = 0.9 × V_{OUT} DC		0.6		ns	N
3 V Swing	Swing terminated, 50 Ω load on transmission line		1.5		ns	N
Toggle Rate	VH = 1 V, VL = 0 V, terminated to 50 Ω, V_{OUT} > 300 mV p-p		1000		MHz	N
DYNAMIC PERFORMANCE, INHIBIT						
Delay Time, Active to Inhibit	Measured at 50%, VH = 4 V, VL = 0 V, VTT = 2 V		1.7	2.0	ns	P
Delay Time, Inhibit to Active	Measured at 50%, VH = 4 V, VL = 0 V, VTT = 2 V		1.7	2.2	ns	P

Parameter	Conditions	Min	Typ[2]	Max	Unit	Specification[3] Performance
Delay Time Matching, Inhibit to Active	Measured at 50%, VH = 4 V, VL = 0 V, VTT = 2 V		150	250	ps	P
Delay Time Matching, Active to Inhibit	Measured at 50%, VH = 4 V, VL = 0 V, VTT = 2 V		150	250	ps	P
I/O Spike	VH = 0 V, VL = 0 V			200	mV p-p	N
Rise, Fall Time, Active to Inhibit	VL = 0 V, VTT = 2 V (20% to 80% of 1 V output)			1.2	ns	N
Rise, Fall Time, Inhibit to Active	VH = 4 V, VL = 0 V, VTT = 2 V (20% to 80% of 1 V output)			0.6	ns	N
DYNAMIC PERFORMANCE, VTERM						
Delay Time, VH to VTERM	Measured at 50%, VL = VH = 2 V, VTERM = 0 V, VTT = 0 V		1.5	1.9	ns	P
Delay Time, VL to VTERM	Measured at 50%, VL = VH = 0 V, VTERM = 2 V, VTT = 0 V		1.6	1.9	ns	P
Delay Time, VTERM to VH	Measured at 50%, VL = VH = 2 V, VTERM = 0 V, VTT = 0 V		1.6	2.0	ns	P
Delay Time, VTERM to VL	Measured at 50%, VL = VH = 0 V, VTERM = 2 V, VTT = 0 V		1.6	2.0	ns	P
Overshoot and Preshoot	VH/VL, VTERM = (0 V, 2 V), (0 V, 6 V)	−6.0 + 50		+6.0 + 50	% of step + mV	N
VTERM Rise Time, VL to VT, Normal Mode	VL, VH = 0 V, VTERM = 2 V, 20% to 80%			1.0	ns	N
VTERM Rise Time, VT to VH, Normal Mode	VL, VH = 2 V, VTERM = 0 V, 20% to 80%			0.6	ns	N
VTERM Fall Time, VT to VL, Normal Mode	VL, VH = 0 V, VTERM = 2 V, 20% to 80%			0.6	ns	N
VTERM Fall Time, VH to VT, Normal Mode	VL, VH = 2 V, VTERM = 0 V, 20% to 80%			1.0	ns	N

[1] All temperature coefficients are measured at T_J = 75°C to 95°C. In test figures, voltmeter loading is 1 MΩ or greater, and scope probe loading is 100 kΩ in parallel with 0.6 pF.
[2] Typical values are not tested or guaranteed. Nominal values are generated from design or simulation analyzes and/or limited bench evaluations and are not tested or guaranteed.
[3] Specification performance: N = nominal, P = production, maximum/minimum.
[4] VTERM linearity over the following condition: VL − 6 V < VTERM < VH + 6 V.

COMPARATOR[1]

Table 2.

Parameter	Conditions	Min	Typ[2]	Max	Unit	Specification[3] Performance
DC INPUT CHARACTERISTICS						
VCCO Range		+2.0		+4.5	V	N
Offset Voltage (V_{OS})	Common-mode Voltage = 0 V	−25		+25	mV	P
Offset Voltage Drift	Common-mode Voltage = 0 V		50		µV/°C	N
HCOMP, LCOMP	Over linearity range	−50		+50	µA	P
BIAS CURRENTS						
Voltage Range (V_{CM})		−0.5		+6.5	V	P

Parameter	Conditions	Min	Typ[2]	Max	Unit	Specification[3] Performance
Differential Voltage (V_{DIFF})				7	V	P
Gain Error	V_{IN} = −0.5 V to +6.5 V	−0.25		0.0	%FSR	N
Linearity Error	V_{IN} = −0.5 V to +6.5 V	−2		+2	mV	N
Extended Range Operation	HCOMP, LCOMP = −1, Output toggle V_{OUT} from −0.9 V to −1.1 V	−1.0			V	P
DIGITAL OUTPUTS						
Logic 1 Voltage, Q	Q or QB, 150 Ω to GND, 150 Ω from Q to QB	VCCO – 1.05		VCCO – 0.85	V	P
Logic 0 Voltage, QB	Q or QB, 150 Ω to GND, 150 Ω from Q to QB	VCCO – 2.2		VCCO – 1.5	V	P
Logic Differential, Q to QB	Q or QB, 150 Ω to GND, 150 Ω from Q to QB	0.65	0.9	1.15	V	P
Slew Rate	Q or QB (20% to 80% of output, 150 Ω from Q to QB)		380		ps	N
CHANNEL COMPARATOR SWITCHING PERFORMANCE PROPAGATION DELAY[4, 5, 6]						
Input to Output	V_{IN} = 3 V p-p, 2 V/ns	0.7		1.1	ns	P
Propagation Delay Temperature Coefficient	V_{IN} = 3 V p-p, 2 V/ns		1.0		ps/°C	N
Prop Delay Change with Respect to:						
Slew Rate: 1 V/ns, 2 V/ns, 3 V/ns	V_{IN} = 0 V to 3 V		120		ps	N
Amplitude: 500 mV, 1.0 V, 3.0 V	V_{IN} = 1.0 V/ns		100		ps	N
Equivalent Input Rise Time	V_{IN} = 0 V to 2 V, < 80 ps, 20% to 80% rise time driver in VTERM = 0 V		275		ps	N
Pulse Width Linearity	V_{IN} = 0 V to 3 V, 2 V/ns, PW = 3 ns, 4 ns, 5 ns, 10 ns, Driver Hi-Z mode			50	ps	N
Settling Time	Settling to ±8 mV, V_{IN} = 0 V to 3 V, Driver Hi-Z mode		25		ns	N
Hysteresis			6		mV	N
Comparator Propagation Delay Matching, HCOMP to LCOMP	V_{IN} = 0 V to 3 V, 2 V/ns			125	ps	P
INPUT CHARACTERISTICS (INHL, INHLB)	See Driver Spec No. 1					
Input Voltage	VIOH = 1 V, VIOL = 1 V, VCOM = 2 V, VDUT = 0 V	0		3.3	V	P
INHL, INHLB Bias Current	INHL, INHLB = 0 V, 3.3 V, AC tests 0.2 V and 0.8 V	−250		+250	µA	P
VIOH Current Program Range, IOH = 0 mA to −40 mA	VDUT = 0.8 V, 6.5 V	0		4.0	V	P

See notes on next page.

[1] All temperature coefficients are measured at T_J = 75°C to 95°C. In test figures, voltmeter loading is 1 MΩ or greater, and scope probe loading is 100 kΩ in parallel with 0.6 pF.

[2] Typical values are not tested or guaranteed. Nominal values are generated from design or simulation analyzes and/or limited bench evaluations and are not tested or guaranteed.
[3] Specification performance: N = nominal, P = production, maximum/minimum.
[4] All AC input values are referred to the source end of transmission line input.
[5] All AC tests are performed with driver in VTERM mode, except where noted.
[6] Rise time is calculated SQRT((comp out T_R)^2 − (comp in T_R)^2).

ACTIVE LOAD[1]

Table 3.

Parameter	Conditions	Min	Typ[2]	Max	Unit	Specification[3] Performance
DC CHARACTERISTICS						
VIOL Current Program Range, IOL = 0 mA to 40 mA	VDUT = −0.5 V, +5.2 V	0		4.0	V	P
VIOH, VIOL Input Bias Current	VIOL = 0 V, 4 V and VIOH = 0 V, 4 V	−300		+300	µA	P
IOXRTN Range VDUT = −0.5 V, +6.5 V	IOL = +40 mA, IOH = −40 mA		−0.5, +6.5		V	N
VDUT Range	IOL = +40 mA, IOH = −40 mA, |VDUT – VCOM| > 1.3 V	−0.5		+6.5	V	P
VDUT Range, IOH = 0 mA to −40 mA	VDUT – VCOM > 1.3 V	0.8		6.5	V	P
VDUT Range, IOL = 0 mA to +40 mA	VCOM − VDUT > 1.3 V	−0.5		+5.2	V	P
OUTPUT CHARACTERISTICS						
Accuracy						
Gain Error, Load Current, Normal Range Calculated at 1 mA and 40 mA points	IOL, IOH = 25 µA – 40 mA, VCOM = 0 V, VDUT = ±2 V, and IOL = 25 µA to 40 mA, VCOM = +6.5 V, VDUT = +5.2 V and IOH = 25 µA to 40 mA, VCOM = −0.5 V, VDUT = +0.8 V	−0.35		+0.35	%I_{SET}	P
Load Offset	Calculated from intercept of 1 mA and 40 mA points	−400		+400	µA	P
Load Nonlinearity	IOL, IOH from 25 µA to 40 mA	−80		+80	µA	P
Output Current Tempco	Measured at IOH, IOL = 200 µA		<±3		µA/°C	N
IOH Extended Range	Driver Inhibited, IOH = 1 mA, Change in IOH from VTT = 0 V to VTT =−1.0 V	2			%	P
VCOM BUFFER						
VCOM Buffer Offset Error	IOL, IOH = 40 mA, VCOM = 0 V	−50		+50	mV	P
VCOM Buffer Bias Current	VCOM = 0 V	−20		+20	µA	P
VCOM Buffer Gain Error	IOL, IOH = 40 mA, VCOM = −0.5 V to +6.5 V	−4		+4	%	P
VCOM Buffer Linearity Error	IOL, IOH = 40 mA, VCOMI = −0.5 V to +6.5 V	−10		+10	mV	P
DYNAMIC PERFORMANCE						
Propagation Delay						
±I_{MAX} to INHIBIT	VTT = 2 V, VCOM = 4 V/0 V, IOL = +20 mA, IOH = −20 mA	1.0	1.3	2.0	ns	P
INHIBIT to ±I_{MAX}	VTT= 2 V, VCOM = 4 V/0 V, IOL = +20 mA, IOH = −20 mA	1.2	1.8	2.4	ns	P
Propagation Delay Matching	Matching = (±I_{MAX} to INHIBIT test value) − (INHIBIT to ±I_{MAX} test value)	−1.0		+1.0	ns	P
I/O Spike	VCOM = 0 V, IOL = 20 mA, IOH =−20 mA		250		mV	N
Settling Time to 15 mV	IOL = +20 mA, IOH = −20 mA, 50 Ω load, to ±15		50		ns	N

Settling Time to 4 mV	mV IOL = +20 mA, IOH = −20 mA, 50 Ω load, to ±4 mV	10	µs	N

[1] All temperature coefficients are measured at T_J = 75°C to 95°C. In test figures, voltmeter loading is 1 MΩ or greater, and scope probe loading is 100 kΩ in parallel with 0.6 pF.
[2] Typical values are not tested or guaranteed. Nominal values are generated from design or simulation analyzes and/or limited bench evaluations and are not tested or guaranteed.
[3] Specification performance: N = nominal, P = production, maximum/minimum.

DYNAMIC CLAMP[1]

Table 4.

Parameter	Conditions	Min	Typ[2]	Max	Unit	Specification[3] Performance
Input Voltage, VCH		2		7.5	V	P
Input Voltage, VCL		−1.5		+4	V	P
Input Bias Current, VCH/VCL	Over ranges of: +2 < VCH < +7.5, and -1.5 > VCL > +4	−250		+250	µA	P
VCH, VCL Offset Error	I_{TEST} = 1 mA	−250		+250	mV	P
VCH, VCL Gain Error	I_{TEST} = 1 mA	0.96		1.01	V/V	P
Static Current Capability		50		75	mA	N
Incremental Resistance	11 mA to 21 mA	45	48	52	Ω	P
VCHP, VCLP Protection Diodes V_f @ 500 µA		0.52		0.64	V	P
Protection Diodes Maximum Current	For information only			2	mA	N

[1] All temperature coefficients are measured at T_J = 75°C to 95°C. In test figures, voltmeter loading is 1 MΩ or greater, and scope probe loading is 100 kΩ in parallel with 0.6 pF.
[2] Typical values are not tested or guaranteed. Nominal values are generated from design or simulation analyzes and/or limited bench evaluations and are not tested or guaranteed.
[3] Specification performance: N = nominal, P = production, maximum/minimum.

TOTAL FUNCTION

Table 5.

Parameter	Conditions	Min	Typ[1]	Max	Unit	Specification[2] Performance
PWRD Input Voltage		0		5	V	P
PWRD Bias Current	PWRD trip point 1.4 V ±0.15 V	−250		+250	µA	P
Power-down Supply Reduction	VIOH = 0 V, VIOL = 0 V	35		60	%	P
Power-down Output Leakage Current	VIOH = 0 V, VIOL = 0 V V_{OUT} = −0.5 V to +5.5 V	−20		+20	nA	P
Power-down Output Leakage Current	VIOH = 0 V, VIOL = 0 V V_{OUT} = 5.5 V to 6.5 V	−500		+500	nA	P
Output Leakage Current	V_{OUT} = −0.5 V to +6.5 V	−1		+1	µA	P
Output Leakage Current	V_{OUT} = 0 V to 5 V	−500		+500	nA	P
Output Leakage Current	V_{OUT} = −1 V	−5		+5	µA	P
Output Capacitance	Driver and load inhibited		9.2		pF	N
Output Capacitance Term	Driver VTERM = 0 V, load inhibited		2.5		pF	N

[1] Typical values are not tested or guaranteed. Nominal values are generated from design or simulation analyzes and/or limited bench evaluations and are not tested or guaranteed.
[2] Specification performance: N = nominal, P = production, maximum/minimum.

POWER SUPPLIES

Table 6.

Parameter	Conditions	Min	Typ[1]	Max	Unit	Specification[2] Performance
Total Supply Range			15		V	N
Positive Supply, VCC			10.5		V	N
Negative Supply, VEE			−4.5		V	N
Positive Supply Current, VCC	Driver = Inhibit, I_{LOAD} Program = 40 mA, Load = Active		465	570	mA	P
Negative Supply Current, VEE	Driver = Inhibit, I_{LOAD} Program = 40 mA, Load = Active		475	600	mA	P
Comparator Supply Current Overhead, VCCO	Driver = Inhibit, I_{LOAD} Program = 40 mA, Load = Active (I_{VCCO} − (comparator logic output currents))			45	mA	P
Total Power Dissipation	Driver = Inhibit, I_{LOAD} Program = 40 mA, Load = Active		7.2	7.9	W	P
Total Power Dissipation	Driver = Inhibit, I_{LOAD} Program = 40 mA, 0 mA		5.2	5.9	W	P
Temperature Sensor Gain Factor	R_{LOAD} = 10 kΩ, V_{SOURCE} = 10.5 V		1		µA/K	N

[1] Typical values are not tested or guaranteed. Nominal values are generated from design or simulation analyzes and/or limited bench evaluations and are not tested or guaranteed.
[2] Specification performance: N = nominal, P = production, maximum/minimum.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
POWER SUPPLY VOLTAGE	
V_{CC} to GND	11.3 V
V_{EE} to GND	−7 V
V_{CC} to V_{EE}	18 V
VCCO to GND	5.5 V
PWRGND, DRGND, GND_ROT, or HQGND	±0.4 V
OUTPUTS	Indefinite[1]
V_{OUT}, Short-Circuit Duration	
V_{OUT}, Inhibit Mode	+8.5 V, −2 V
V_{OUT}, Inhibit Mode	VL − 5.5 V < V_{OUT} < VH + 5.5 V
VHDCPL	Do not connect except for capacitor to V_{CC}
VLDCPL	Do not connect except for capacitor to V_{EE}
QH, QHB, QL, QLB MAXIMUM IOUT	
Continuous	50 mA
Surge	100 mA
THERM	11 V, 0 V
Driver Output Capacitance, Maximum	10 pF

Parameter	Rating
INPUTS	
DATA, DATAB, IOD, IODB, RLD, RLDB	V_{CCO} + 1.5 V, V_{CCO} − 4.5 V
INHL, INHLB, CMPD	−0.4 V to +5.5 V
PWRD	−0.4 V to +4.5 V
DATA to DATAB, IOD to IODB, RLD to RLDB	±3 V
INHL to INHLB	±6 V
VH, VL, VTERM to GND (R_{SERIES} < 500 Ω)	+7.5 V, −1.1 V
VH to VL	+8 V, −3.5 V
VH − VTERM and VTERM − VL	±8 V
Reflection Clamp High/Low	+8.5 V, −2 V
Protection Clamp Breakdown Voltage	12 V
Protection Clamp Current	±5 mA
V_{OUT} to HCOMP or LCOMP	±7.8 V
ENVIRONMENTAL	
Operating Temperature (Junction)	175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[2]	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] Output short-circuit protection is guaranteed as long as proper heat sinking is employed to ensure compliance with the operating temperature limits.

[2] To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C ± 5°C (75°F ± 10°F) with relative humidity not to exceed 65%.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 8. Driver Truth Table

DATA	DATAB	IOD	IODB	RLD	RLDB	Output State
0	1	1	0	X	X	VL
1	0	1	0	X	X	VH
X	X	0	1	0	1	INH and CLAMP
X	X	0	1	1	0	VTERM

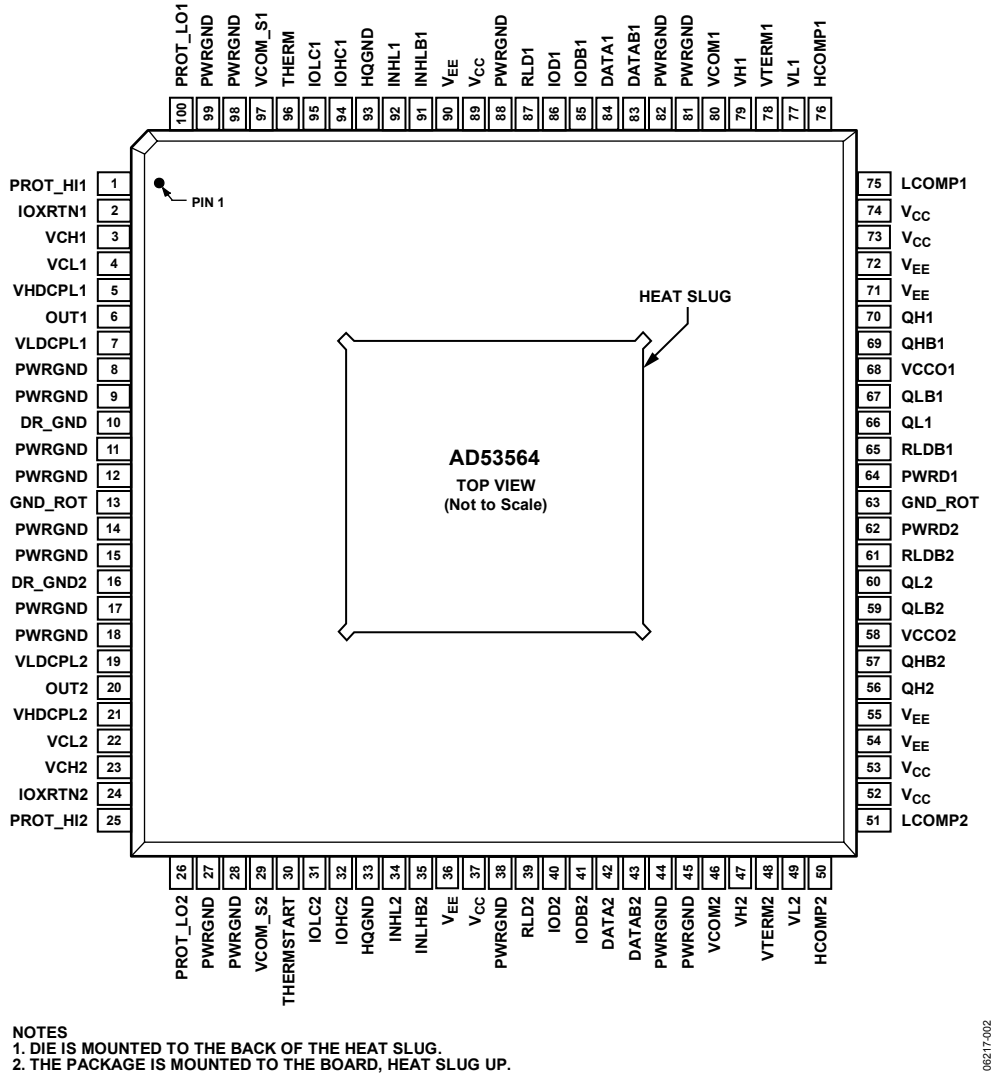
Table 9. Comparator Truth Table

V_{OUT}		Output States			
		QH	QHB	QL	QLB
>HCOMP	>LCOMP	1	0	1	0
>HCOMP	<LCOMP	1	0	0	1
<HCOMP	>LCOMP	0	1	1	0
<HCOMP	<LCOMP	0	1	0	1

Table 10. Active Load Truth Table

			Output States (Including Diode Bridge)		
VDUT	INHL	INHLB	IOH	IOL	I (V_{OUT})
<VCOM	0	1	V(IOHC) × +10 mA	V(IOLC) × −10 mA	IOL
>VCOM	0	1	V(IOHC) × +10 mA	V(IOLC) × −10 mA	IOH
X	1	0	0	0	0

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DIE IS MOUNTED TO THE BACK OF THE HEAT SLUG.
2. THE PACKAGE IS MOUNTED TO THE BOARD, HEAT SLUG UP.

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	PROT_HI1	Channel 1, Output Voltage Sensing Diode.
2	IOXRTN1	Current Return Path for the Active Load for Channel 1. Typically connected to a power ground.
3	VCH1	Analog Input Voltage that Sets the Reflection Clamp High Level of Channel 1.
4	VCL1	Analog Input Voltage that Sets the Reflection Clamp Low Level of Channel 1.
5	VHDCPL1	Internal Supply Decoupling for the Driver Output Stage of Channel 1. This pin needs to be connected to V_{CC} through a 39 nF (minimum) capacitor.
6	OUT1	Input/Output for the Driver, Window Comparator, Reflection Clamp, and Active Load of Channel 1.
7	VLDCPL1	Internal Supply Decoupling for the Driver Output Stage of Channel 1. This pin needs to be connected to V_{EE} through a 39 nF (minimum) capacitor.

Pin Number	Mnemonic	Description
8, 9, 11, 12, 14, 15, 17, 18, 27, 28, 38, 44, 45, 81, 82, 88, 98, 99	PWRGND	Power Ground.
10	DR_GND	Analog Ground.
13, 63	GND_ROT	Analog Ground.
16	DR_GND2	Analog Ground.
19	VLDCPL2	Internal Supply Decoupling for the Driver Output Stage of Channel 2. This pin needs to be connected to V_{EE} through a 39 nF (minimum) capacitor.
20	OUT2	Input/Output for the Driver, Window Comparator, Reflection Clamp, and Active Load of Channel 2.
21	VHDCPL2	Internal Supply Decoupling for the Driver Output Stage of Channel 2. This pin needs to be connected to V_{CC} through a 39 nF (minimum) capacitor.
22	VCL2	Analog Input Voltage that Sets the Reflection Clamp Low Level of Channel 2.
23	VCH2	Analog Input Voltage that Sets the Reflection Clamp High Level of Channel 2.
24	IOXRTN2	Current Return Path for the Active Load for Channel 2. Typically connected to a power ground.
25	PROT_HI2	Channel 2, Output Voltage Sensing Diode.
26	PROT_LO2	Channel 2, Output Voltage Sensing Diode.
29	VCOM_S2	Analog Output Voltage that Represents a Buffered VCOM1 Input.
30	THERMSTART	Temperature Sensor Start-Up Pin. Normally not connected.
31	IOLC2	Analog Input Voltage that Programs the Channel 2 Active Load Source Current.
32	IOHC2	Analog Input Voltage that Programs the Channel 2 Active Load Sink Current.
33	HQGND	Clean Analog Ground for the Active Load for Channel 2.
34	INHL2	One of Two Complementary Inputs that Control the Inhibit Mode for the Active Load Bridge of Channel 2.
35	INHLB2	One of Two Complementary Inputs that Control the Inhibit Mode for the Active Load Bridge of Channel 2.
36, 54, 55, 71, 72, 90	V_{EE}	Negative Supply Terminal.
37, 52, 53, 73, 74, 89	V_{CC}	Positive Supply Terminal.
39	RLD2	One of Two Complementary Inputs that Control, in Conjunction with IOD2 and IODB2, the Operating Mode of the Channel 2 Driver. Refer to Table 8 for specific conditions.
40	IOD2	One of Two Complementary Inputs that Control, in Conjunction with RLD2 and RLDB2, the Operating Mode of the Channel 2 Driver. Refer to Table 8 for specific conditions.
41	IODB2	One of Two Complementary Inputs that Control, in Conjunction with RLD2 and RLDB2, the Operating Mode of the Channel 2 Driver. Refer to Table 8 for specific conditions.
42	DATA2	One of Two Complementary Inputs that Determine the High and Low State of the Channel 2 Driver. Driver output is high for DATA2 > DATAB2. Refer to Table 8 for specific conditions.
43	DATAB2	One of Two Complementary Inputs that Determine the High and Low State of the Channel 2 Driver. Driver output is high for DATA2 > DATAB2. Refer to Table 8 for specific conditions.
46	VCOM2	Analog Input Voltage that Establishes the Commutation Voltage for the Active Load Diode Bridge for Channel 2.
47	VH2	Analog Input Voltage that Sets the Logic 1 Level of the Driver Output Limit for Channel 2. Determines the driver output for DATA2 > DATAB2.

Pin Number	Mnemonic	Description
48	VTERM2	Analog Input Voltage that Sets the Termination Voltage Level of the Channel 2 Driver when in VTERM Mode.
49	VL2	Analog Input Voltage that Sets the Logic 0 Level of the Driver Output Limit for Channel 2. Determines the driver output for DATAB2 > DATA2.
50	HCOMP2	Analog Input Voltage that Sets the Logic 1 Compare Reference for the Window Comparator of Channel 2.
51	LCOMP2	Analog Input Voltage that Sets the Logic 0 Compare Reference for the Window Comparator of Channel 2.
56	QH2	One of Two Complementary Outputs for the Logic 1 Window Comparator of Channel 1.
57	QHB2	One of Two Complementary Outputs for the Logic 1 Window Comparator of Channel 1.
58	VCCO2	Input Supply Voltage for QH2, QHB2, QL2, and QLB2 Signals and Reference Voltage for DATA2, DATAB2, IOD2, IODB2, RLD2, and RLDB2.
59	QLB2	One of Two Complementary Outputs for the Logic 0 Window Comparator of Channel 2.
60	QL2	One of Two Complementary Outputs for the Logic 0 Window Comparator of Channel 2.
61	RLDB2	One of Two Complementary Inputs that Control, in Conjunction with IOD2 and IODB2, the Operating Mode of the Channel 2 Driver. Refer to Table 8 for specific conditions.
62	PWRD2	Power-Down Control for Channel 2.
64	PWRD1	Power-Down Control for Channel 1.
65	RLDB1	One of Two Complementary Inputs that Control, in Conjunction with IOD1 and IODB1, the Operating Mode of the Channel 1 Driver.
66	QL1	One of Two Complementary Outputs for the Logic 0 Window Comparator of Channel 1.
67	QLB1	One of Two Complementary Outputs for the Logic 0 Window Comparator of Channel 1.
68	VCCO1	Input Supply Voltage for QH1, QHB1, QL1, and QLB1 Signals and Reference Voltage for DATA1, DATAB1, IOD1, IODB1, RLD1, and RLDB1.
69	QHB1	One of Two Complementary Outputs for the Logic 1 Window Comparator of Channel 1.
70	QH1	One of Two Complementary Outputs for the Logic 1 Window Comparator of Channel 1.
75	LCOMP1	Analog Input Voltage that Sets the Logic 0 Compare Reference for the Window Comparator of Channel 1.
76	HCOMP1	Analog Input Voltage that Sets the Logic 1 Compare Reference for the Window Comparator of Channel 1.
77	VL1	Analog Input Voltage that Sets the Logic 0 Level of the Driver Output Limit for Channel 1. Determines the driver output for DATAB1 > DATA1.
78	VTERM1	Analog Input Voltage that Sets the Termination Voltage Level of the Channel 1 Driver when in VTERM Mode.
79	VH1	Analog Input Voltage that Sets the Logic 1 Level of the Driver Output Limit for Channel 1. Determines the driver output for DATA1 > DATAB1.
80	VCOM1	Analog Input Voltage that Establishes the Commutation Voltage for the Active Load Diode Bridge for Channel 1.
83	DATAB1	One of Two Complementary Inputs that Determine the High and Low State of the Channel 1 Driver. Driver output is high for DATA1 > DATAB1. Refer to the Driver Truth Table for specific conditions.
84	DATA1	One of Two Complementary Inputs that Determine the High and Low State of the Channel 1 Driver. Driver output is high for DATA1 > DATAB1. Refer to the Driver Truth Table for specific conditions.
85	IODB1	One of Two Complementary Inputs that Control, in Conjunction with RLD1 and RLDB1, the Operating Mode of the Channel 1 Driver. Refer to Table 8 for specific conditions.
86	IOD1	One of Two Complementary Inputs that Control, in Conjunction with RLD1 and RLDB1, the Operating Mode of the Channel 1 Driver. Refer to Table 8 for specific conditions.
87	RLD1	One of Two Complementary Inputs that Control, in Conjunction with IOD1 and IODB1, the

Pin Number	Mnemonic	Description
		Operating Mode of the Channel 1 Driver. Refer to Table 8 for specific conditions.
91	INHLB1	One of Two Complementary Inputs that Control the Inhibit Mode for the Active Load Bridge of Channel 1.
92	INHL1	One of Two Complementary Inputs that Control the Inhibit Mode for the Active Load Bridge of Channel 1.
93	HQGND	Clean Analog Ground for the Active Load for Channel 1.
94	IOHC1	Analog Input Voltage that Programs the Channel 1 Active Load Sink Current.
95	IOLC1	Analog Input Voltage that Programs the Channel 1 Active Load Source Current.
96	THERM	Temperature Sensor Output Pin. A resistor (10 kΩ) should be connected between THERM and V_{CC}. The approximate die temperature can be determined by measuring the current through the resistor. The typical scale factor is 1 µA/K.
97	VCOM_S1	Analog Output Voltage that Represents a Buffered VCOM1 Input.
100	PROT_LO1	Channel 1 Output Voltage Sensing Diode.

OUTLINE DIMENSIONS

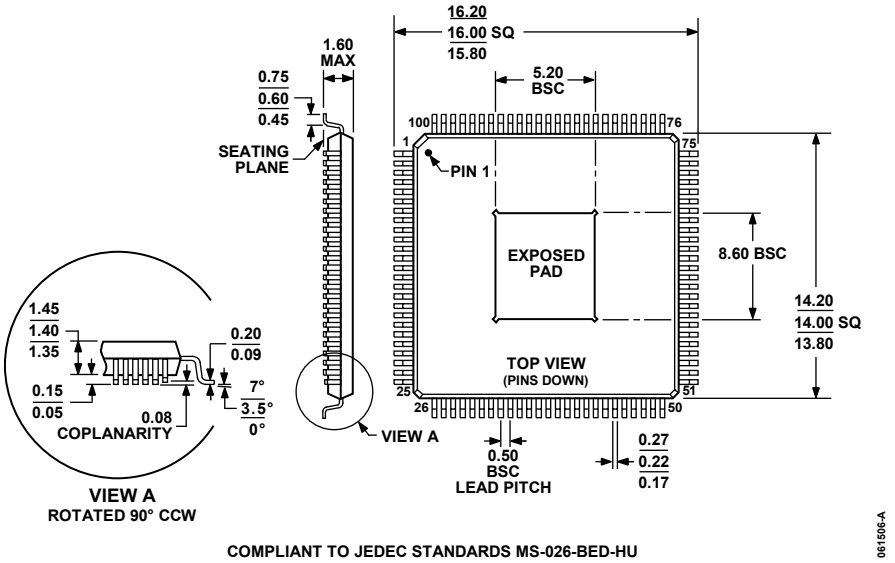


Figure 3. 100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP] (SW-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD53564JSW	0°C to 70°C	100-Lead Low Profile Quad Flat Package, Exposed Pad (LQFP_EP)	SW-100-1

NOTES

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