

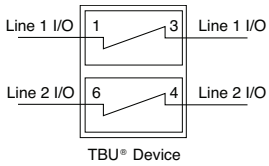
Features

- Superior circuit protection
- Overcurrent protection
- Blocks surges up to rated voltage limit
- High-speed performance
- Small SMT package
- RoHS compliant*
- AEC-Q101 compliant**

TBU-DB-Q Series - TBU® High-Speed Protectors

General Information

The TBU-DB-Q Series of Bourns® TBU® products are low capacitance dual bidirectional high-speed protection components, constructed using MOSFET semiconductor technology, and designed to protect against faults caused by short circuits, overvoltage transients and faults in battery cells, up to rated limits.



TBU® Device

The TBU® high-speed protector placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics will not be exposed to large currents during transient events.

The TBU® device is provided in a surface mount DFN package and meets industry standard requirements such as RoHS and Pb Free solder reflow profiles.

Additional Information

Click these links for more information:

PRODUCT SELECTOR | TECHNICAL LIBRARY | INVENTORY | SAMPLES | CONTACT

Absolute Maximum Ratings (@ T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Value	Unit
V_{imp}	Peak impulse voltage withstand with duration less than 10 ms	550	V
V_{dc}	Peak DC voltage withstand with duration less than 1 hour	450	V
T_{op}	Operating temperature range	-55 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C
T_{amax}	Maximum Ambient Temperature	+125	°C

Electrical Characteristics (@ T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{trigger}$	Current required for the device to go from operating state to protected state	100	150	200	mA
R_{device}	Series resistance of the TBU® device	10.5	13.5	16.5	Ω
R_{match}	Package resistance matching of the TBU® device #1 - TBU® device #2			±0.5	Ω
t_{block}	Time taken for the device to go into current limiting		1		µs
I_Q	Current through the triggered TBU® device with 50 Vdc circuit voltage		0.5		mA
V_{reset}	Voltage below which the triggered TBU® device will transition to normal operating state	4.5	7.5	9.5	V
$R_{th(j-a)}$	Junction to package pads - FR4 using JESD51-3 board		125		°C/W
$R_{th(j-a)}$	Junction to package pads - FR4 using JESD51-7 board		50		°C/W

Environmental Characteristics

Parameter	Value
Moisture Sensitivity Level	1
ESD Classification (HBM)	1B

CALIFORNIA WARNING: Can expose you to lead, a carcinogen and reproductive toxicant. See www.P65Warnings.ca.gov

*RoHS Directive 2015/863, Mar 31, 2015 and Annex.
**"Q" part number suffix for automotive and other applications requiring appropriate AEC-Q101 compliance.
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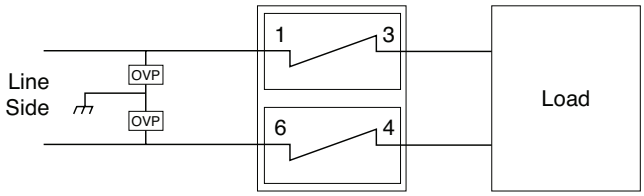
Reference Application

The TBU® devices are general use protectors used in a wide variety of applications, including telecommunications, industrial communications and automotive battery management systems. The maximum voltage rating of the TBU® device should never be exceeded. Where necessary, an OVP device should be employed to limit the maximum voltage. A cost-effective protection solution combines Bourns® TBU® protection devices with a pair of Bourns® TISP® Overvoltage Protectors or MOVs. For bandwidth sensitive applications, a Bourns® GDT may be substituted for the MOV.



TBU® Device

Basic TBU Operation

The TBU® device, constructed using MOSFET semiconductor technology, placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during transient events. When operated, the TBU® device will limit the current to less than the $I_{trigger}$ value within the t_{block} duration. If voltage above V_{reset} is continuously sustained, the TBU® device will subsequently reduce the current to a quiescent current level within a period of time that is dependent upon the applied voltage.

After the surge, the TBU® device resets when the voltage across the TBU® device falls to the V_{reset} level. The TBU® device will automatically reset on lines which have no DC bias or have DC bias below V_{reset} (such as unpowered signal lines).

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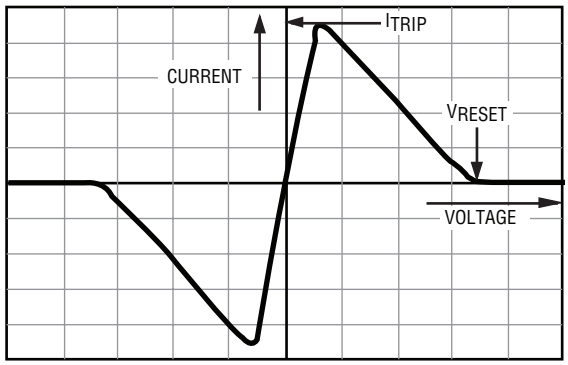
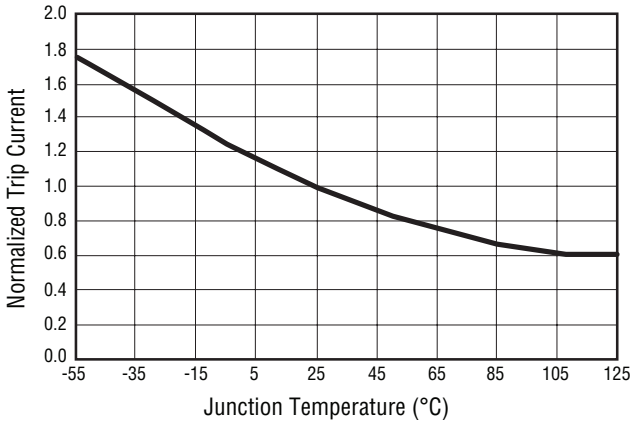
Performance Graphs

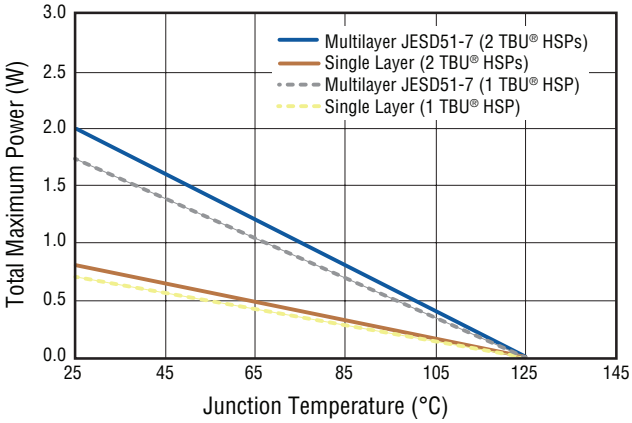
Typical V-I Characteristics



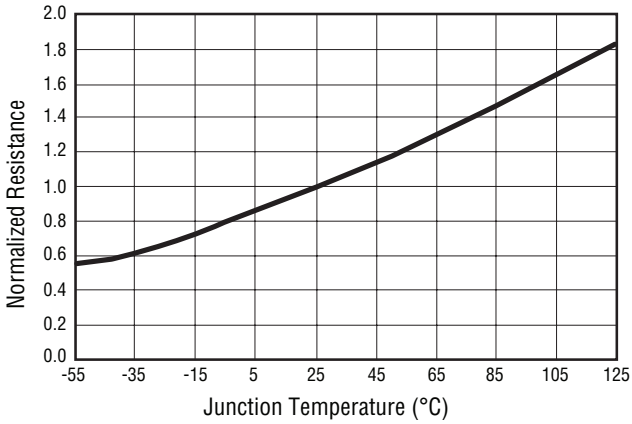
Typical Trigger Current vs. Temperature



Power Derating Curve



Typical Resistance vs. Temperature



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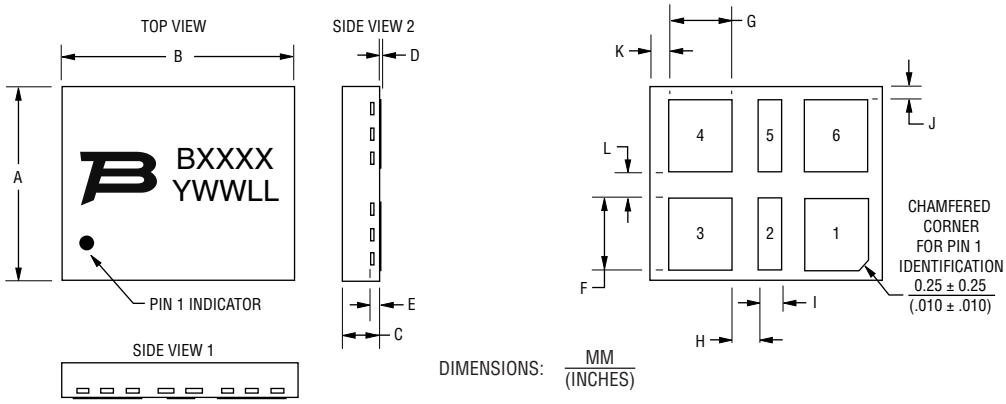
Product Dimensions



Dim.	Min.	Nom.	Max.
A	5.40 (.213)	5.50 (.217)	5.60 (.220)
B	6.40 (.252)	6.50 (.256)	6.60 (.260)
C	0.80 (.031)	0.90 (.035)	1.00 (.039)
D	0.00 (.000)	—	0.05 (.002)
E	0.20 (.008) REF.		
F	1.90 (.075)	2.00 (.079)	2.10 (.083)
G	1.75 (.069)	1.85 (.073)	1.95 (.077)
H	0.65 (.026)	0.70 (.028)	0.75 (.030)
I	0.70 (.028)	0.80 (.031)	0.90 (.035)
J	0.30 (.012)	0.35 (.014)	0.40 (.016)
K	0.25 (.010)	0.30 (.012)	0.35 (.014)
L	0.75 (.030)	0.80 (.031)	0.85 (.033)

Pad #	Pin Out
1	Line 1 In/Out
2	NU (Not Used)
3	Line 1 In/Out
4	Line 2 In/Out
5	NU (Not Used)
6	Line 2 In/Out

NOTES:

1. Pin 1 Indicator is laser marked; radius and location within the Pin 1 terminal.
   Pin 1 dot size: 0.500 ± 0.125 mm / .020 ± .005 in.
2. Pin 2 and 5 are NU (Not Used) and must be left unconnected; do not connect to In/Out lines, do not connect to system Ground.
3. Coplanarity on exposed pads shall not exceed 0.08 mm / .003 in.
4. Warpage shall not exceed 0.10 mm / .004 in. on all surfaces.
5. Exposed tie bars at package side are not plated.

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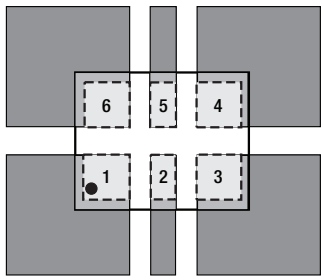
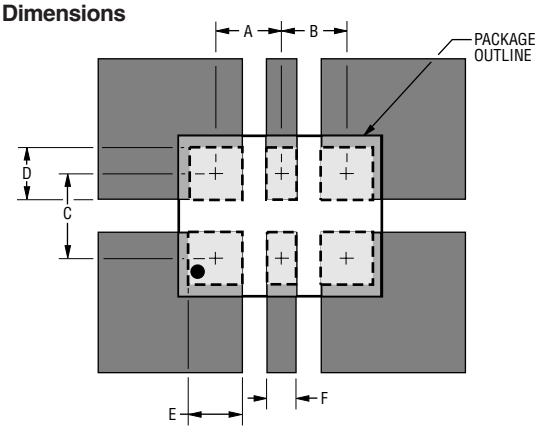
Recommended Pad Layout

TBU® High-Speed Protectors have a 100 % matte-tin termination finish. For improved thermal dissipation, the recommended layout uses PCB copper areas which extend beyond the exposed solder pad. The exposed solder pads should be defined by a solder mask which matches the pad layout of the TBU® device in size and spacing. It is recommended that they should be the same dimension as the TBU® pads but if smaller solder pads are used, they should be centered on the TBU® package terminal pads and not more than 0.10-0.12 mm (0.004-0.005 in.) smaller in overall width or length. Solder pad areas should not be larger than the TBU® pad sizes to ensure adequate clearance is maintained. The recommended stencil thickness is 0.10-0.12 mm (0.004-0.005 in.) with a stencil opening size 0.025 mm (0.0010 in.) less than the solder pad size. Extended copper areas beyond the solder pad significantly improve the junction to ambient thermal resistance, resulting in operation at lower junction temperatures with a corresponding benefit of reliability. All pads should soldered to the PCB, including pads marked as NC or NU but no electrical connection should be made to these pads. Care should be taken to assure no resistive path exists between the NU pins to any other point to avoid unexpected performance issues. For minimum parasitic capacitance, it is recommended that signal, ground or power signals are not routed beneath any pad.



Dark grey areas show added PCB copper area for better thermal resistance.

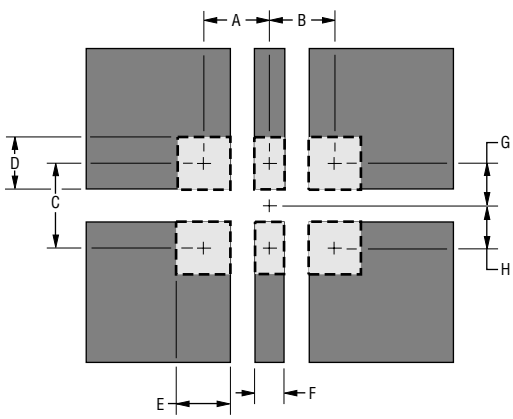
Solder Pad Dimensions



Dimensions	
A	2.025 (0.080)
B	2.025 (.080)
C	2.80 (.110)
D	2.00 (.079)
E	1.85 (.073)
F	0.80 (.031)

DIMENSIONS: MM (INCHES)

Recommended Stencil Opening



Dimensions	
A	2.025 (0.080)
B	2.025 (.080)
C	2.80 (.110)
D	1.95 (.077)
E	1.80 (.071)
F	0.75 (.030)
G	1.40 (.055)
H	1.40 (.055)

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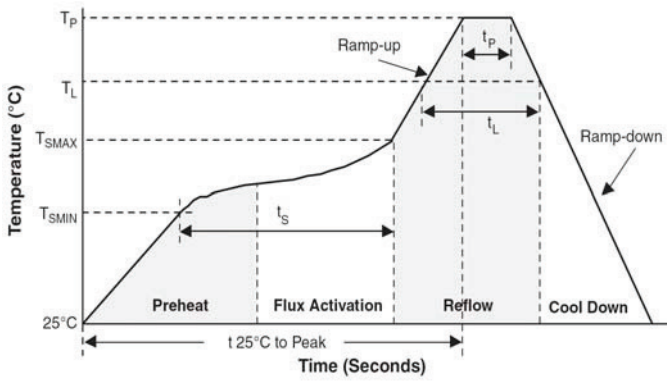
Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	 150 °C 200 °C 60-180 sec.
Time maintained above: - Temperature (TL) - Time (tL)	 217 °C 60-150 sec.
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.



How to Order

TBU - DB 055 - 100 - WH - Q

TBU® Product

Series
DB = Dual Bidirectional Series

Impulse Voltage Rating
055 = 550 V

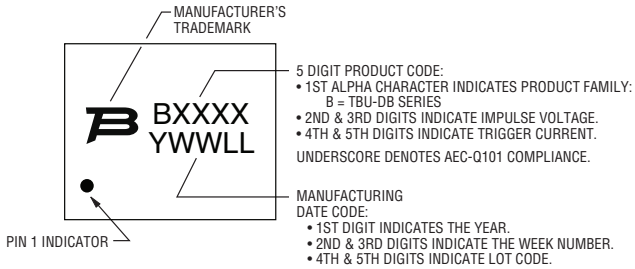
Trigger Current
100 = 100 mA

Hold to Trip Ratio Suffix
W = Hold to Trip Ratio

Package Suffix
H = DFN Package

AEC-Q101 Suffix
Q = AEC-Q101 Compliant

Typical Part Marking



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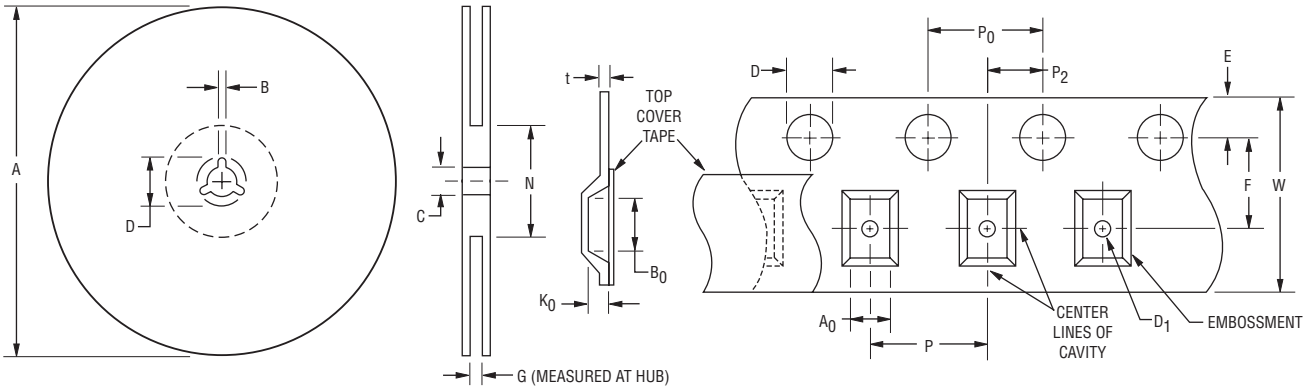
Packaging Specifications



QUANTITY: 3000 PIECES PER REEL

A		B		C		D		G	N
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
328.5 (12.93)	331 (13.05)	2.0 (0.079)	2.4 (0.094)	12.8 (0.504)	13.5 (.531)	17.0 (0.669)	17.4 (0.690)	16.5 (0.650)	100 ± 1.5 (3.94 ± 0.059)

A_0		B_0		D_0		D_1		E		F	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	max.
5.75 (0.224)	5.95 (0.234)	6.75 (0.266)	6.95 (0.274)	1.5 (0.059)	1.6 (0.063)	1.5 (0.059)	—	1.65 (0.065)	1.85 (0.073)	7.4 (0.291)	7.6 (0.299)
K_0		P		P_0		P_2		t		W	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
1.05 (0.041)	1.25 (0.049)	7.9 (0.311)	8.1 (0.319)	3.9 (0.159)	4.1 (0.161)	1.9 (0.075)	2.1 (0.083)	0.25 (0.010)	0.35 (0.014)	15.7 (0.618)	16.3 (0.642)

DIMENSIONS: MM (INCHES)

BOURNS®

Asia-Pacific: Tel: +886-2 2562-4117 • Email: asiacus@bourns.com
Europe: Tel: +36 88 885 877 • Email: eurocus@bourns.com
Mexico: Tel: +52 614 478 0400 • Email: mexicus@bourns.com
The Americas: Tel: +1-951 781-5500 • Email: americus@bourns.com
www.bourns.com

REV. 10/26

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