EV48H83A MEC1753B Evaluation Board User Guide

EV48H83A

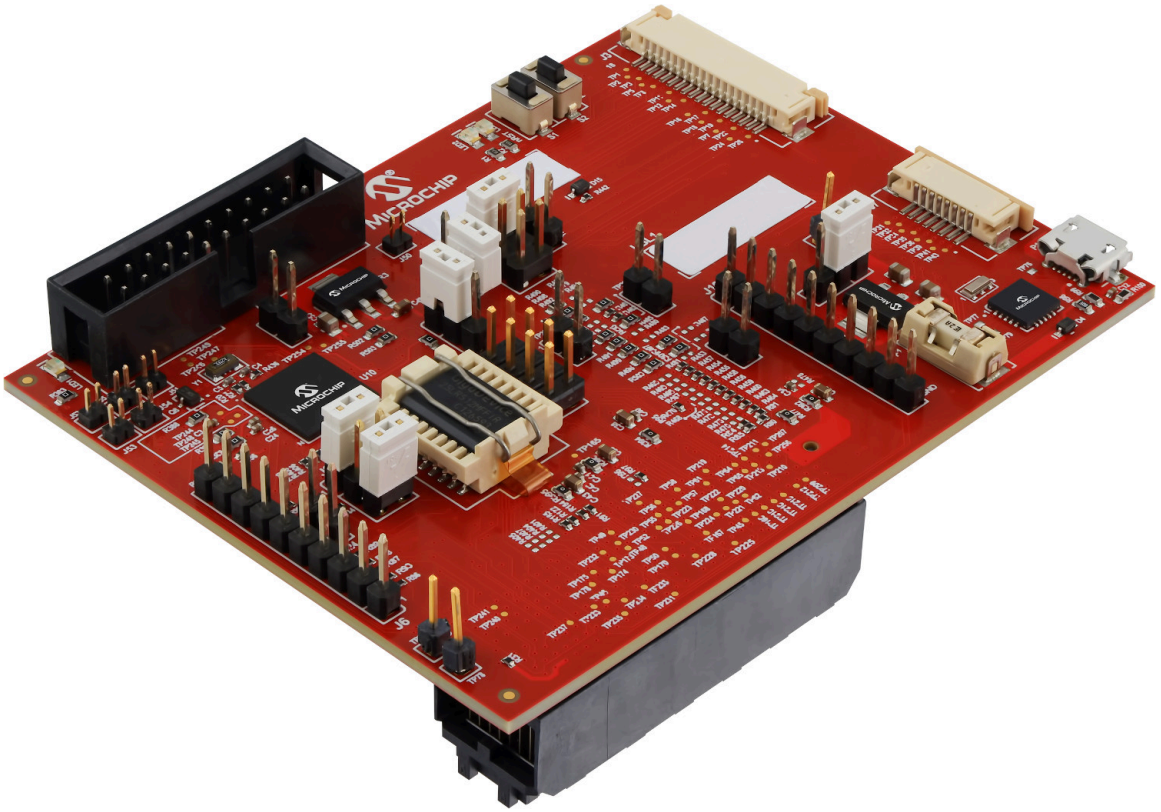
Product Page Links

Introduction

The EV48H83A evaluation board supports the MEC1753B, a highly configurable embedded keyboard controller that accommodates a broad range of peripheral functions. The device provides a wide range of security features and includes support for Post Quantum Computing (PQC). The board is primarily intended for use with the Intel Meteor Lake Reference Validation Platform (RVP). The EV48H83A board serves as a platform for the development of BIOS, drivers, firmware and related software. This evaluation board can be also used as a standalone embedded controller development board for embedded and industrial computing applications. This document outlines the features of the EV48H83A evaluation board and provides setup procedures for comprehensive system development, application validation, or standalone operation for application development. The board is equipped with an Intel-specified 240-Pin Expansion Connector and MS Windows keyboard connectors, enabling direct connection to the Intel Meteor Lake RVP via the expansion connector.

To enhance flexibility, the board includes a JTAG header for programming the MEC1753B, a QSPI Socket that allows users to select their preferred QSPI memory, and configurable resistor options to enable various MEC1753B features and interface them with the 240-Pin Expansion Connector.

Figure 1. EV48H83A Evaluation Board



© 2026 Microchip Technology Inc. and its subsidiaries

Table of Contents

Introduction....1

1. Evaluation Board Hardware....3
   - 1.1. Features....3
   - 1.2. Jumper Settings....4
   - 1.3. Component Description....4
   - 1.4. Connectors....5

2. Collateral....6

3. Board Programming....7

Microchip Information....8
- Trademarks....8
- Legal Notice....8
- Microchip Devices Code Protection Feature....8

Product Page Links....9

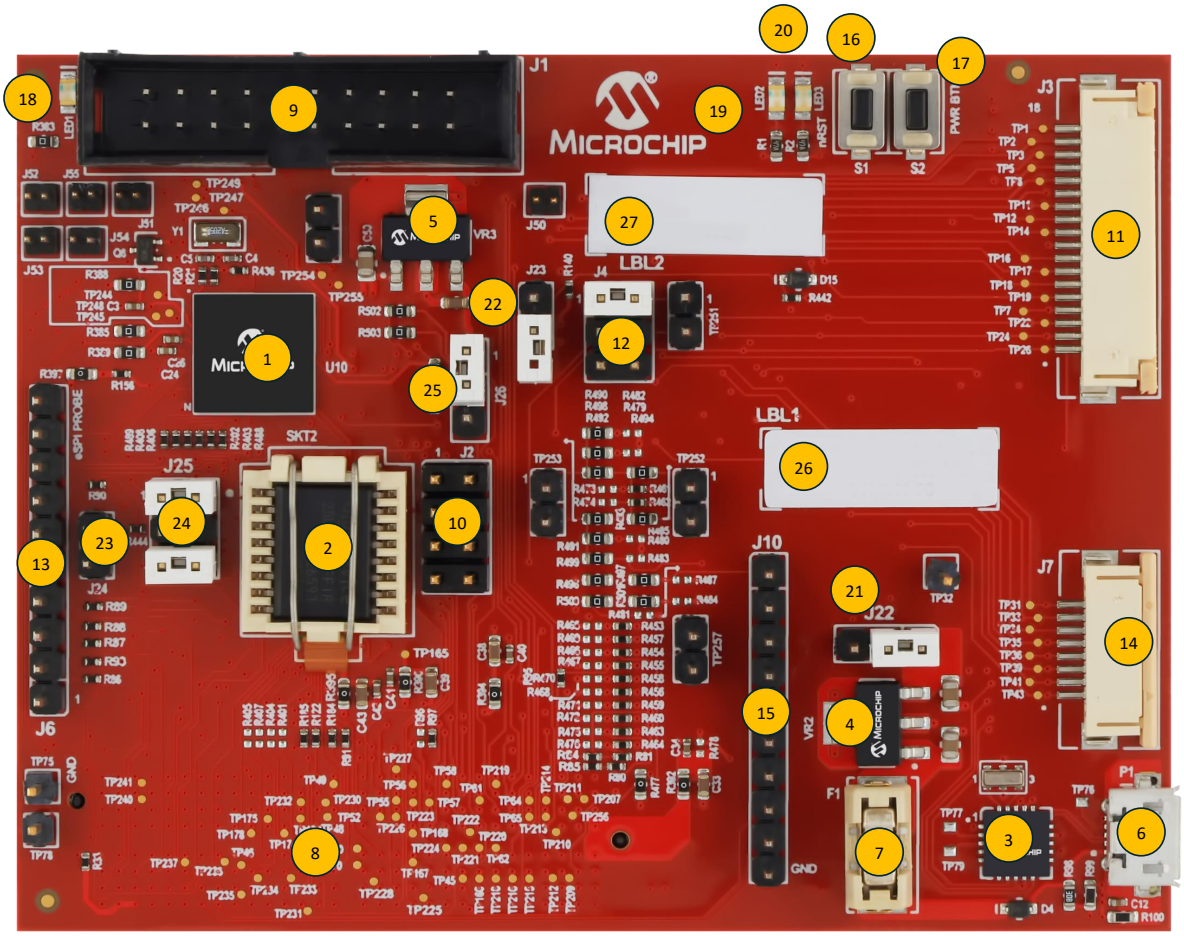
© 2026 Microchip Technology Inc. and its subsidiaries

1. Evaluation Board Hardware

1.1. Features

The following diagram highlights the features of the EV48H83A evaluation board.

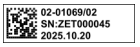
Figure 1-1. EV48H83A Evaluation Board

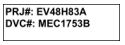


1. MEC1753B Device
2. 512 Mb QSPI Memory Socket and Device
3. MCP2200 USB-to-UART Interface
4. VR2 3.3V LDO
5. VR3 1.8V LDO
6. Micro USB Connector
7. Board Fuse
8. P2 240-Pin Connector (Backside Mounted)
9. J1 - JTAG Header
10. J2 Dediprog SF100 Header
11. J3 - 18-Pin KSI Keyboard Header
12. J4 - Software Developer Interface
13. J6 - ESPI Probe Header
14. J7 - 8-Pin KSO Keyboard Header
15. J10 - Power Sequence Header
16. S1 - Reset Switch
17. S2- Power Button Switch
18. LED1 - EC-CORE Power
19. LED2 - Connected to GPIO153
20. LED3 - Connected to GPIO157
21. J22 - Power Source Selection(1)
22. J23 - Crisis Recovery Strap(1)
23. J24 - BSS Strap(1)
24. J25 - Configuration Jumper(1)
25. J26 - VTR2 Power Select(1)
26. LBL1 - Serial Number Label(2)
27. LBL2 - Identification Label(3)

© 2026 Microchip Technology Inc. and its subsidiaries

Notes:

1. See Jumper Settings for possible jumper settings and default values
2. Example format of LBL1 - Serial Number Label: 

3. Format of LBL2 - Identification label: 

1.2. Jumper Settings

The EV48H83A evaluation board provides several jumper settings that allow users to configure features and operational modes as needed.

Table 1-1. EV48H83A Jumper Settings

Jumper #	Description	Jumper Settings
J22	Power Source Selection	1-2 (Default): Board is powered from the USB connector 2-3: Board is powered through the 240-pin connector
J23	Crisis Recovery Strap	Open (Default): Crisis recovery is disabled Closed: Crisis recovery is enabled
J24	BSS Strap	Open (Default): Bootstrap mode is disabled Closed: Bootstrap mode is enabled
J25	6-Pin Configuration	1-2 (Closed, Default): GPIO054 connected to PM_RSMRST 3-4 (Open, Default): GPIO054 connected to EC_SPI_FLASH_CS_L 5-6 (Closed, Default): GPIO055 connected to EC_SPI_FLASH_CS_L
J26	VTR2 - Power Select	1-2 (Default): VTR2 is connected to 1.8V power 2-3: VTR2 is connected to 3.3V power

1.3. Component Description

The EV48H83A development board includes the following integrated circuits:

MEC1753B

Microchip's MEC1753B is a highly configurable, mixed-signal advanced I/O controller designed for desktop and notebook PCs, provided in a 144-pin WFBGA package. The device contains a 32-bit ARM® Cortex-M4F or M4 processor core with closely coupled memory for optimal code execution and data access. This device includes a wide range of security features for authentication, data integrity, data privacy, secure boot, root-of-trust and a NIST-certified true random number generator. It also supports Post Quantum Computing (PQC) algorithms for authentication and secure boot.

MCP2200

Microchip's MCP2200, in a 20-pin UDFN package, converts a USB signal to UART to facilitate communication with the MEC1753B embedded controller. The device communicates through a USB 2.1 interface.

MCP1826S

The development board includes two Microchip MCP1826S low drop-out (LDO) regulators. The MCP1826S/3.3V generates a 3.3V supply from the USB 5.0V input. The MCP1826S/1.8V generates a 1.8V supply from the output of the 3.3V LDO.

GD25LR512MFFIR

The development board includes a socketed Gigadevice GD25LR512MFFIR 512 Mbit QSPI memory device, capable of operating at a 1.8V supply. The socketed interface allows users to select the memory supplier of their choice. The J26 jumper controls the VTR2 power rail, enabling the memory device to operate at either 1.8V or 3.3V.

© 2026 Microchip Technology Inc. and its subsidiaries

> **⚠ CAUTION** If the memory is switched, it is the user's responsibility to validate the operating voltage of the selected device and set the J26 jumper accordingly.

1.4. Connectors

Connectors and headers on the board are divided between those needed for the Meteor Lake Reference Validation Platform (RVP) connections and those provided by Microchip to program or observe signals on the evaluation board. For a detailed understanding of the connections, please refer to the EV48H83A validation board schematics available on MyMicrochip.

Meteor Lake RVP Connectors

P2 - 240-Pin Expansion Connector: Defined by Intel, this connector serves as the primary interface between the MEC1753B embedded controller and the Intel RVP.

J3 - KSO Keyboard Connector: An 18-pin FFC/FPC connector specified by Intel, used to connect the board to the RVP platform. This interface provides a direct connection between the MEC1753B and the Windows keyboard interface.

J7 - KSI Keyboard Connector: An 8-pin FFC/FPC connector specified by Intel, used to connect the board to the RVP platform. This interface provides a direct connection between the MEC1753B and the Windows keyboard interface.

Additional Connectors

P1 - USB Connector: The micro USB connector supplies power to the board and communicates with the MCP2200 USB-to-UART converter.

J1 - JTAG Connector: The 20-pin JTAG connector provides a configuration and programming interface for the MEC1753B embedded controller. The device can be configured using Microchip's MPLAB® X IDE or IPE.

J2 - SF100 Dediprog Header: The 8-pin SF100 Dediprog header allows users to flash a firmware image into the onboard QSPI memory.

J4 - Software Developer Interface: The 6-pin header can be used to assist in setting up and validating some of the features of the evaluation board.

J6 - eSPI Probe Header: The eSPI probe header enables monitoring and communication between the eSPI interface and the MEC1753B embedded controller.

J10 - Power Sequence Header: The power sequence header allows users to observe the relative timing of signals associated with the board's power ramp-up sequence.

© 2026 Microchip Technology Inc. and its subsidiaries

2. Collateral

The following references may be useful in developing applications for the EV48H83A MEC1753B evaluation board.

Kit Information:

- Ordering Code - EV48H83A
- EV48H83A Kit web page

Device Web Pages:

- MEC1753B - Embedded controller and keyboard interface for notebook and desktop computers
- MCP2200 - USB to UART protocol converter
- GD25LR512MF - Gigadevice 512 Mb QSPI memory

Intel Meteor Lake RVP Documentation:

- Intel Meteor Lake Technical Documentation
- Intel Document #646710 – Meteor Lake P DDR5 SODIMM RVP Schematic package (Contact Intel for access)

Software Support:

- MPLAB®X - Version 6.20 or higher - Microchip Integrated Design Environment
- MEC165xB/MEC175xB Blinking LEDs Sample Code on MyMicrochip SDE Portal
- Intel Zephyr EC Firmware (Contact your MCHP representative for more information)

Hardware Debuggers:

- Microchip DV164055 ICD5 In-Circuit Debugger
- Microchip PG164150 MPLAB® PICkit™ 5 In-Circuit Debugger
- Microchip AC102015 Target Adapter Board
- Keil ULINK2 Debug Adapter

© 2026 Microchip Technology Inc. and its subsidiaries

3. Board Programming

The following section provides an overview of programming the various features of the EV48H83A evaluation board. For comprehensive instructions, please refer to the resources available on MyMicrochip and the Secure Document Extranet (SDE) for the MEC1753B. Please note that access to these resources requires a Non-Disclosure Agreement (NDA).

MEC1753B SPI Image Generation

Before operating the board for a specific application, an image defining the device and board operation must be generated. This can be accomplished using Microchip's PC-based image generation tool, which is compatible with both Windows x64 and Linux x64 operating systems. The generated customer image can then be programmed into the onboard QSPI memory using the SF100 DediProg programmer.

Note: For initial verification, a predefined image is preloaded on the board that flashes LED2 and LED3.

Programming the On-board QSPI memory

The onboard QSPI memory can be loaded with an image via the J2 DediProg header, which is compatible with the SF100 SPI Nor Flash DediProg programmer. After loading the image, it is recommended to verify that the MEC1753B boots correctly before configuring the device.

Configuring the MEC1753B

The MEC1753B includes a set of One-Time-Programmable (OTP) registers. Microchip's OTP generator tool must be used to define the configuration image. The actual image generated will be based on the customers requirements for configuring the device. Once defined, the registers can be programmed through the J1 JTAG header using Microchip's MPLAB® X Integrated Development Environment (IDE) and one of Microchip's debuggers, such as the ICD5 or the PICkit™ 5. Alternately, the Keil ULINK2 debug adapter or other supported tools may be used.

⚠ WARNING The OTP registers cannot be programmed unless a bootable image is already installed on the device. OTP bits can only be set to a "1" value once, and once programmed, the configuration cannot be altered.

© 2026 Microchip Technology Inc. and its subsidiaries

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-2612-8

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

© 2026 Microchip Technology Inc. and its subsidiaries

Product Page Links

MEC1753B

© 2026 Microchip Technology Inc. and its subsidiaries