

PE4312

Product Specification

UltraCMOS® RF Digital Step Attenuator, 1 MHz–4 GHz



Features

- Attenuation: 0.5 dB steps to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy:
 - $\pm(0.10 + 1\% \times \text{attenuation})$ at 1 GHz
 - $\pm(0.15 + 2\% \times \text{attenuation})$ at 2.2 GHz
 - $\pm(0.15 + 8\% \times \text{attenuation})$ at 4 GHz
- High linearity: +59 dBm IIP3
- Wide power supply range: 2.3–5.5V
- 1.8V control logic compatible
- Operating temperature: 105 °C
- Programming modes:
 - Direct parallel
 - Latched parallel
 - Serial
- Unique power-up state selection
- Pin compatible with the PE4302, PE4305, and PE4306
- Package: 20-lead 4 × 4 mm QFN

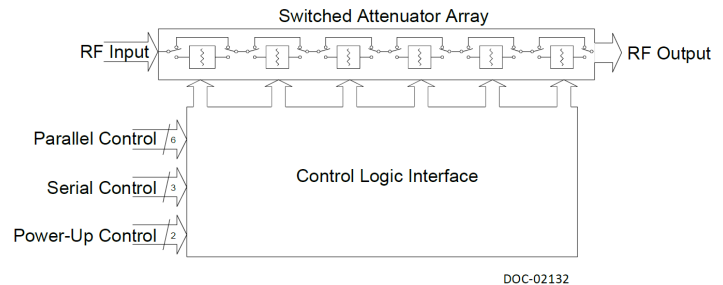


Figure 1. PE4312 functional diagram

Product description

The PE4312 is a 50Ω, HaRP technology-enhanced 6-bit RF digital step attenuator (DSA) designed for use in 3G/4G wireless infrastructure and other high-performance RF applications.

This DSA is a pin-compatible and upgraded version of the PE4302 with higher linearity, improved attenuation accuracy, and faster switching speed. An integrated digital control interface supports both serial and parallel programming of the attenuation, including the capability to program an initial attenuation state at power-up.

Covering a 31.5 dB attenuation range in 0.5 dB steps, the DSA maintains high linearity and low power consumption from 1 MHz through 4 GHz. The PE4312 also features an external negative supply option and is offered in a 20-lead 4 × 4 mm QFN package. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE4312 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. Absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage	V_{CTRL}	-0.3	3.6	V
Maximum input power	P_{MAX_ABS}	–	+30	dBm
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM, all pins ⁽¹⁾	$V_{ESD,HBM}$	–	1500	V
ESD voltage CDM, all pins ⁽²⁾	$V_{ESD,CDM}$	–	250	V
Notes: 1. Human Body Model (MIL-STD-883 Method 3015) 2. Charged device model (JEDEC JESD22-C101)				

Recommended operating conditions

Table 2 lists the PE4312 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. Operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Normal mode⁽¹⁾					
Supply voltage	V_{DD}	2.3	–	5.5	V
Supply current	I_{DD}	–	130	200	μA
Bypass mode⁽²⁾					
Supply voltage	V_{DD}	2.7	–	5.5	V
Supply current	I_{DD}	–	50	60	μA
Negative supply voltage	V_{SS_EXT}	-3.6	–	-3.2	V
Negative supply current	I_{SS}	-40	-16	–	μA
Normal or bypass mode					
Digital input high	–	1.17	–	3.6	V
Digital input low	–	-0.3	–	0.6	V
Digital input leakage ⁽³⁾	–	–	–	20	μA
RF input power, CW - 1–50 MHz - >50 MHz–4 GHz	P_{MAX_CW}	–	–	See Figure 4 +24	dBm
RF input power, pulsed ⁽⁴⁾ - 1–50 MHz - >50 MHz–4 GHz	P_{MAX_PULSED}	–	–	See Figure 4 +27	dBm
Operating temperature range	T_{OP}	-55	–	+105	°C
Notes: 1. Normal mode: Connect pin 12 to GND to enable the internal negative voltage generator. 2. Bypass mode: Apply a negative voltage to V_{SS_EXT} (pin 12) to bypass and disable the internal negative voltage generator. 3. Applies to all pins except 1, 5, 7, and 20. Pins 1, 7, and 20 have an internal pull-down resistor and pin 5 has an internal pull-up resistor. 4. Pulsed, 5% duty cycle of 4620- μs period, 50 Ω .					

Electrical specifications

Table 3 lists the PE4312 key electrical specifications at +25 °C ($Z_S = Z_L = 50\Omega$), unless otherwise specified.

- Normal mode⁽¹⁾: $V_{DD} = 3.3V$, $V_{SS_EXT} = 0V$
- Bypass mode⁽²⁾: $V_{DD} = 3.3V$, $V_{SS_EXT} = -3.3V$

Table 3. Electrical specifications

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency	–	–	1	–	4000	MHz
Attenuation range	0.5 dB step	–	–	0–31.5	–	dB
Insertion loss	–	1 MHz–<1 GHz 1–2.2 GHz 2.2–4 GHz	–	1.3 1.5 2.1	1.5 1.8 2.3	dB
Attenuation error	Any bit or bit combination	1 MHz–1 GHz 1–<2.2 GHz 2.2–4 GHz	–	–	$\pm(0.10 + 1\% \text{ of atten setting})$ $\pm(0.15 + 2\% \text{ of atten setting})$ $\pm(0.15 + 8\% \text{ of atten setting})$	dB
Return loss (input or output port)	–	1–2.2 GHz 2.2–4 GHz	14 10	18 17	–	dB
Input 0.1-dB compression point ⁽³⁾	–	1 MHz–4 GHz	–	30	–	dBm
Input IP3	Two tones at +18 dBm, 10 kHz spacing	1950 MHz	–	59	–	dBm
Switching time	50% CTRL to 90% or 10% RF	–	–	500	800	ns

Notes:

1. Normal mode: Single external positive supply used.
2. Bypass mode: Both external positive supply and external negative supply used.
3. The input 0.1-dB compression point is a linearity figure of merit. For the operating RF input power (50Ω), see [Table 2](#).

Safe attenuation state transitions

The PE4312 features a novel architecture to provide safe transition behavior when changing attenuation states. When RF input power is applied, positive output power spikes are prevented during attenuation state changes by optimized internal timing control.

Resistors on pins 1 and 3

A 10-kΩ resistor on the inputs to pin 1 and 3 (see [Figure 24](#)) eliminates the package resonance between the RF input pin and the two digital inputs. The specified attenuation error versus frequency performance depends upon this condition.

Spurious performance

The PE4312 typical low-frequency spurious performance in normal mode is -140 dBm (pin 12 = GND). For spur-free performance, disable the internal negative voltage generator by applying a negative voltage to V_{SS_EXT} (pin 12).

Programming options

Parallel/serial selection

Use a parallel or serial interface to control the PE4312 using the P/S bit. P/S = LOW selects the parallel interface and P/S = HIGH selects the serial interface.

Parallel mode interface

The parallel interface consists of six CMOS-compatible control lines that select the preferred attenuation state, as listed in Table 4.

The parallel interface timing requirements are defined by [Figure 2](#) (the parallel interface timing diagram), [Table 7](#) (the parallel interface AC characteristics), and the switching speed ([Table 3](#)).

For latched parallel programming, the Latch Enable (LE) must be held LOW while changing the attenuation state control values, then pulse LE HIGH to LOW (per [Figure 2](#)) to latch the new attenuation state into the device.

For direct parallel programming, the Latch Enable (LE) line must be pulled HIGH. Changing the attenuation state control values changes the device state to the new attenuation. Direct Mode is ideal for manual control of the device using hardwire, switches, or jumpers.

Table 4. Truth table^(*)

P/S	C16	C8	C4	C2	C1	C0.5	Attenuation state
0	0	0	0	0	0	0	Reference loss
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB
Note: * This table does not show all 64 possible C0.5–C16 combinations.							

Serial interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input must then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by [Figure 3](#) (the serial interface timing diagram) and [Table 8](#) (the serial interface AC characteristics).

Power-up control settings

The PE4312 always assumes a specifiable attenuation setting on power-up. This feature exists for both serial and parallel modes of operation and establishes a known attenuation state before an initial serial or parallel control word is provided.

When the attenuator powers up in serial mode ($P/S = 1$), the six control bits are set to whatever data is present on the six parallel data inputs (C0.5 to C16). This specifies any one of the 64 attenuation settings as the power-up state.

When the attenuator powers up in parallel mode ($P/S = 0$) with $LE = 0$, the control bits are automatically set to one of four possible values. The two power-up control bits, PUP1 and PUP2, select these four values, as listed in [Table 5](#).

Table 5. Parallel power-up (PUP) truth table(*)

P/S	LE	PUP2	PUP1	Attenuation state
0	0	0	0	Reference loss
0	0	1	0	8 dB
0	0	0	1	16 dB
0	0	1	1	31.5 dB
0	1	X	X	Defined by C0.5–C16

Note: * Power up with $LE = 1$ provides normal parallel operation with C0.5–C16, and PUP1 and PUP2 are not active.

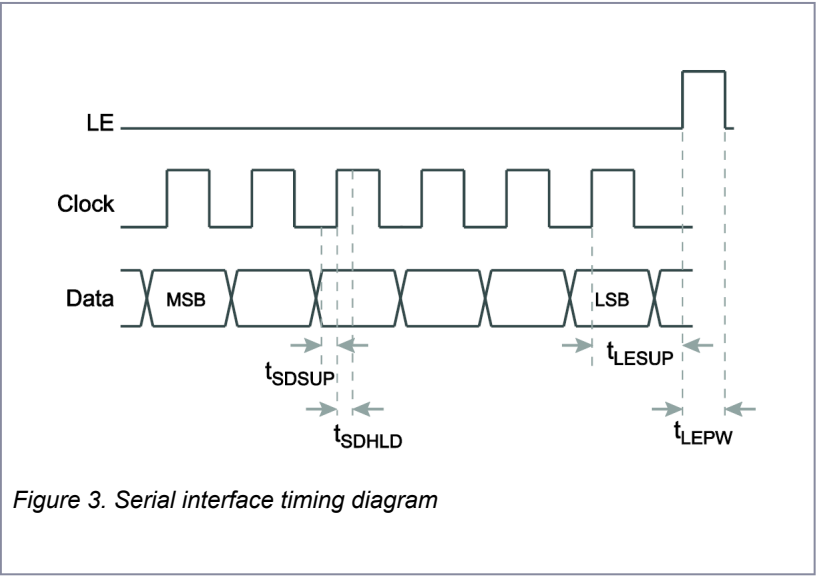
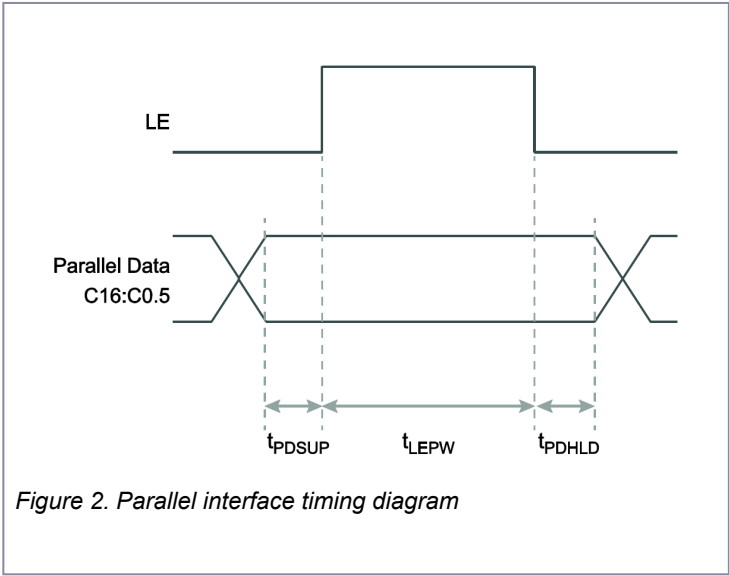


Table 6. Six-bit attenuator serial programming register map

B5	B4	B3	B3	B1	B0
C16	C8	C4	C2	C1	C0.5
↑ MSB (first in)	—				↑ LSB (last in)

Table 7. Parallel interface AC characteristics

Table 7 lists the parallel interface AC characteristics at $V_{DD} = 3.3V$ and $-55^{\circ}C < T_A < 105^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Min	Max	Unit
LE minimum pulse width	t_{LEPW}	10	—	ns
Data set-up time before rising edge of LE	t_{PDSUP}	10	—	ns
Data hold time after falling edge of LE	t_{PDHLD}	10	—	ns

Table 8. Serial interface AC characteristics

Table 8 lists the serial interface AC characteristics at $V_{DD} = 3.3V$ and $-55^{\circ}C < T_A < 105^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Min	Max	Unit
Serial data clock frequency ^(*)	f_{CLK}	—	10	MHz
Serial clock HIGH time	t_{CLKH}	30	—	ns
Serial clock LOW time	t_{CLKL}	30	—	ns
LE set-up time after last clock rising edge	t_{LESUP}	10	—	ns
LE minimum pulse width	t_{LEPW}	30	—	ns
Serial data set-up time before clock rising edge	t_{SDSUP}	10	—	ns
Serial data hold time after clock rising edge	t_{SDHLD}	10	—	ns
Note: * f_{CLK} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify the f_{CLK} specification.				

Power derating curve

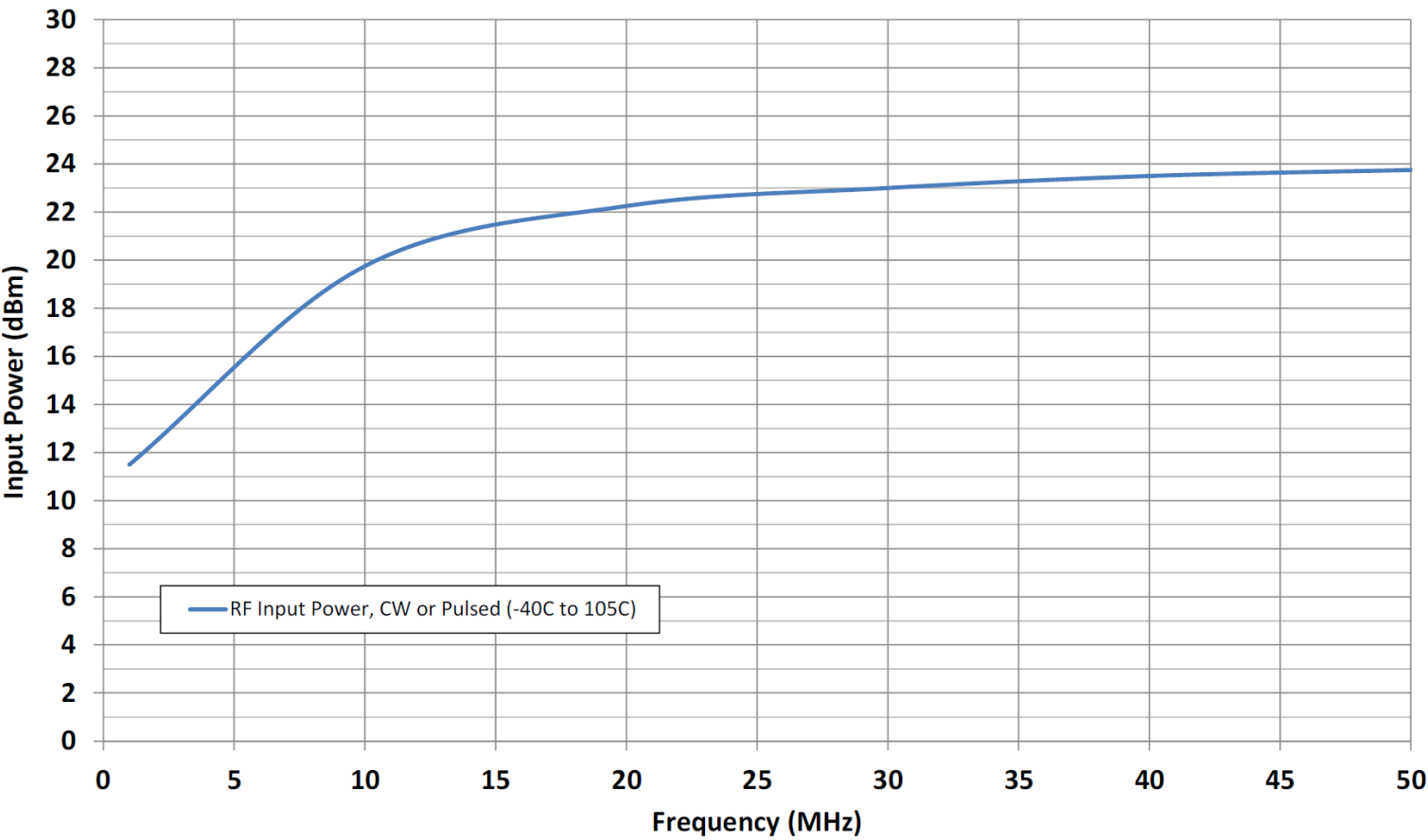
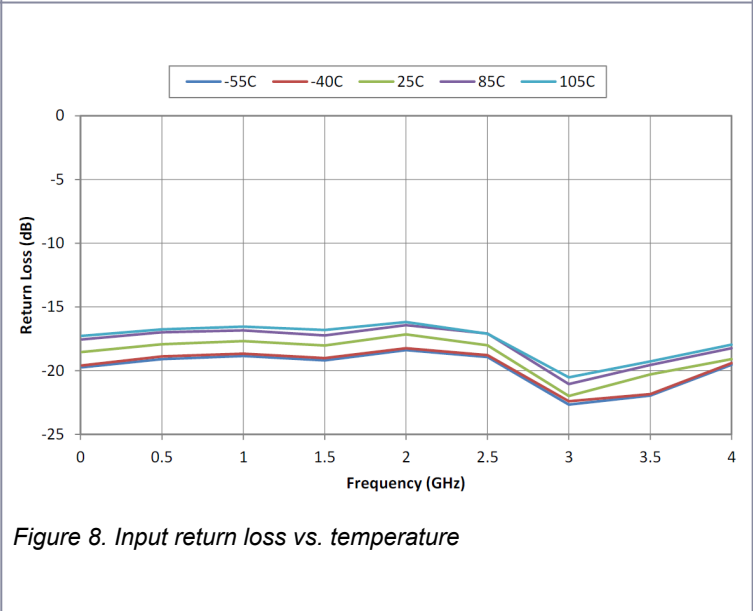
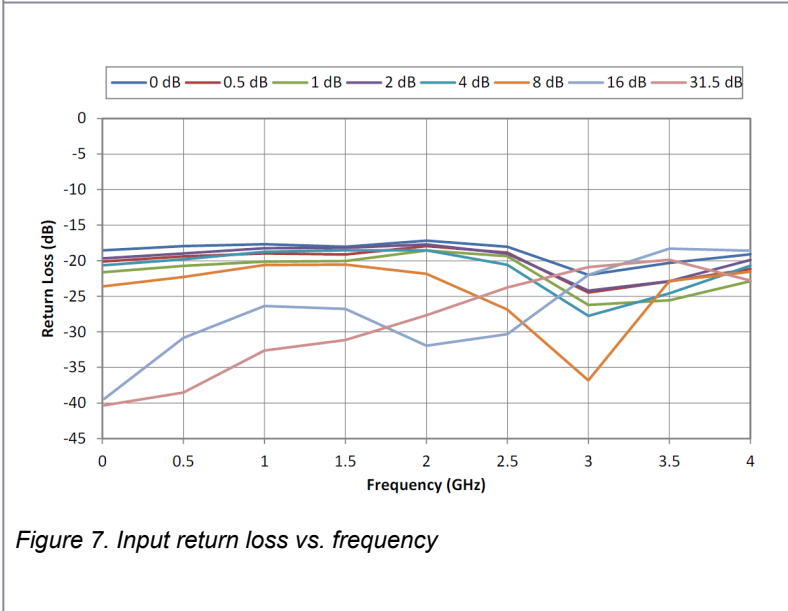
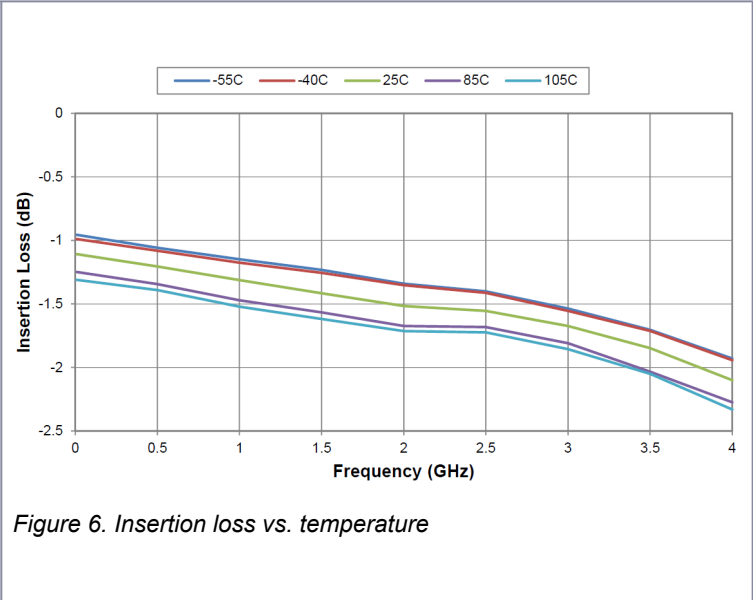
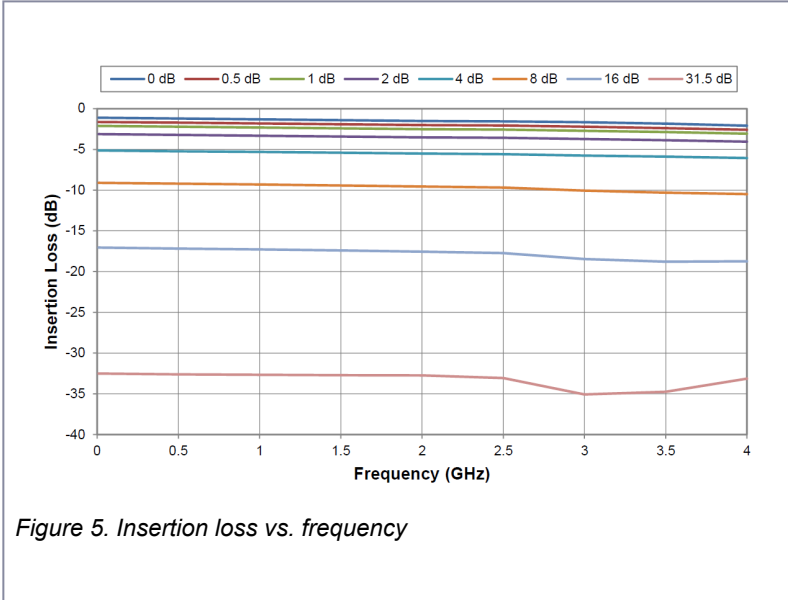


Figure 4. Power derating curve for 1–50 MHz

Typical performance data

Figure 5–Figure 21 how the typical performance data at +25 °C and $V_{DD} = 3.3V$, unless otherwise specified.



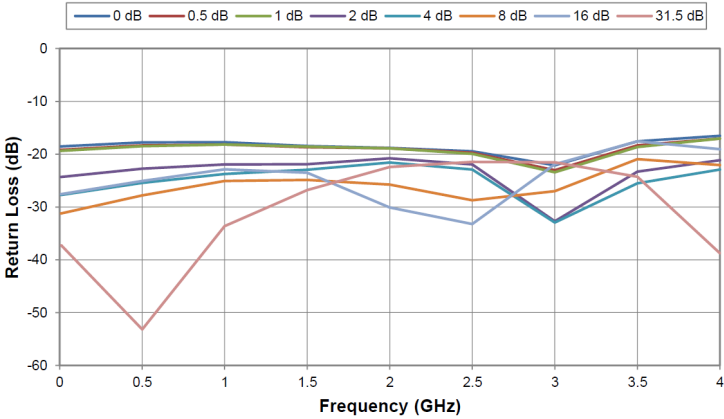


Figure 9. Input return loss vs. frequency at major attenuation steps

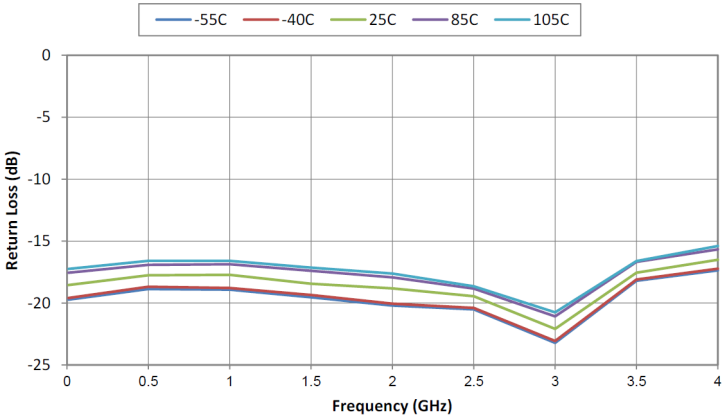


Figure 10. Output return loss vs. temperature

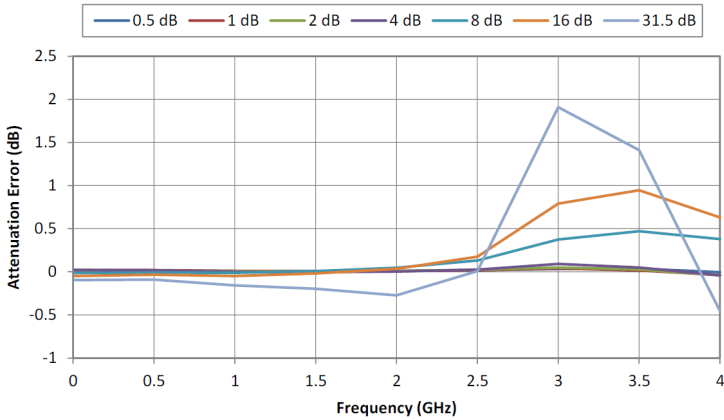


Figure 11. Attenuation error vs. frequency

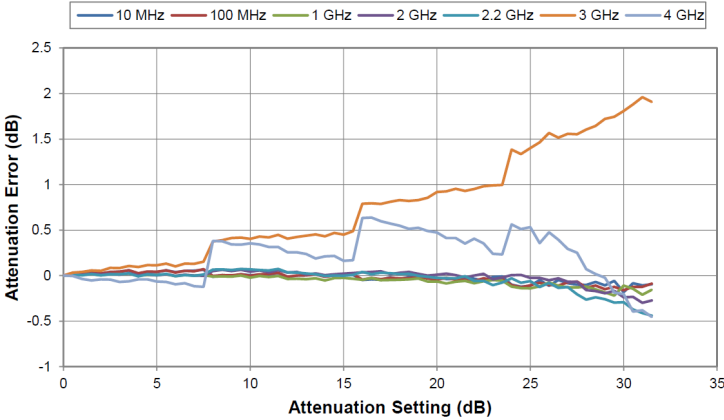


Figure 12. Attenuation error vs. attenuation setting

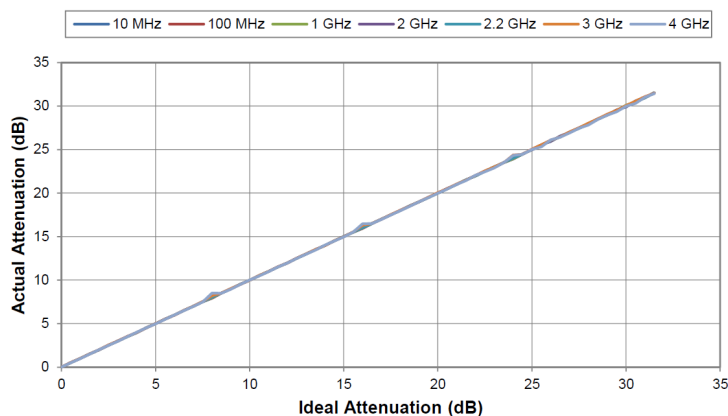


Figure 13. Actual attenuation vs. ideal attenuation

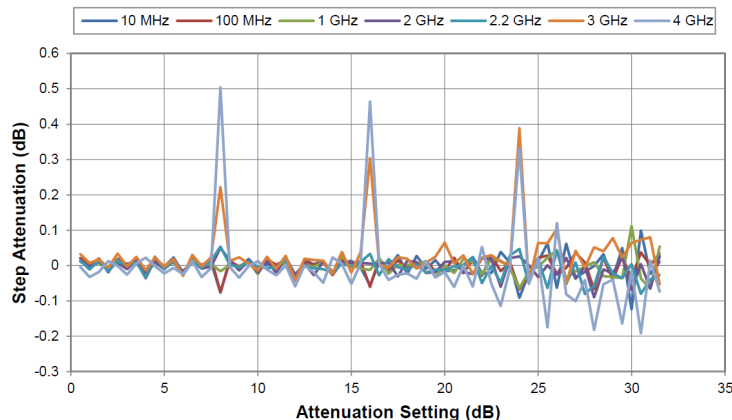


Figure 14. 0.5-dB step attenuation vs. attenuation(*)

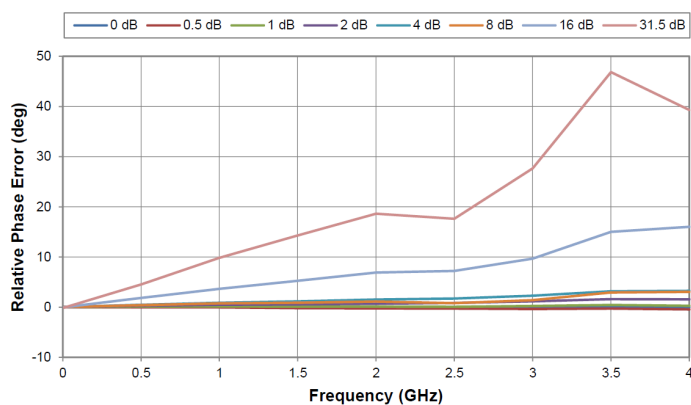


Figure 15. Relative phase error vs. frequency at major attenuation steps

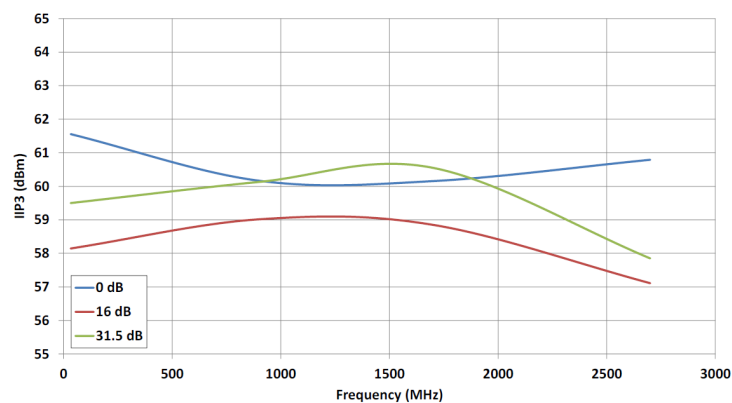


Figure 16. IIP3 vs frequency

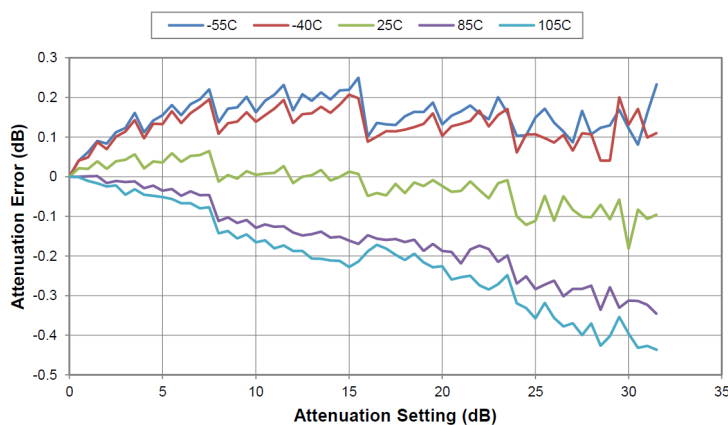


Figure 17. Attenuation error at 10 MHz vs. temperature

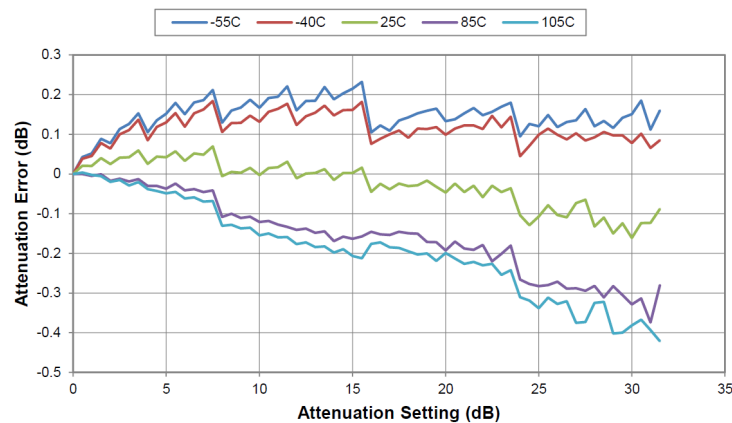


Figure 18. Attenuation error at 100 MHz vs. temperature

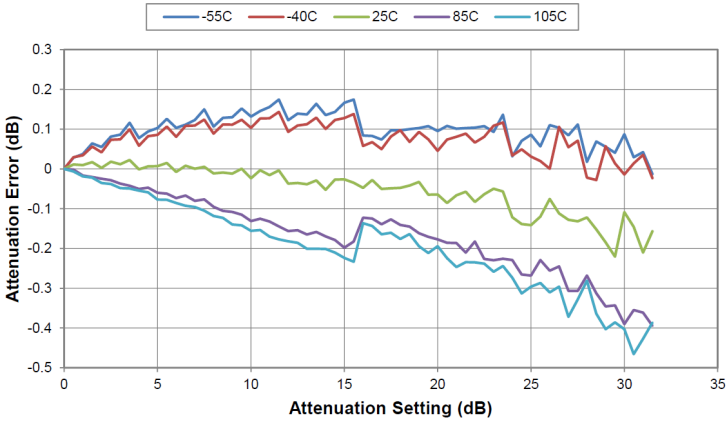


Figure 19. Attenuation error at 1 GHz vs. temperature

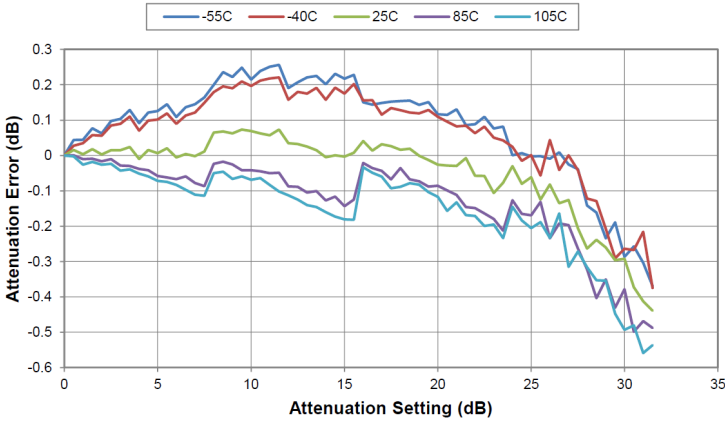


Figure 20. Attenuation error at 2.2 GHz vs. temperature

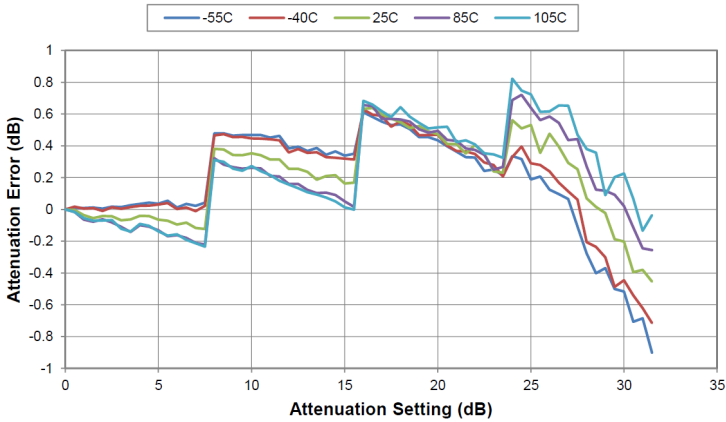


Figure 21. Attenuation error at 4 GHz vs. temperature

Note: * Monotonicity is held as long as step attenuation does not decrease below -0.5 dB.

Evaluation kit

pSemi designed the DSA evaluation board (EVB) to ease your evaluation of the PE4312. The EVB supports direct parallel, latched parallel, and serial programming modes.

Evaluation kit setup

Connect the EVB with the USB dongle board and USB cable, as shown in Figure 22.

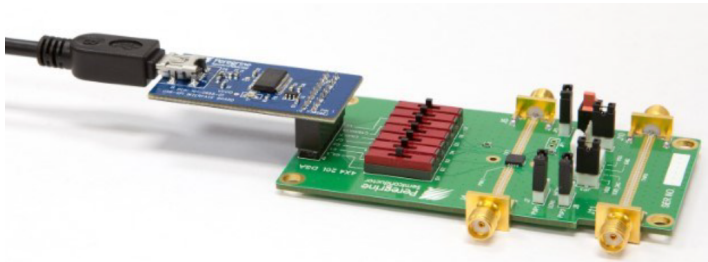
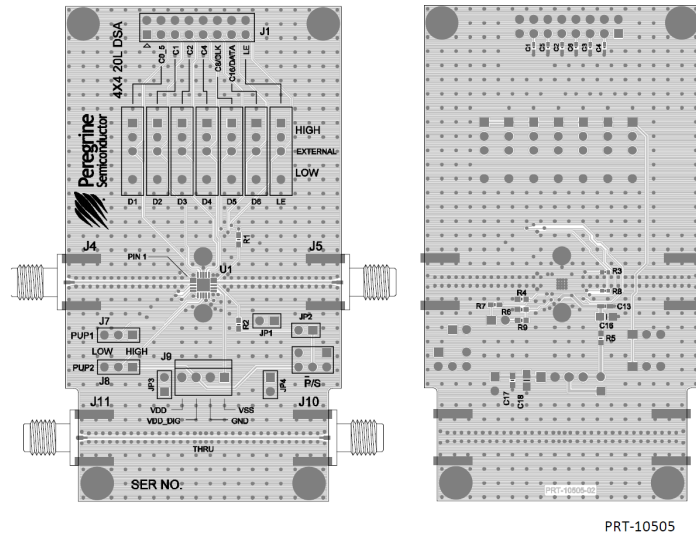


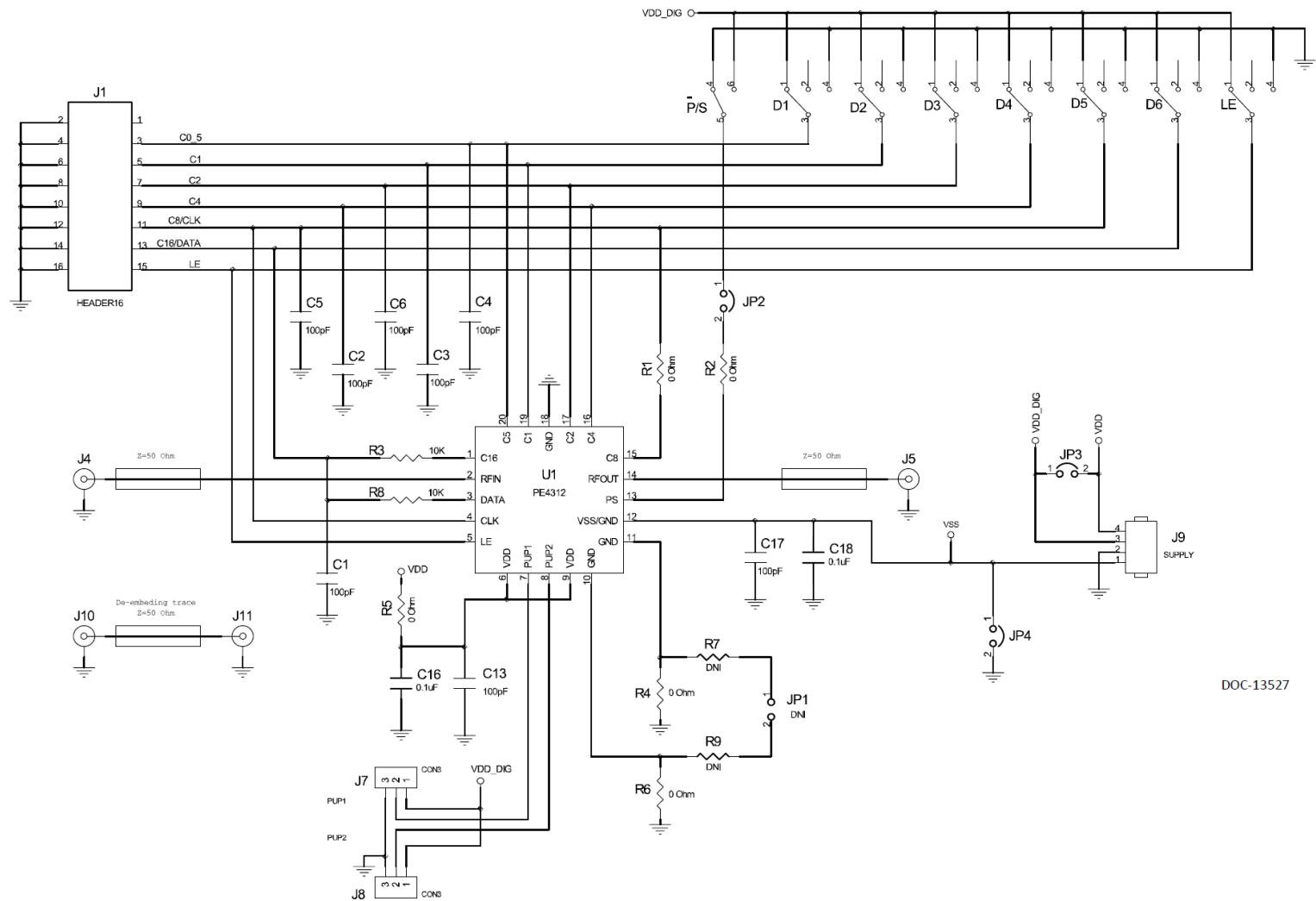
Figure 22. USB dongle board and cable

Direct parallel programming procedure

Direct parallel programming is suitable for manual operation without software programming. For manual direct parallel programming, position the Parallel/Serial (P/S) select switch to the Parallel (or left) position. The LE mechanical programming switch must be set to the HIGH position. Switches D1–D6 are SP3T switches that allow you to manually program the parallel bits. When D1–D6 are toggled to the HIGH position, logic high is presented to the parallel input. When toggled to the LOW position, logic low is presented to the parallel input. Setting D1–D6 to the EXTERNAL position presents as OPEN, which is set for software programming of latched parallel and serial mode. Table 4 lists the parallel programming truth table.



Evaluation board schematic



DOC-13527

- Notes:
- 1. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).
 - 2. Install shunt connector on JP2, JP3 and JP4.

Figure 24. Evaluation board schematic

Pin configuration

Figure 25 shows the PE4312 pin configuration for the 20-lead 4 × 4 mm QFN package, and Table 9 lists the description for each pin.

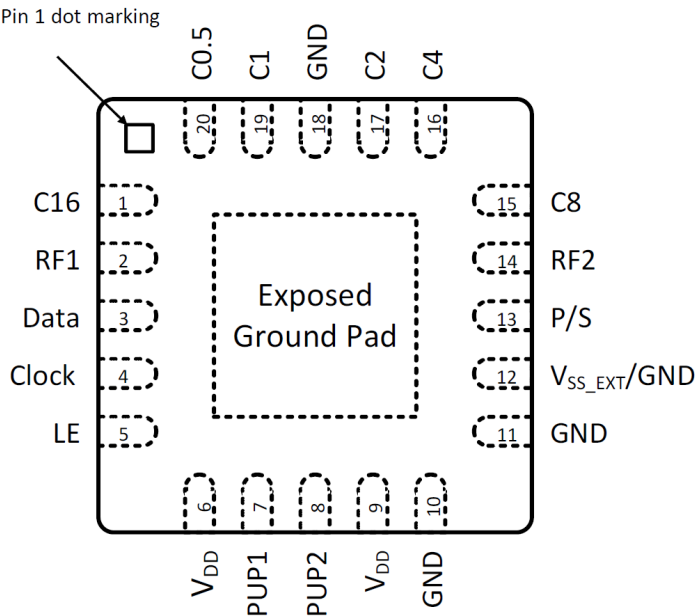


Figure 25. Pin configuration, top view

Table 9. Pin descriptions

Pin no.	Pin name	Description
1	C16 ⁽¹⁾⁽²⁾	Attenuation control bit, 16 dB
2	RF1 ⁽³⁾	RF1 port (RF input)
3	Data ⁽¹⁾	Serial interface data input
4	Clock	Serial interface clock input
5	LE ⁽⁴⁾	Latch Enable input
6	V _{DD}	Supply voltage (nominal 3.3V)

Pin no.	Pin name	Description
7	PUP1 ⁽²⁾	Power-up selection bit 1
8	PUP2	Power-up selection bit 2
9	V _{DD}	Supply voltage (nominal 3.3V)
10, 11, 18	GND	Ground
12	V _{SS_EXT} / GND ⁽⁵⁾	External V _{SS} negative voltage control or ground
13	P/S	Parallel/Serial mode select
14	RF2 ⁽³⁾	RF2 port (RF output)
15	C8	Attenuation control bit, 8 dB
16	C4	Attenuation control bit, 4 dB
17	C2	Attenuation control bit, 2 dB
19	C1	Attenuation control bit, 1 dB
20	C0.5 ⁽²⁾	Attenuation control bit, 0.5 dB
Pad	GND	Exposed pad. Ground for proper operation.

- Notes:
1. Place a 10-kΩ resistor in series, as close to pin as possible, to avoid frequency resonance.
 2. This pin has an internal 200-kΩ resistor to GND.
 3. RF pins 2 and 14 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
 4. This pin has an internal 2-MΩ resistor to the internal positive digital supply.
 5. Use V_{SS_EXT} (pin 12, see [Table 2](#)) to bypass and disable the internal negative voltage generator. Connect V_{SS_EXT} (pin 12, V_{SS_EXT} = GND) to enable the internal negative voltage generator.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE4312 moisture sensitivity level rating for the 20-lead 4 × 4 mm QFN package is MSL1.

Package drawing

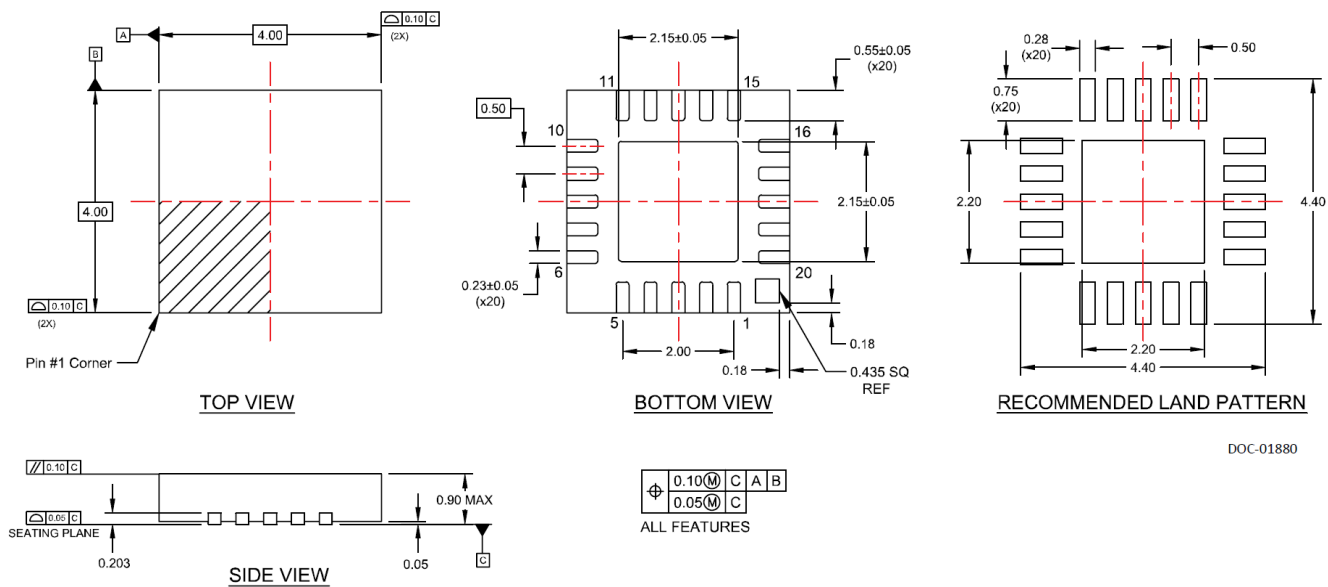
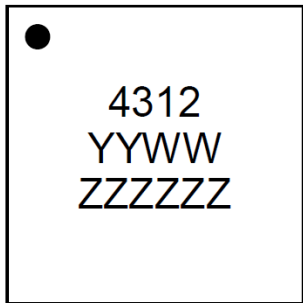


Figure 26. Package mechanical drawing for the 20-lead 4 × 4 mm QFN package

Top-marking specification



DOC-65736

- = Pin 1 designator
- YYWW = Date code, last two digits of the year and work week
- ZZZZZZ = Assembly lot code (max 6 characters)

Figure 27. Package marking specification



1. 10 sprocket hole pitch cumulative tolerance $\pm .02$.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

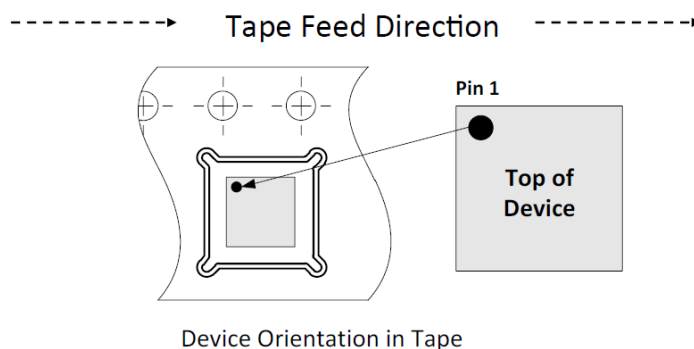


Figure 28. Tape and reel specification for the 20-lead 4 × 4 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE4312C-Z	PE4312 digital step attenuator	Green 20-lead 4 × 4 mm QFN	3000 units/T&R
EK4312-13	PE4312 evaluation kit	Evaluation kit	1/box

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