A Product Line of
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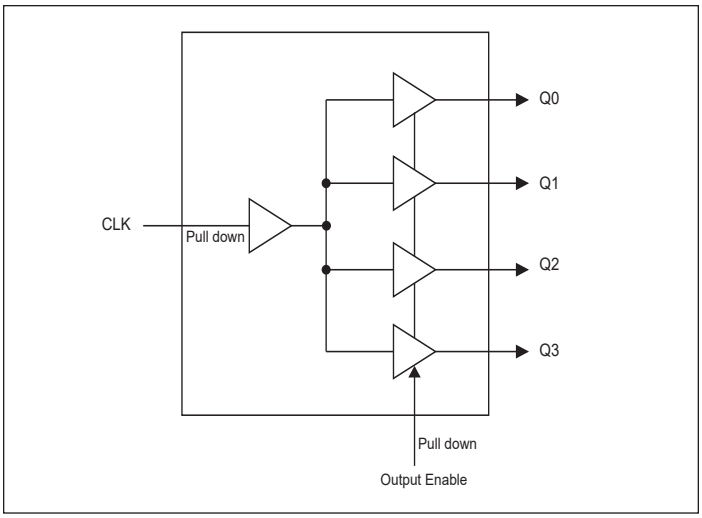
PI6C39X1104

Low Skew 1 to 4 Clock Buffer

Description

The PI6C39X1104 is a low skew, low additive jitter single input to four output clock buffer.

Block Diagram



Features

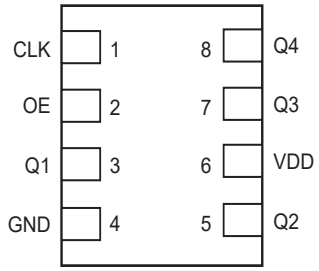
- Low Skew Outputs (50ps)
- Low Additive Jitter RMS: <55fs
- Input/Output Frequency up to 250MHz
- Operating Voltages of 1.5V to 3.3V
- Output Enable Pin Tri-states Outputs
- 3.3V Tolerant Input Clock
- Extended Temperature Range: -40°C to 105°C
- Packaging (Pb-free & Green):
  - 8-pin, X1DFN (XEC)
  - 8-pin, TSSOP (L)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Pin Configuration

8-X1DEN (XEC)/8-TSSOP (L)



Pin Descriptions

8-X1DEN (XEC)/8-TSSOP (L)

Pin Number	Pin Name	Type	Pin Description
1	CLK	Input	Single-ended clock input with internal 300kΩ (typical) pulldown resistor to GND. PDT.
2	OE	Input	Output Enable with internal 300kΩ (typical) pulldown resistor to GND. Typically connected to VDD with external pullup resistor. PDT. HIGH: outputs enabled LOW: outputs disabled
3	Q1	Output	Clock Output 1.
4	GND	Power	Connect to ground.
5	Q2	Output	Clock Output 2.
6	VDD	Power	Connect to 1.5V, 1.8V, 2.5V or 3.3V.
7	Q3	Output	Clock Output 3.
8	Q4	Output	Clock Output 4.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD and GND, as close to the device as possible.

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Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage (VDD) 4.6V
All Outputs . . . . . -0.5V to VDD+0.5V
Output Enable and CLK . . . . . -0.5V to 3.6V (VDD > 0)
Storage Temperature . . . . . -65 to +150°C
Junction Temperature . . . . . 125°C max
ESD Protection (HBM) 2000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (Extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.425		+3.465	V

Thermal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
θJA	Thermal Resistance Junction to Ambient	Still air		157		°C/W
θJC	Thermal Resistance Junction to Case			42		°C/W

DC Electrical Characteristics

VDD = 1.5V±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		1.425	1.5	1.575	V
V_{IH}	Input High Voltage(1)	CLK, OE	0.7xVDD		VDD	V
V_{IL}	Input Low Voltage(1)	CLK, OE			0.3xVDD	V
I_{IH}	Input High Current	CLK, OE	-1		1	µA
I_{IL}	Input Low Current	CLK, OE	-40			µA
V_{OH}	Output High Voltage	I_{OH} = -3mA	0.95			V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.45	V
IDD	Operating Supply Current	100MHz, no load		11	13	mA
		100MHz, 5pf load, 5inch trace		20	23	
Z_O	Nominal Output Impedance			55		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF
I_{STB}	Output Disable Supply Current	CLK = 0, OE = 0 or NC			5	uA
	Standby Current	CLK = 0, OE = 1			15	uA

Notes:
1. Nominal switching threshold is VDD/2.

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VDD = 1.8V±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		1.7	1.8	1.89	V
V_{IH}	Input High Voltage(1)	CLK, OE	0.7xVDD		VDD	V
V_{IL}	Input Low Voltage(1)	CLK, OE			0.3xVDD	V
I_{IH}	Input High Current	CLK, OE	-1		1	µA
I_{IL}	Input Low Current	CLK, OE	-40			µA
V_{OH}	Output High Voltage	I_{OH} = -5mA	1.4			V
V_{OL}	Output Low Voltage	I_{OL} = 5mA			0.4	V
IDD	Operating Supply Current	100MHz, no load		12.5	15	mA
		100MHz, 5pf load, 5inch trace		24	28	
Z_O	Nominal Output Impedance			52		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF
I_{STB}	Output Disable Supply Current	CLK = 0, OE = 0 or NC			5	uA
	Standby Current	CLK = 0, OE = 1			15	uA

Notes:
1. Nominal switching threshold is VDD/2.

VDD = 2.5V±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		2.375	2.5	2.625	V
V_{IH}	Input High Voltage(1)	CLK, OE	0.7xVDD		VDD	V
V_{IL}	Input Low Voltage(1)	CLK, OE			0.3xVDD	V
I_{IH}	Input High Current	CLK, OE	-1		1	µA
I_{IL}	Input Low Current	CLK, OE	-60			µA
V_{OH}	Output High Voltage	I_{OH} = -8mA	1.8			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.4	V
IDD	Operating Supply Current	100MHz, no load		18	22	mA
		100MHz, 5pf load, 5inch trace		35	40	
Z_O	Nominal Output Impedance			50		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF
I_{STB}	Output Disable Supply Current	CLK = 0, OE = 0 or NC			5	uA
	Standby Current	CLK = 0, OE = 1			15	uA

Notes:
1. Nominal switching threshold is VDD/2.

VDD = 3.3V±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		3.135	3.3	3.465	V
V_{IH}	Input High Voltage(1)	CLK, OE	0.7xVDD		VDD	V
V_{IL}	Input Low Voltage(1)	CLK, OE			0.3xVDD	V

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	CLK, OE	-1		1	µA
I_{IL}	Input Low Current	CLK, OE	-70			µA
V_{OH}	Output High Voltage	I_{OH} = -12mA	2.2			V
V_{OL}	Output Low Voltage	I_{OL} = 12mA			0.7	V
IDD	Operating Supply Current	100MHz, no load		25	30	mA
		100MHz, 5pf load, 5inch trace		47	54	
Z_O	Nominal Output Impedance			48		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF
I_{STB}	Output Disable Supply Current	CLK = 0, OE = 0 or NC			5	uA
	Standby Current	CLK = 0, OE = 1			20	uA

Notes:
1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics

VDD = 1.5V±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		100	MHz
tOR	Output Rise Time	0.3V to 1.2V		1	1.6	ns
tOF	Output Fall Time	1.2V to 0.3V		1	1.6	ns
T_{PD}	Propagation Delay(1)		2	3	5	ns
T_{SK}	Output to Output Skew(2)	Rising edges at VDD/2		50	65	ps
J_{ADD}	Additive Jitter	@125MHz, 12k to 20MHz			0.055	ps
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t_{EN}	Output Enable Time	C_L < 5pF			3	cycles
t_{DIS}	Output Disable Time	C_L < 5pF			3	cycles
T_{DC}	Duty Cycle	50% Input, at half of the output, 100MHz max	45		55	%

Notes:
1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.

VDD = 1.8V±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		200	MHz
tOR	Output Rise Time	0.36V to 1.44V		0.6	1	ns
tOF	Output Fall Time	1.44V to 0.36V		0.6	1	ns
T_{PD}	Propagation Delay(1)		1.3	2	4	ns
T_{SK}	Output to Output Skew(2)	Rising edges at VDD/2		50	65	ps
J_{ADD}	Additive Jitter	@125MHz, 12k to 20MHz			0.055	ps

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t_{EN}	Output Enable Time	C_L < 5pF			3	cycles
t_{DIS}	Output Disable Time	C_L < 5pF			3	cycles
T_{DC}	Duty Cycle	50% Input, at half of the output, 200MHz max	45		55	%

Notes:
1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.

VDD = 2.5V±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		250	MHz
tOR	Output Rise Time	0.5V to 2V		0.6	1	ns
tOF	Output Fall Time	2V to 0.5V		0.6	1	ns
T_{PD}	Propagation Delay(1)		0.8	1.5	3	ns
T_{SK}	Output to Output Skew(1)	Rising edges at VDD/2		50	65	ps
J_{ADD}	Additive Jitter	@125MHz, 12k to 20MHz			0.055	ps
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t_{EN}	Output Enable Time	C_L < 5pF			3	cycles
t_{DIS}	Output Disable Time	C_L < 5pF			3	cycles
T_{DC}	Duty Cycle	50% Input, at half of the output, 250MHz max	45		55	%

Notes:
1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.

VDD = 3.3V±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		250	MHz
tOR	Output Rise Time	0.66V to 2.64V		0.6	1	ns
tOF	Output Fall Time	2.64V to 0.66V		0.6	1	ns
T_{PD}	Propagation Delay (1)		0.8	1.0	2.5	ns
T_{SK}	Output to Output Skew(2)	Rising edges at VDD/2		50	65	ps
J_{ADD}	Additive Jitter	@125MHz, 12k to 20MHz			0.055	ps
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t_{EN}	Output Enable Time	C_L < 5pF			3	cycles
t_{DIS}	Output Disable Time	C_L < 5pF			3	cycles

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{DC}	Duty Cycle	50% Input, at half of the output, 250MHz max	45		55	%

Notes:
1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.

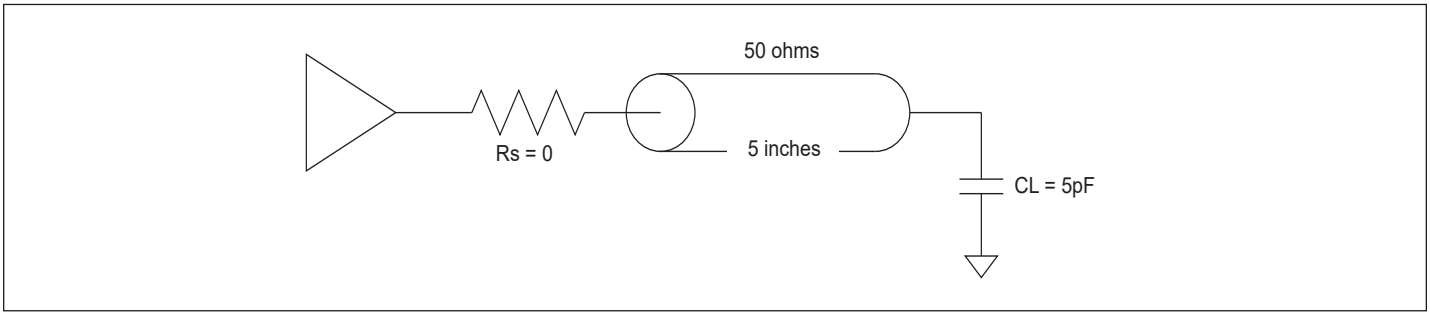
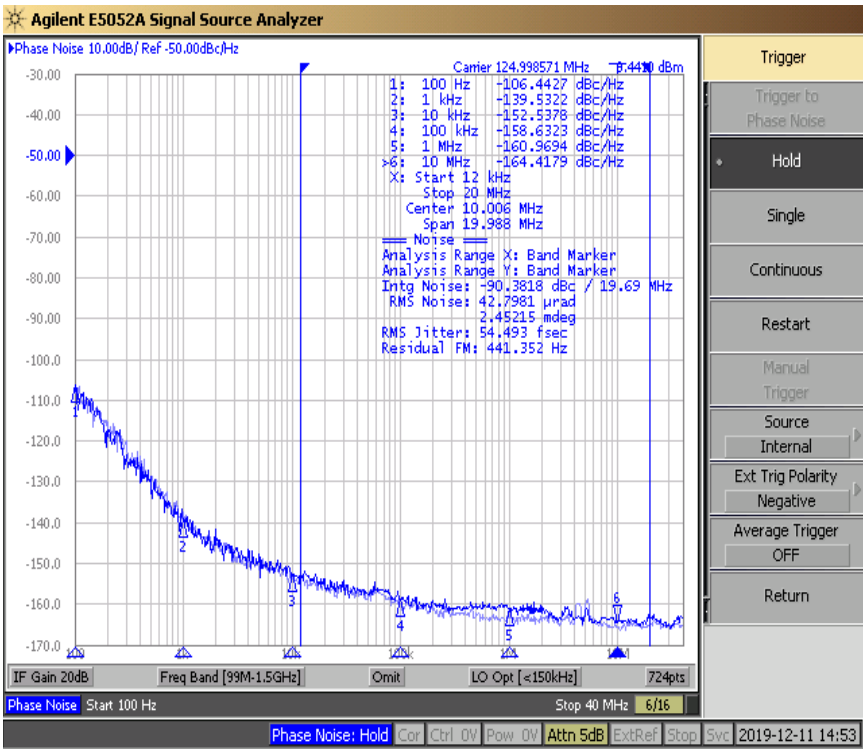


Figure 1. Test Circuit

Additive Phase Noise Plot



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Application Information

Suggest for Unused Inputs and Outputs

LVCMOS Input Control Pins

It is suggested to add pull-up = 4.7k and pull-down = 1k for LVCMOS pins even though they have internal pull-up/down but with much higher value (≥50k) for higher design reliability.

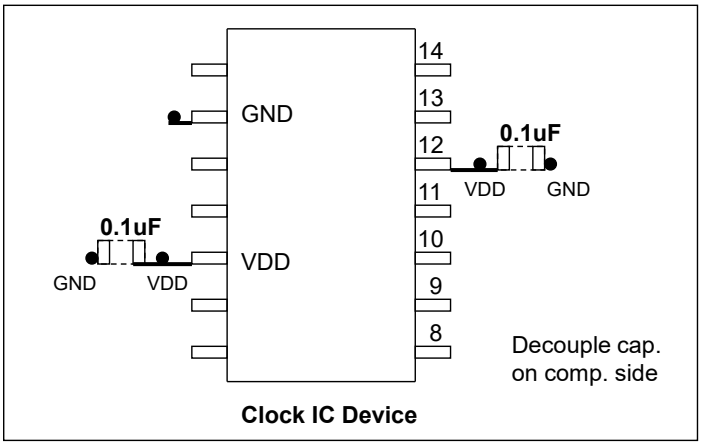
Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power consumption.

Power Decoupling & Routing

VDD Pin Decoupling

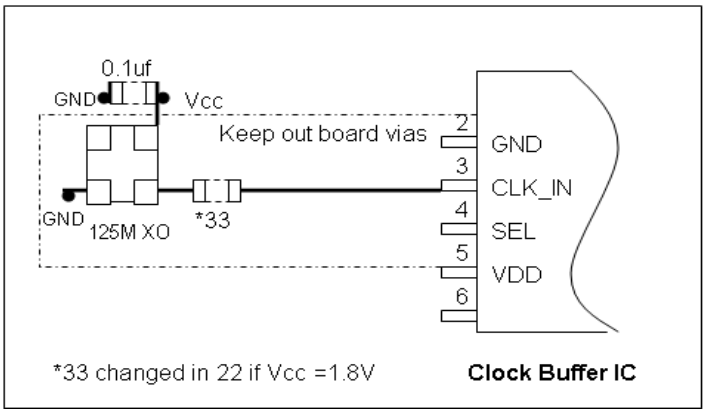
Each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as shown.



Placement of Decoupling Caps

CMOS Clock Trace Routing

Please ensure that there is a sufficient keep-out area to the adjacent trace (>20mil.). In an example using a 125MHz XO driving a buffer IC, it is better to route the clock trace on the component side with a 33Ω termination resistor.

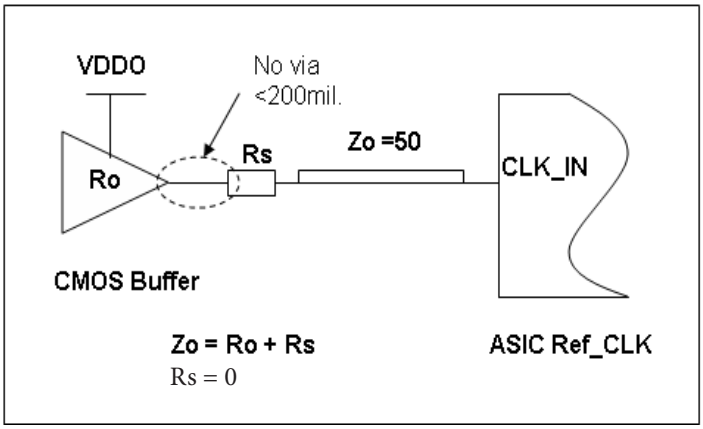


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CMOS Output Termination

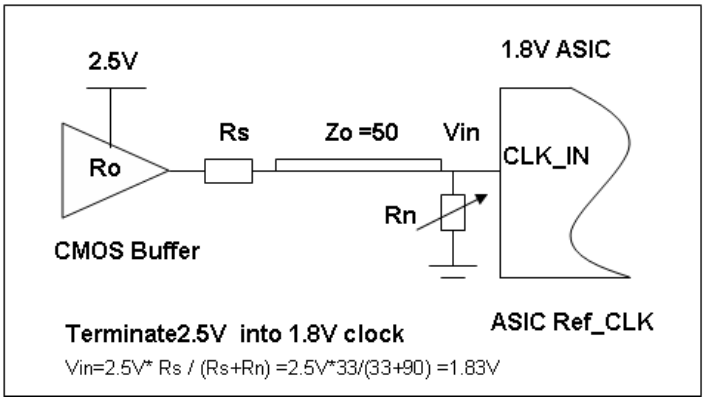
Popular CMOS Output Termination

The most popular CMOS termination is a serial resistor close to the output pin (≤200mil.). It is simple and balances the drive strength. The resistor's value can be fine tuned for best performance during board bring-up based on VDDO voltage used.



Combining Serial and Parallel Termination

Designers can also use a parallel termination for CMOS outputs. For example, a 50Ω pull-down resistor can be used at the Rx side to reduce signal reflection, but it reduces the signals V_swing in half. This pull-down can be combined with a serial resistor to form a smaller clock voltage difference. The following diagram shows how to transition a 2.5V clock into 1.8V clock.



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Clock Jitter Definitions

Total Jitter = RJ + DJ

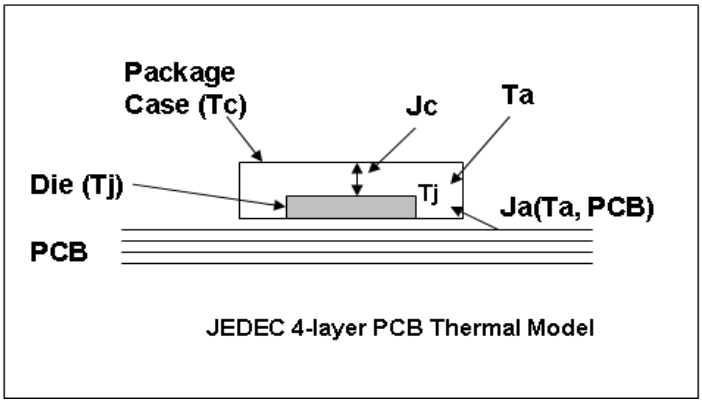
Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter, where is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

Phase Jitter

Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz@10kHz which is phase noise power in 1Hz normalized bandwidth vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter ≤1ps at 12k to 20MHz offset band as SONET standard specification.

Device Thermal Calculation

The JEDEC thermal model in a 4-layer PCB is shown below.



JEDEC IC Thermal Model

Important factors to influence device operating temperature are:

1) The power dissipation from the chip (P_chip) is after subtracting power dissipation from external loads. Generally it can be the no-load device IDD

2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker has better heat dissipation

3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature Tj

The individual device thermal calculation formula:

Tj = Ta + Pchip x Ja

Tc = Tj - Pchip x Jc

Ja ___ Package thermal resistance from die to the ambient air in °C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce Ja (still air) by 20~30%

Jc ___ Package thermal resistance from die to the package case in °C/W unit

Tj ___ Die junction temperature in °C (industry limit <125°C max.)

Ta ___ Ambient air temperature in °C

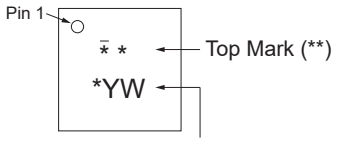
Tc ___ Package case temperature in °C

Pchip___ IC actually consumes power through Iee/GND current

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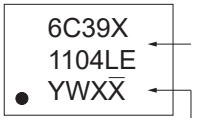
Part Marking

8-X1DFN (XEC)



*: Die Rev (For Fab part ID #: BF23-BA
Y: Date Code (Year)
W: Date Code (Workweek)
Note: Date Code per MA-1251

8-TSSOP (L)

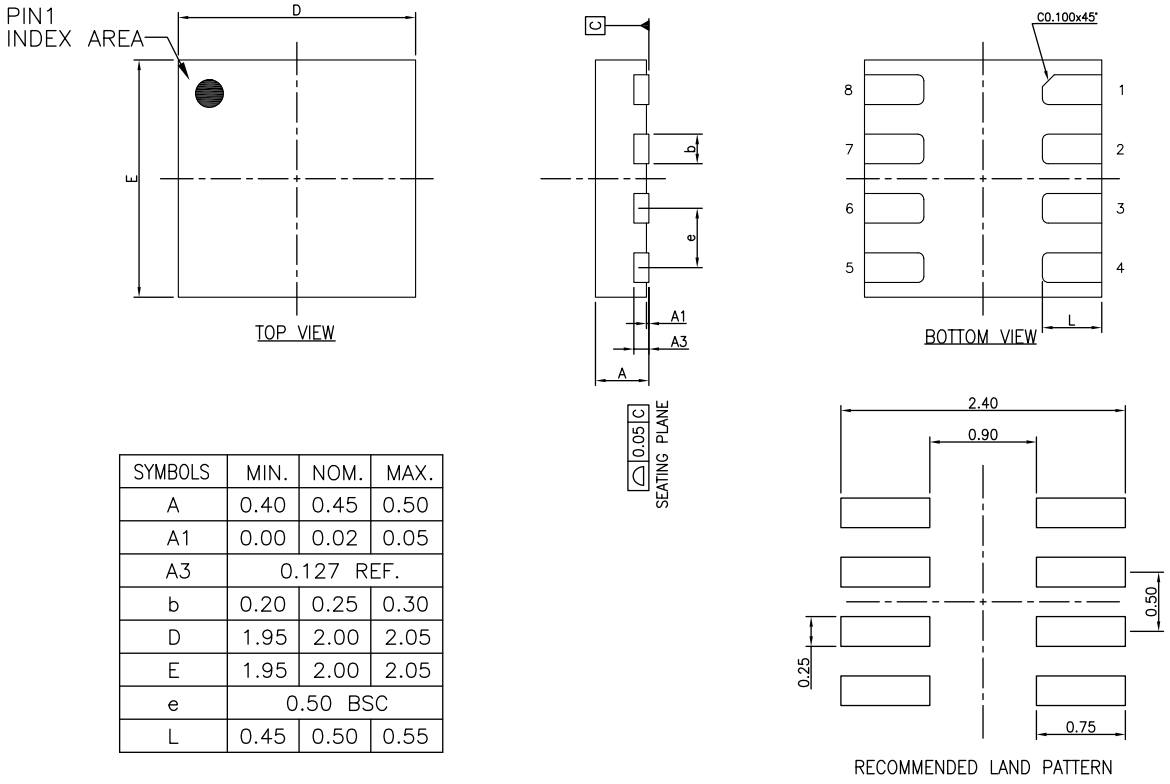


Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Note: Date Code per MA-1251

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Packaging Mechanical

8-X1DFN (XEC)



SYMBOLS	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3		0.127 REF.	
b	0.20	0.25	0.30
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e		0.50 BSC	
L	0.45	0.50	0.55

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. Ref JEDEC MO-287
3. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

DIODES INCORPORATED | PERICOM A PRODUCT LINE OF DIODES INCORPORATED — ENABLING SERIAL CONNECTIVITY

DATE: 09/10/19

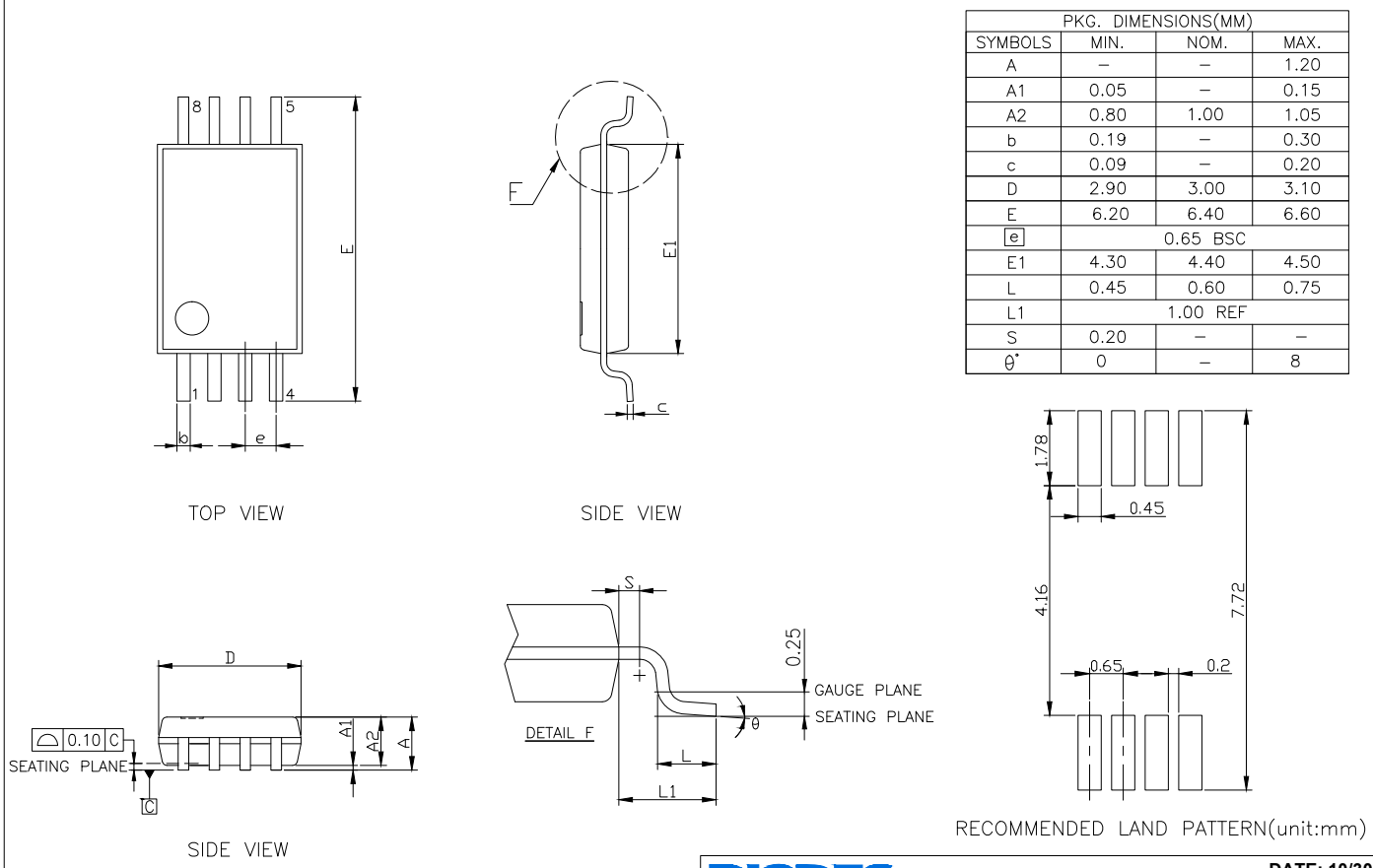
DESCRIPTION: 8-Contact, Extra Thin Dual Flat No-Lead (X1DFN)

PACKAGE CODE: XEC (XEC8)

DOCUMENT CONTROL #: PD-2242 **REVISION: –**

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8-TSSOP (L)



PKG. DIMENSIONS(MM)			
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	2.90	3.00	3.10
E	6.20	6.40	6.60
e	0.65 BSC		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	–	–
θ°	0	–	8

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGRESS.
2. JEDEC MO-153F/AA
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. RECOMMENDED LAND PATTERN REFERENCE DIODES TSSOP8.

DATE: 10/30/25

DESCRIPTION: 8-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L8)

DOCUMENT CONTROL#: PD-1308 REVISION: I

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Mechanical Data

8-X1DFN (XEC)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.0055 grams (Approximate)

8-TSSOP (L)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Sn Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.035 grams (Approximate)

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Ordering Information

Orderable Part Number	Package Code	Package Description
PI6C39X1104XECEX	XEC	8-contact, Extra Thin Dual Flat No-Lead (X1DFN)
PI6C39X1104LEX	L	8-pin, 173mil Wide (TSSOP)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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