A New Direction in Mixed-Signal

XR81112

Universal Clock - High Frequency LVCMOS/LVDS/LVPECL Clock Synthesizer

General Description

The XR81112 is a family of Universal Clock synthesizer devices in a compact QFN-12 package. The devices generate ANY frequency in the range of 10 MHz to 1.5GHz by utilizing a highly flexible delta sigma modulator and a wide ranging VCO. The outputs are configurable for single ended LVCMOS or differential LVDS or LVPECL. The clock outputs have very low phase noise jitter of sub 0.6ps while consuming extremely low power. These devices can be used with standard crystals or an external system clock and can be configured to select from four different frequency multiplier settings to support a wide variety of applications. This family of products have an extremely low power PLL block with core power consumption less than 40% of equivalent devices in the market.

The XR81112 is a clock synthesizer with Integer/fractional divider, LVCMOS/LVDS/LVPECL driver, 3.3V/2.5V supply, taking a Xtal input and providing one of four selectable output frequencies. The device is optimized for use with a fundamental mode 10MHz to 60MHz crystal (or system clock) and generates a selection of output frequencies from 10MHz to 1.5GHz in either integer or fractional mode. In fractional mode, frequency resolution of less than 1Hz steps can be achieved.

The application diagram below shows a typical synthesizer configuration with any standard crystal oscillating in fundamental mode. Internal load capacitors are optionally available to minimize/eliminate external crystal loads. A system clock can also be used to overdrive the oscillator for a synchronous timing system.

The typical phase noise plot below shows the jitter integrated over the 12KHz to 20MHz range that is widely used in WAN systems. The typical noise for the integration range of 1.875MHz to 20MHz is sub 200fs which is important for LAN applications. These clock devices show a very good high frequency noise floor below -150dB.

FEATURES

- Small footprint 3mm x 3mm QFN package
- Configurable - As one differential LVPECL/LVDS output pair or as a single ended LVCMOS output
- Crystal oscillator interface which can also be overdriven using a single-ended reference clock
- Output frequency range: 10MHz - 1500MHz
- Crystal/input frequency: 10MHz to 60MHz, parallel resonant crystal
- VCO range: 2GHz - 3GHz
- RMS phase jitter @ 156.25MHz, 12KHz - 20MHz: <0.60ps
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) package

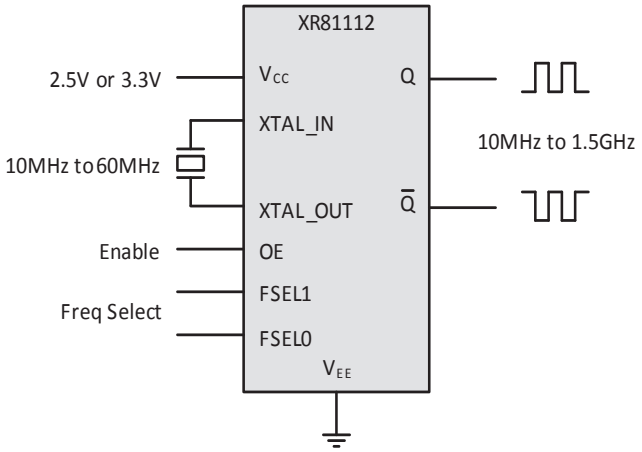
APPLICATIONS

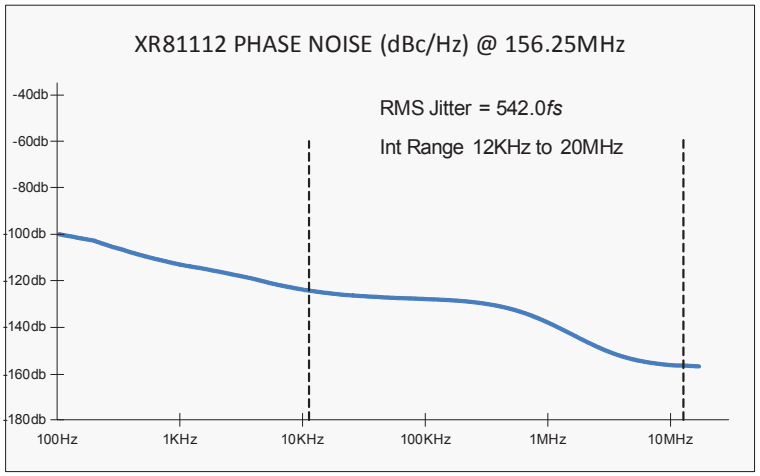
- 10GE, GE LAN/WAN
- 2.5G/10G SONET/SDH/OTN
- xDSL, PCIe
- Low-jitter Clock Generation
- Synchronized clock systems

Ordering Information – back page

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Typical Application





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Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Maximum Rating condition for extended periods may affect device reliability and lifetime.

Power Supply Voltage (VCC).....+4.2V

Input Voltage.....-0.5V to VCC + 0.5V

Output Voltage.....-0.5V to VCC + 0.5V

Reference Frequency/Input Crystal.....10MHz to 60MHz

Storage Temperature.....-55°C to +125°C

Lead Temperature (Soldering, 10 sec).....300°C

ESD Rating (HBM - Human Body Model).....2.0kV

Operating Conditions

Operating Temperature Range.....-40°C to +85°C

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Electrical Characteristics

Unless otherwise noted: T_A = -40°C to +85°C, V_{CC} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V

Symbol	Parameter	Conditions	*	Min	Typ	Max	Units
3.3V Power Supply DC Characteristics							
V_{CC}	Power Supply Voltage		•	3.135	3.3	3.465	V
I_{EE}	Power Supply Current PECL LVDS CMOS	Includes output loading Measured at 1500MHz Measured at 1500MHz Measured at 200MHz	 • • •		 86 34 48	 120 50 65	 mA mA mA
2.5V Power Supply DC Characteristics							
V_{CC}	Power Supply Voltage		•	2.375	2.5	2.625	V
I_{EE}	Power Supply Current PECL LVDS CMOS	Includes output loading Measured at 1500MHz Measured at 1500MHz Measured at 200MHz	 • • •		 69 25 37	 95 35 50	 mA mA mA
LVCMOS/LVTTL DC Input Characteristics							
V_{IH}	Input High Voltage (OE, FSEL[1:0])	V_{CC} = 3.465V	•	2.42		V_{CC} + 0.3	V
		V_{CC} = 2.625V	•	1.83		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage(OE, FSEL[1:0])	V_{CC} = 3.465V	•	-0.3		1.03	V
		V_{CC} = 2.625V	•	-0.3		0.785	V
I_{IH}	Input High Current (OE, FSEL[1:0])	V_{IN} = V_{CC} = 3.465V or 2.625V	•			15	µA
I_{IL}	Input Low Current (OE, FSEL[1:0])	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	•	-10			µA
LVCMOS DC Output Characteristics (Vcc = 3.3 +/- 5% or Vcc = 2.5 +/- 5%)							
V_{OH}	Output High Voltage	Output Unloaded	•	0.8 * V_{CC}			V
V_{OL}	Output Low Voltage	Output Unloaded	•			0.1 * V_{CC}	V
LVPECL DC Output Characteristics (Vcc = 3.3 +/- 5% or Vcc = 2.5 +/- 5%)							
V_{OH}	Output High Voltage		•	V_{CC} - 1.3		V_{CC} - 0.4	V
V_{OL}	Output Low Voltage		•	V_{CC} - 2.0		V_{CC} - 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		•	0.6		1.2	V
LVDS DC Output Characteristics (Vcc = 3.3 +/- 5% or Vcc =2.5 +/- 5%)							
V_{OD}	Differential Output Voltage	Output < 1GHz	•	200		550	mV
V_{OC}	Common Mode Voltage		•		1.25		V

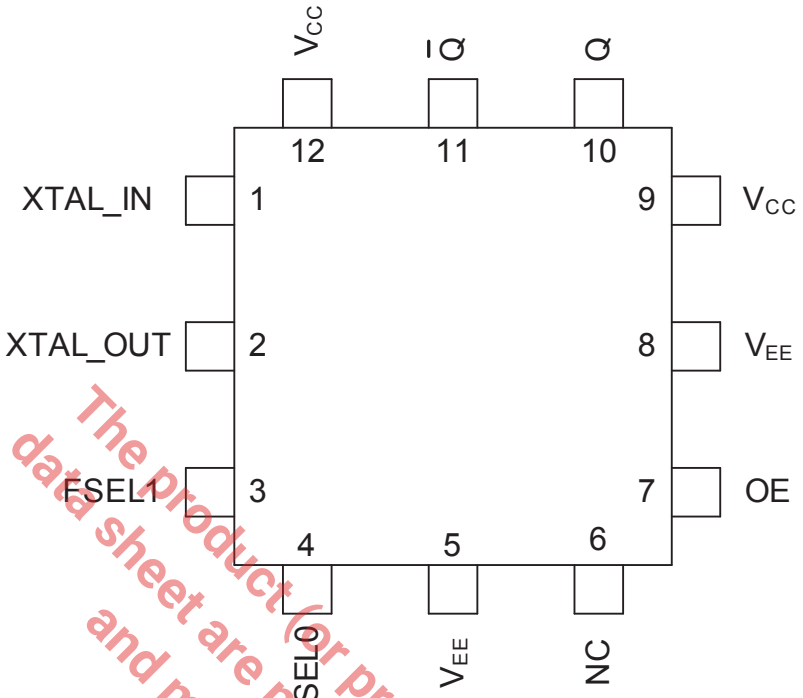
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Symbol	Parameter	Conditions	*	Min	Typ	Max	Units
Crystal Characteristics							
X_{Mode}	Mode of Oscillations			Fundamental			
X_f	Frequency			10		60	MHz
ESR	Equivalent Series Resistance					50	Ω
C_S	Shunt Capacitance					7	pF
AC Characteristics							
f_{OUT}	Output Frequency			10		1500	MHz
$t_{jit}(\phi)$	RMS Phase Jitter	156.25MHz (w/25MHz ref) Integration Range 12kHz-20MHz			0.6		pS
		150MHz (w/25MHz ref) Integration Range 12kHz-20MHz			0.6		pS
		125MHz (w/25MHz ref) Integration Range 12kHz-20MHz			0.6		pS
		100MHz (w/25MHz ref) Integration Range 12kHz-20MHz			0.6		pS
$t_{jit}(\phi)$I	Integer RMS Phase Jitter		•			1.0	pS
$t_{jit}(\phi)$F	Fractional RMS Phase Jitter	with Ref input >25MHz	•			1.5	pS
t_R/t_F	Output Rise/Fall Time	20% to 80%, see Figure 10	•	100		500	pS
Odc	Output Duty Cycle	see Figure 11	•	45		55	%

* Limits applying over the full operating temperature range are denoted by a "•".

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Pin Configuration



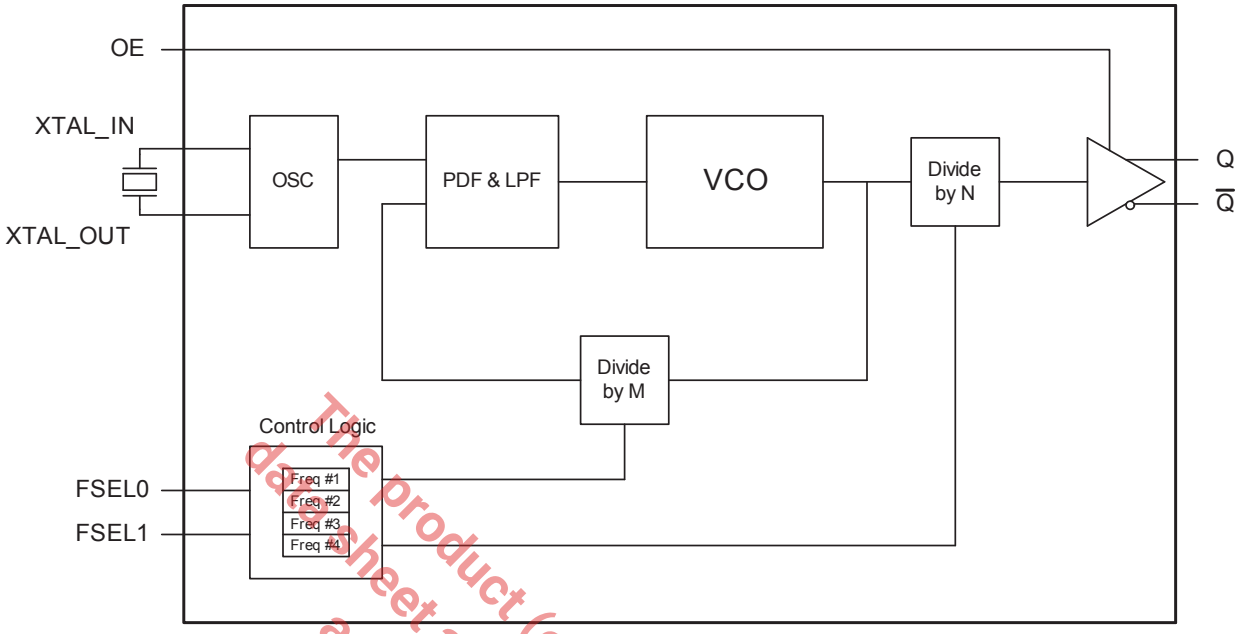
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Pin Assignments

Pin No.	Pin Name	Type	Description
1	XTAL_IN	Input	Crystal oscillator input.
2	XTAL_OUT	Output	Crystal oscillator output.
3	FSEL1	Input (900KΩ pull-dwn)	Output frequency select pin, MSB (LVCMOS/LVTTL input).
4	FSEL0	Input (900KΩ pull-dwn)	Output frequency select pin, LSB (LVCMOS/LVTTL input).
5	V_{EE}	Supply	Negative supply pin.
6	NC	No Connect	Unused, do not connect.
7	OE	Input (900KΩ pull-up)	Output enable pin - LVCMOS/LVTTL active high input. Outputs are enabled when OE = high. Outputs are disabled when OE = low.
8	V_{EE}	Supply	Negative supply pin.
9	V_{CC}	Supply	Power supply pin.
10	Q	Output	Positive output.
11	$\overline{Q}$	Output	Inverted output.
12	V_{CC}	Supply	Power supply pin.

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Functional Block Diagram



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Typical Performance Characteristics

Figures 1, 2, 3 and 4 show typical phase noise performance plots for 156.25 MHz, 150MHz, 125M, and 100MHz clock outputs respectively. The data was taken using the industry standard Agilent E5052B instrument. The integration range is the widely referenced 12KHz to 20MHz range most often used in WAN applications.

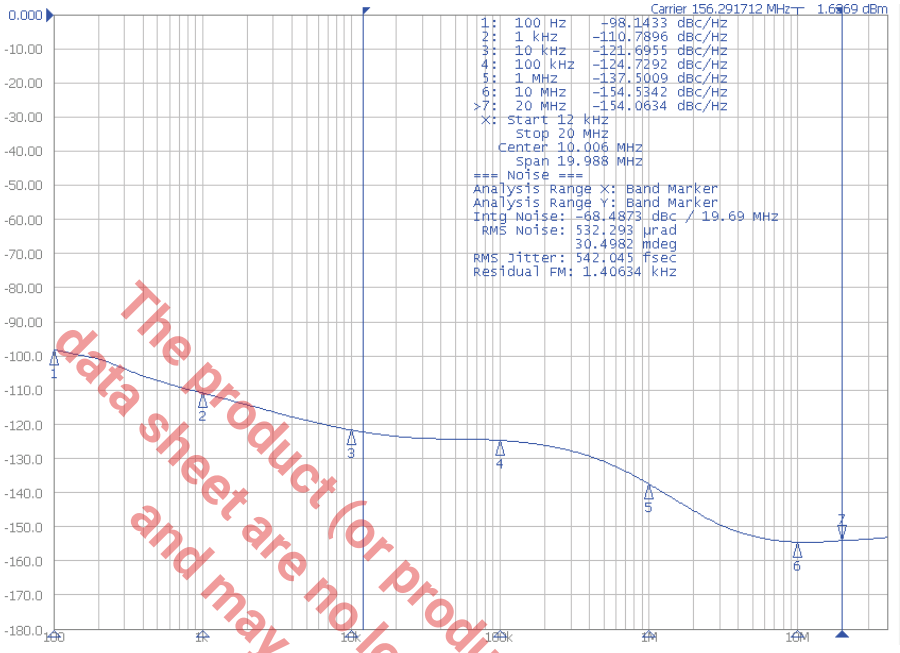


Figure 1: 156.25MHz Operation, Phase Noise at 3.3V

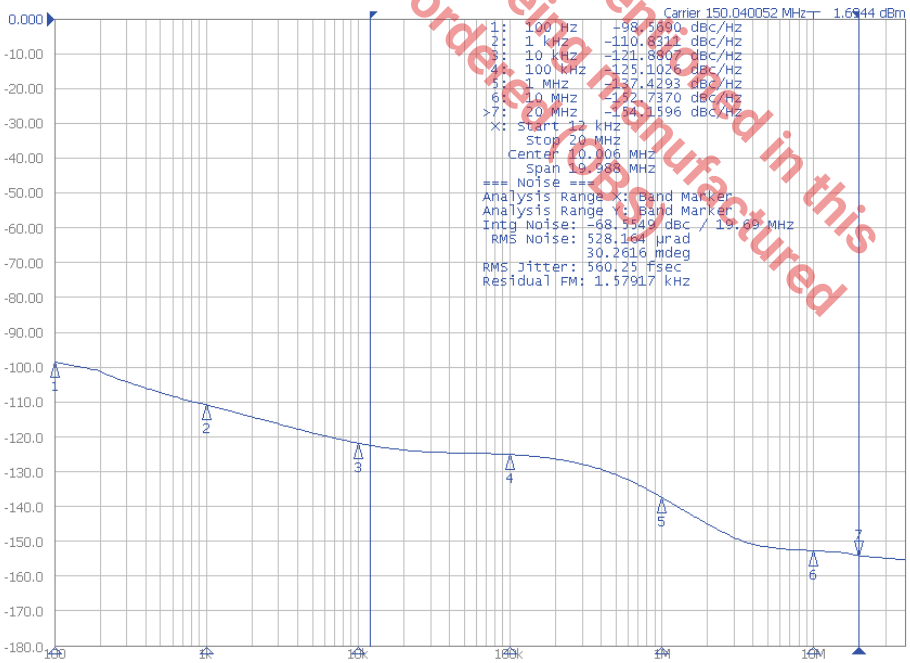


Figure 2: 150MHz Operation, Phase Noise at 3.3V)

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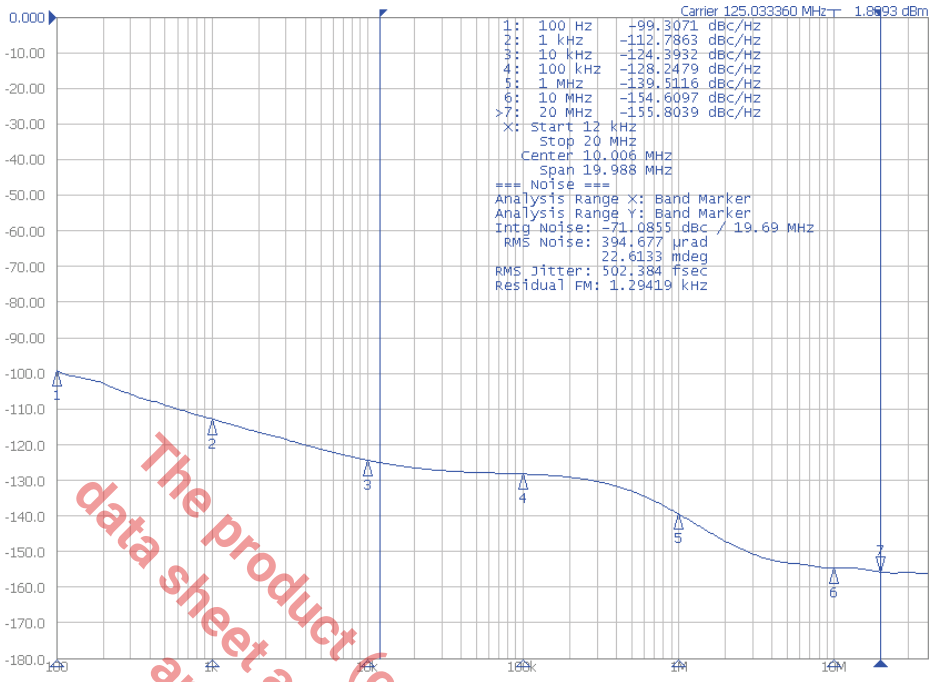


Figure 3: 125MHz Operation, Phase Noise at 3.3V

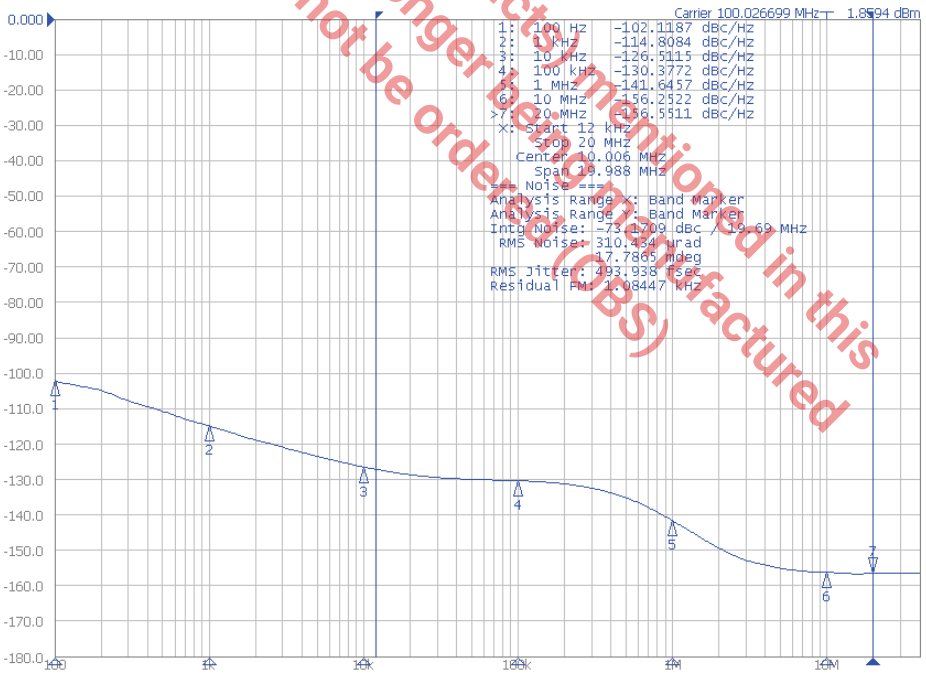


Figure 4: 100MHz Operation, Phase Noise at 3.3V

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Application Information

Functional Truth Table

The XR81112 Universal Clock can support up to 4 individual output frequency configurations. Once configured, the two frequency select pins, FSLEL[1:0], will determine the output frequency from the device. This allows the XR81112 to support a variety of applications. If the FSEL pins are left floating, the XR81112 will default (with internal pull-down resistors on the FSEL inputs) to the Frequency #1 output.

Table 1: Output Frequency Selection

FSEL[1:0]	Output Frequency (MHz)
00	Frequency #1
01	Frequency #2
10	Frequency #3
11	Frequency #4

Termination for LVPECL Outputs

The termination schemes shown in Figure 5 and Figure 6 are typical for LVPECL outputs. Matched impedance layout techniques should be used for the LVPECL output pairs to minimize any distortion that could impact your maximum operating frequency. Figure 7 is an alternate termination scheme that uses a Y-termination approach.

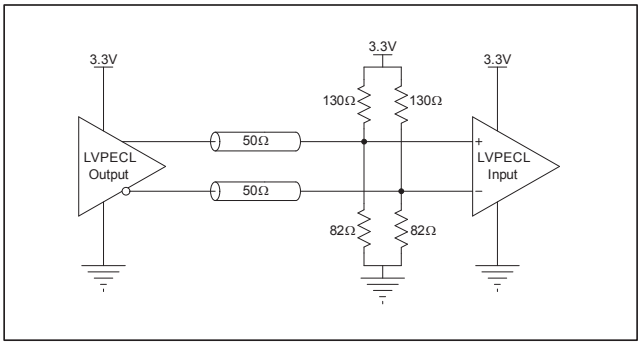


Figure 5: XR81112 3.3V LVPECL Output Termination

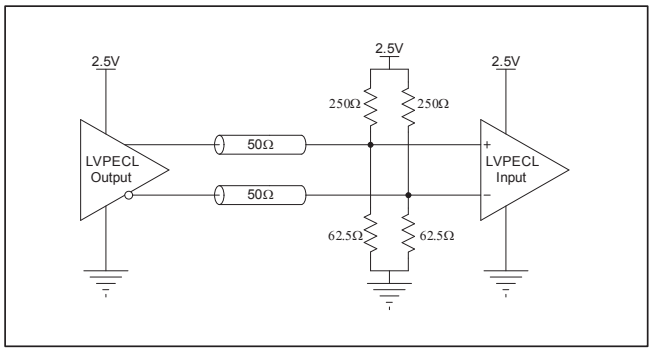


Figure 6: XR81112 2.5V LVPECL Output Termination

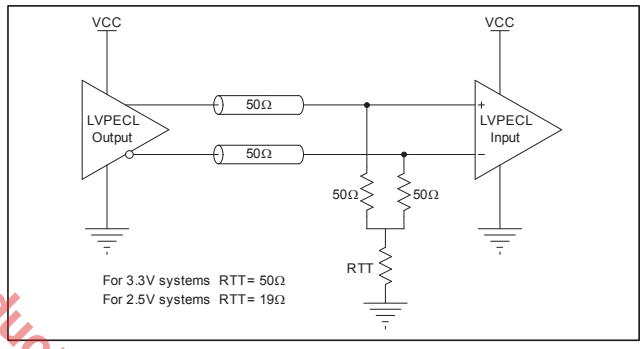


Figure 7: XR81112 Alternate LVPECL Output Termination Using Y-termination

Termination for LVDS Outputs

The termination schemes shown in Figure 8 and Figure 9 are typical for LVDS outputs. LVDS swing is a small , typically 350mV, on 1.2V of common mode. The LVDS output pair needs a 100Ω resistor across the differential pair as close to the destination as possible.

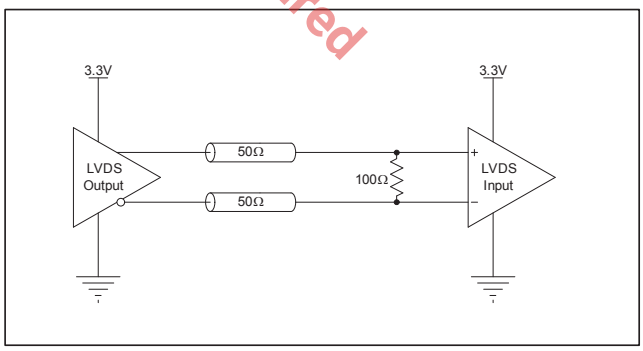


Figure 8: XR81112 3.3V LVDS Output Termination

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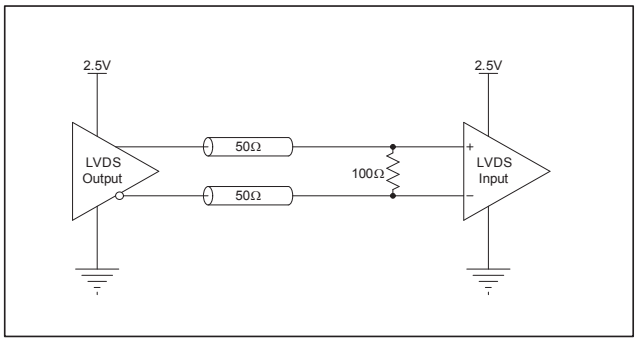


Figure 9: XR81112 2.5V LVDS Output Termination

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Output Signal Timing Definitions

The following diagrams clarify the common definitions of the AC timing measurements.

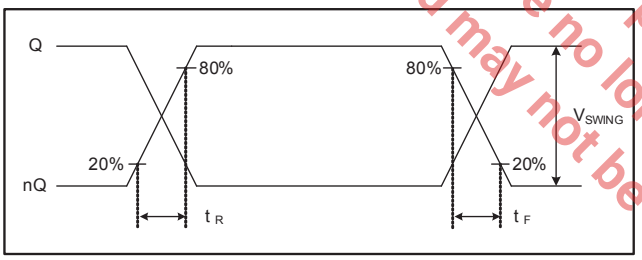


Figure 10: Output Rise/Fall Time and Swing

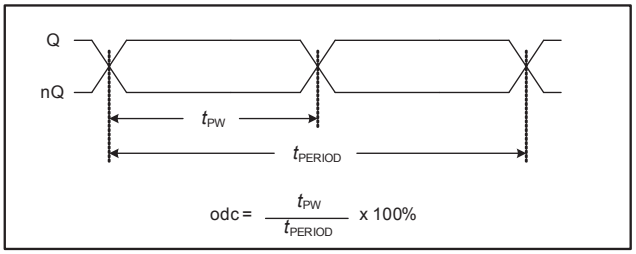
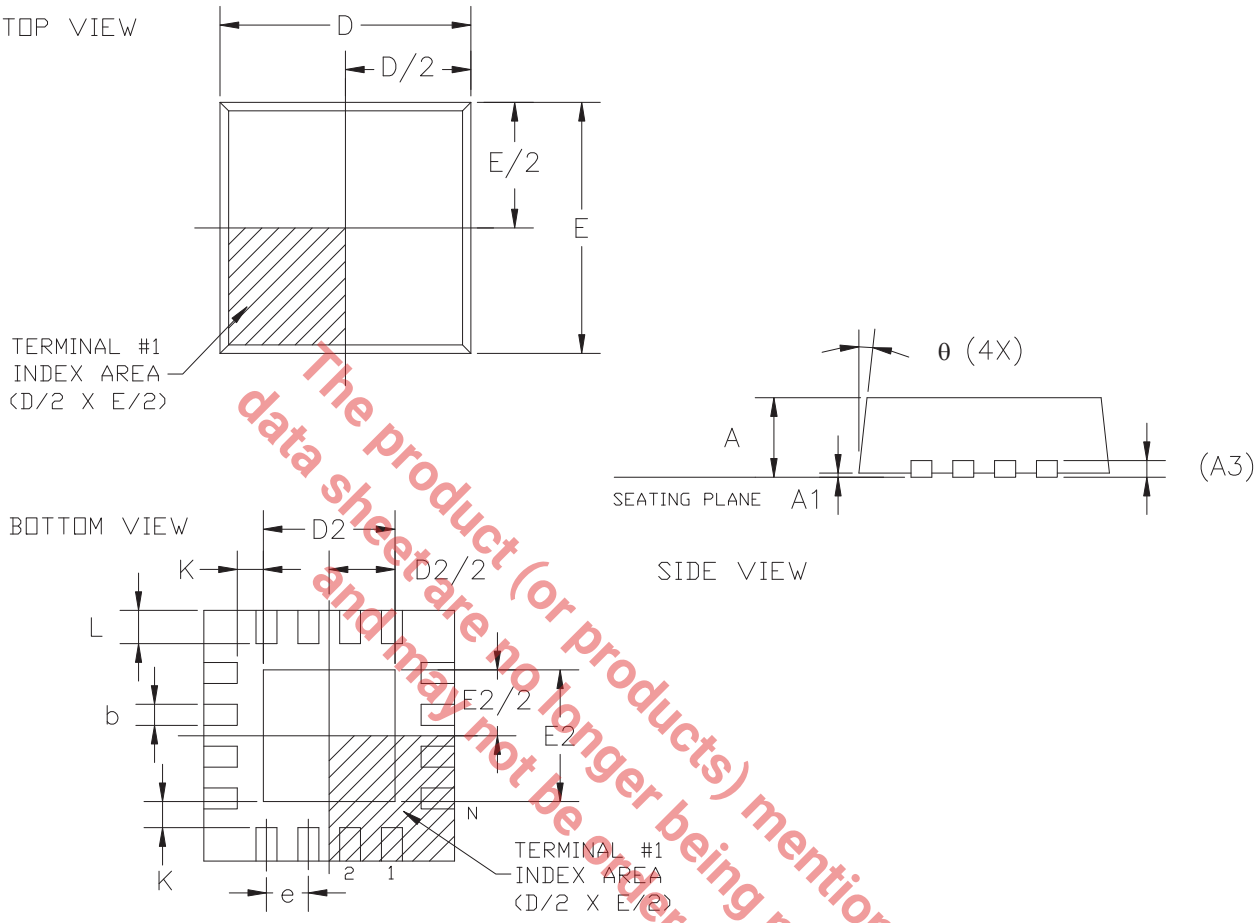


Figure 11: Output Period and Duty Cycle

Mechanical Dimensions

12-Pin QFN



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12LD 3x3 QFN JEDEC MO-220 Variation VEED-5.1						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	3.00 BSC			0.118 BSC		
D2	1.30	1.45	1.55	0.051	0.057	0.061
E	3.00 BSC			0.118 BSC		
E2	1.30	1.45	1.55	0.051	0.057	0.061
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	—	—	0.008	—	—
θ	0°	—	14°	0°	—	14°
N	12			12		
ND	3			3		
NE	3			3		

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Ordering Information

Part Number	Package	Green	Operating Temperature Range	Shipping Packaging	Marking
XR81112-F	12-pin QFN	Yes	-40°C to +85°C	Tube/Tray	T112
XR81112EVB	Eval Board	N/A	N/A	N/A	N/A

Revision History

Revision	Date	Description
1A	June 2014	Initial release. [ECN1426-29_6/28/2014]

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