Preliminary

# XRD64L43

## Dual 10-Bit 40MSPS CMOS ADC

July 2003

### FEATURES

- 10-Bit Resolution
- Two Monolithic Complete 10-Bit ADCs
- 40 MSPS Conversion Rate
- On-Chip Track-and-Hold
- On-Chip Voltage Reference
- Low 5 pF Input Capacitance
- TTL/CMOS Outputs
- Tri-State Output Buffers
- Single +3.0V Power Supply Operation
- Low Power Dissipation: 200mW-typ @ 2.7V
- Power Down Mode Less Than 5mW
- 75dB Crosstalk (fin=1.0MHz)
- -40°C to +85°C Operation Temperature Range

### APPLICATIONS

- Medical Imaging
- Instrumentation
- Data Aquisition Systems
- Digital Comunications

### BENEFITS

- Reduction of Components
- Reduction of System Cost
- High Performance @ Low Power Dissipation
- Long Term Time and Temperature Stability

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### GENERAL DESCRIPTION

The XRD64L43 is two 10-bit, monolithic, 40 MSPS ADCs. Manufactured using a standard CMOS process, the XRD64L43 offers low power, low cost and excellent performance. The on-chip track-and-hold amplifier(T/H) and voltage reference (VREF) eliminate the need for external active components, requiring only an external ADC conversion clock for the application. The XRD64L43 analog input can be driven with ease due to the high input impedance.

The design architecture uses 17 time- interleaved 10-bit SAR ADCs in each converter to achieve high conversion rate of 40 MSPS minimum. In order to insure and maintain accurate 10-bit operation with respect to time and temperature, XRD64L43 incorporates an auto-calibration circuit which continuously adjusts and matches the offset and linearity of each ADC. This auto-calibration circuit is transparent to the user after the initial 4.2ms calibration (168,000 initial clock cycles).

The power dissipation is only 200mW at 40 MSPS with +2.7V power supply.

The digital output data is straight binary format, and the tri-state disable function is provided for common bus interface.

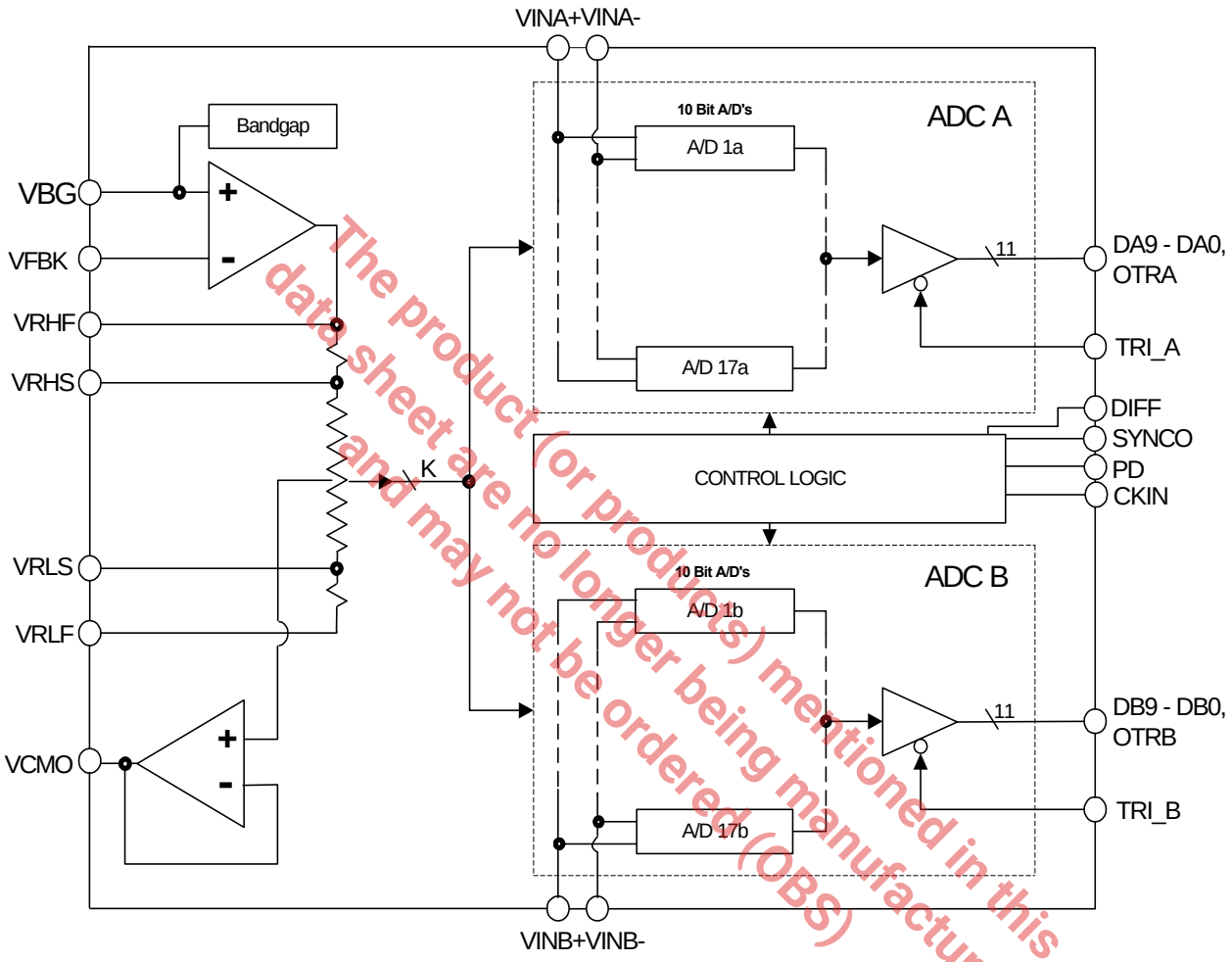
The XRD64L43 internal reference provides cost savings and simplifies the design/development. The output voltage of the internal reference is set by two external resistors. The internal reference can be disabled if an external reference is used for a power savings of 50mW.

### ORDERING INFORMATION

| Part Number | Package Type | Temperature Range |
|---|---|---|
| XRD64L43AIV | 64-Lead LQFP | -40°C to +85°C |

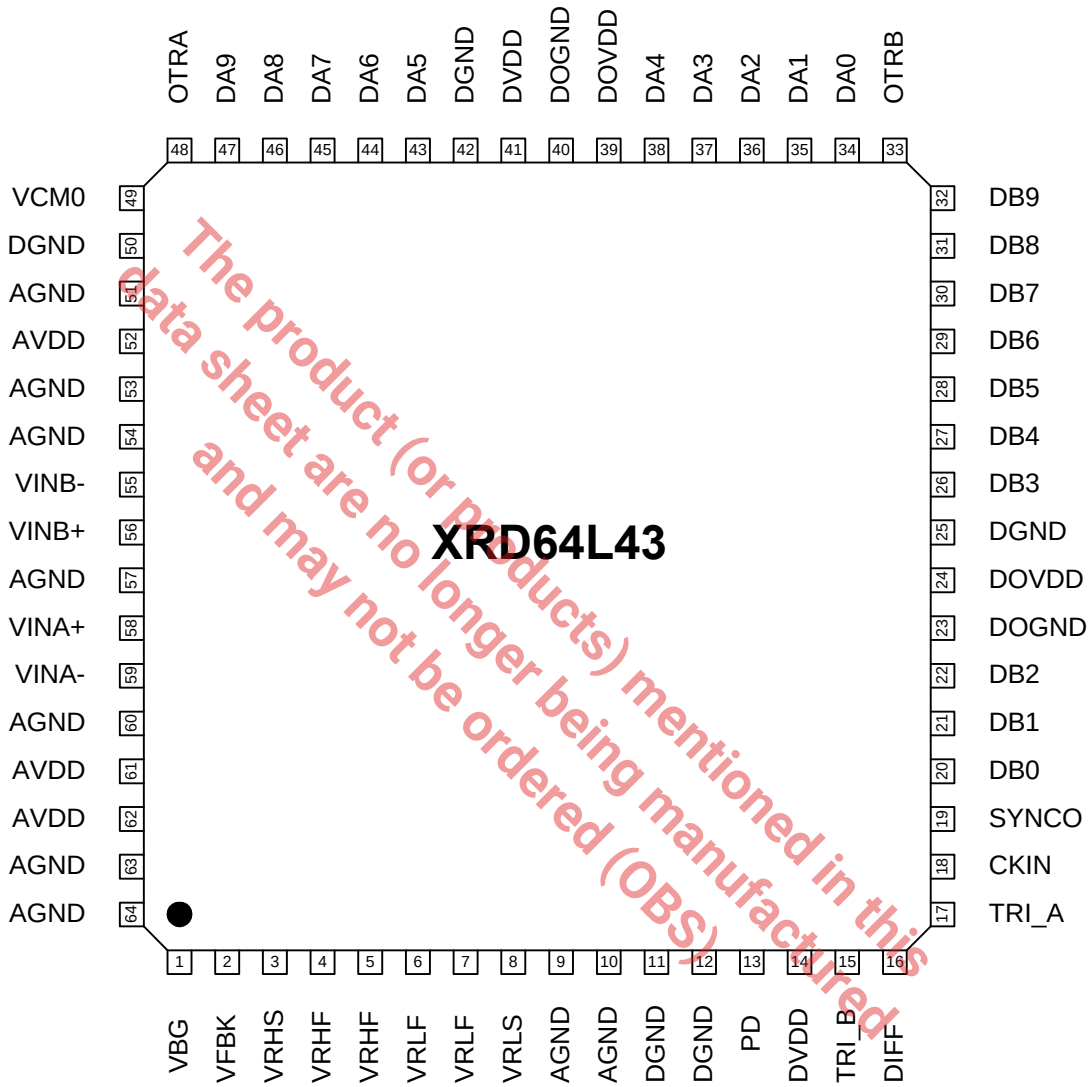


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**Figure 1. XRD64L43 Simplified Block Diagram**




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## PIN DESCRIPTION

| Pin # | Symbol | Description |
|---|---|---|
| 1 | VBG | Bandgap Voltage Output |
| 2 | VFBK | Analog Reference Feedback |
| 3 | VRHS | Top Voltage Reference Sense |
| 4 | VRHF | Top Voltage Reference Force |
| 5 | VRHF | Top Voltage Reference Force |
| 6 | VRLF | Bottom Voltage Reference Force |
| 7 | VRLF | Bottom Voltage Reference Force |
| 8 | VRLS | Bottom Voltage Reference Sense |
| 9 | AGND | Analog Ground |
| 10 | AGND | Analog Ground |
| 11 | DGND | Digital Ground |
| 12 | DGND | Digital Ground |
| 13 | PD | Power Down, Active High |
| 14 | DVDD | Digital Supply Voltage |
| 15 | TRI_B | Tri-state for the B Channel Outputs, Active High |
| 16 | DIFF | Hi=Differential Mode, Lo=Single-Ended Mode |
| 17 | TRI_A | Tri-state for the A Channel Outputs, Active High |
| 18 | CKIN | Clock Input |
| 19 | SYNCO | Data Valid Output (Rising Edge) |
| 20 | DB0 | Digital Output Bit 0 (LSB) ADC B |
| 21 | DB1 | Digital Output Bit 1 ADC B |
| 22 | DB2 | Digital Output Bit 2 ADC B |
| 23 | DOGND | Digital Output Ground |
| 24 | DOVDD | Digital Output Supply Voltage |
| 25 | DGND | Digital Ground |
| 26 | DB3 | Digital Output Bit 3 ADC B |
| 27 | DB4 | Digital Output Bit 4 ADC B |
| 28 | DB5 | Digital Output Bit 5 ADC B |
| 29 | DB6 | Digital Output Bit 6 ADC B |
| 30 | DB7 | Digital Output Bit 7 ADC B |
| 31 | DB8 | Digital Output Bit 8 ADC B |
| 32 | DB9 | Digital Output Bit 9 (MSB) ADC B |
| 33 | OTRB | Over Range Digital Output Bit ADC B |
| 34 | DA0 | Digital Output Bit 0 (LSB) ADC A |
| 35 | DA1 | Digital Output Bit 1 ADC A |
| 36 | DA2 | Digital Output Bit 2 ADC A |
| 37 | DA3 | Digital Output Bit 3 ADC A |
| 38 | DA4 | Digital Output Bit 4 ADC A |
| 39 | DOVDD | Digital Output Supply Voltage |
| 40 | DOGND | Digital Output Ground |
| 41 | DVDD | Digital Supply Voltage |

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**PIN DESCRIPTION (CONT'D)**

| Pin # | Symbol | Description |
|---|---|---|
| 42 | DGND | Digital Ground |
| 43 | DA5 | Digital Output Bit 5 ADC A |
| 44 | DA6 | Digital Output Bit 6 ADC A |
| 45 | DA7 | Digital Output Bit 7 ADC A |
| 46 | DA8 | Digital Output Bit 8 ADC A |
| 47 | DA9 | Digital Output Bit 9 ADC A |
| 48 | OTRA | Over Range Digital Output Bit ADC A |
| 49 | VCMO | Differential Common Mode Voltage Output |
| 50 | DGND | Digital Ground |
| 51 | AGND | Analog Ground |
| 52 | AVDD | Analog Supply Voltage |
| 53 | AGND | Analog Ground |
| 54 | AGND | Analog Ground |
| 55 | VINB- | Analog Input B(-) |
| 56 | VINB+ | Analog Input B(+) |
| 57 | AGND | Analog Ground |
| 58 | VINA+ | Analog Input A(+) |
| 59 | VINA- | Analog Input A(-) |
| 60 | AGND | Analog Ground |
| 61 | AVDD | Analog Supply Voltage |
| 62 | AVDD | Analog Supply Voltage |
| 63 | AGND | Analog Ground |
| 64 | AGND | Analog Ground |

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**ELECTRICAL CHARACTERISTICS TABLE (CONT'D)**

**Test Conditions (Unless Otherwise Specified)**

**$T_A$ = 25°C $AV_{DD}$ = $DV_{DD}$ = +3.0V, VIN = GND to +2.5V, $V_{RLF}$ = GND, $V_{RHF}$ = +2.5V and Fs = 40 MSPS, 50% Duty Cycle, Differential Input Mode**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **DC ACCURACY** | | | | | | |
| DNL | Differential Non-Linearity | -0.75 | +/-0.25 | 0.75 | LSB | |
| INL | Integral Non-Linearity | | +/-0.5 | | LSB | |
| MON | Monotonicity | No Missing Codes | | | | Guaranteed by Test |
| FSE | Full Scale Error | | ±10 | | mV | Note 1 |
| ZSE | Zero Scale Error | | 5 | | mV | Single Ended Mode |
| **ANALOG INPUT** | | | | | | |
| INVR | Input Voltage Range | 1 | | VRHS - VRLS | V | VRLF Grounded |
| INRES | Input Resistance | | 20 | | KOhms | |
| INCAP | Input Capacitance | | 5 | | pF | |
| INBW | Input Bandwidth | | 400 | | MHz | -1dB Small Signal |
| **REFERENCE INPUT, INTERNAL BANDGAP REFERENCE AND REFERENCE BUFFER** | | | | | | |
| $R_{LADDER}$ | Ladder Resistance | 100 | 125 | 150 | Ohms | Note 1 |
| $R_{SENSE}$ | Sense Resistance | | 2 | | Ohms | |
| RLADTCO | Ladder Resistance Tempco | | +0.8 | | Ohms/°C | |
| VBG | Bandgap Output Voltage Range | 1.15 | 1.25 | 1.35 | V | |
| VBGTC | Bandgap Reference Tempco | | 30 | | ppm/°C | |
| VRLF | | 0.0 | 0.0 | 2.0 | V | |
| VRHF | | VRLF+ 1.0 | | AVdd-0.3 | V | Internal Reference Buffer |
| VRHF | External Reference | VRLF+ 1.0 | 2.5 | AVdd | V | External |
| VRHF PSRR | Internal Reference Buffer | | 6 | | mV/V | |
| **VCMO, Common Mode Voltage** | | | | | | |
| VCMO | Common Mode Voltage | 1.15 | 1.25 | 1.35 | V | |
| Isource | Current Source | 200 | 500 | | uA | |

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***Notes:***

1 *Full Scale ADC reference is VRHS - VRLS.*

**ELECTRICAL CHARACTERISTICS TABLE (CONT'D)**

**Test Conditions (Unless Otherwise Specified)**

**$T_A$ = 25°C $AV_{DD}$ = $DV_{DD}$ = +3.0V, VIN = GND to +2.5V, $V_{RLF}$ = GND, $V_{RHF}$ = +2.5V and Fs = 40MSPS, 50% Duty Cycle, Differential Input Mode**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE Fs = 40MHz** | | | | | | |
| SNR | Signal-to-Noise Ratio | | | | | Not Including Harmonics |
| | fin = 1.0 MHz | 58 | 60 | | dB | |
| | fin = 4.0 MHz | 57 | 60 | | dB | |
| | fin = 10.0 MHz | 57 | 59 | | dB | |
| SINAD | Signal-to Noise and Distortion | | | | | Including Harmonics |
| | fin = 1.0 MHz | 58 | 60 | | dB | |
| | fin = 4.0 MHz | 57 | 59 | | dB | |
| | fin = 10 MHz | 56 | 58 | | dB | |
| **ENOB EFFECTIVE NUMBER OF BITS** | | | | | | |
| | fin = 1.0 MHz | 9.3 | 9.7 | | Bit | |
| | fin = 4.0 MHz | 9.2 | 9.5 | | Bit | |
| | fin = 10 MHz | 9.0 | 9.2 | | Bit | |
| **SFDR SPURIOUS FREE DYNAMIC RANGE** | | | | | | |
| SFDR | fin = 1.0 MHz | | 70 | | dB | |
| Crosstalk | fin = 1.0 MHz | | 75 | | dB | |
| IMD | $fin_1$ = 2.5 MHz<br>$fin_2$ = 3.5 MHz | | 70 | | dB | Intermodulation Distortion |
| **CONVERSION AND TIMING CHARACTERISTICS ($C_L$ = 10pF)** | | | | | | |
| MAXCON | Maximum Conversion | 40 | 50 | | MSPS | |
| MINCON | Minimum Conversion | | 100 | | KSPS | |
| Lat | Latency | | 17 | | cycles | Guaranteed by Design |
| APJT | Aperture Jitter Time | | 12 | | ps | Peak-to Peak |
| $t_r$ | Digital Output Rise Time | | 3 | | ns | |
| $t_f$ | Digital Output Fall Time | | 3 | | ns | |
| $t_{pd}$ | Output Data Propagation Delay | | 6 | 25 | ns | |
| $t_{den}$ | Output Data Enable Delay | | 6 | 20 | ns | Guaranteed by Design |
| $t_{dis}$ | Output Data Disable Delay | | 5 | 20 | ns | Guaranteed by Design |
| CLKDC | Clock Duty Cycle | 40 | 50 | 60 | % | Guaranteed by Design |

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**ELECTRICAL CHARACTERISTICS TABLE (CONT'D)**

**Test Conditions (Unless Otherwise Specified)**

**$T_A$ = 25°C $AV_{DD}$ = $DV_{DD}$ = +3.0V, VIN = GND to +2.5V, $V_{RLF}$ = GND, $V_{RHF}$ = +2.5V and Fs = 40 MSPS, 50% Duty Cycle, Differential Input Mode**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | | |
| DVINH | Digital Input High Voltage | 2.5 | | | V | |
| DVINL | Digital Input Low Voltage | | | 0.5 | V | |
| **DIINH** | **Digital Input High Leakage** | | | | | |
| CKIN | Clock Input | -1.0 | 0.05 | 1.0 | µA | |
| DIFF | Differential/Single-Ended Input | -1.0 | -0.25 | 1.0 | uA | Internal pull-up resistor |
| TRI_A/TRI_B | A/B Channel Tri-State | -125.0 | -90.0 | -50.0 | uA | Internal pull-down resistor |
| PD | Power Down | -125.0 | -90.0 | -50.0 | uA | Internal pull-down resistor |
| **DIINL** | **Digital Input Low Leakage** | | | | | |
| CKIN | Clock Input | -5.0 | 0.05 | 5.0 | nA | |
| DIFF | Differential/Single-Ended Input | 50.0 | 90.0 | 125.0 | uA | Internal pull-up resistor |
| TRI_A/TRI_B | A/B Channel Tri-State | -1.0 | 0.25 | 1.0 | uA | Internal pull-down resistor |
| PD | Power Down | -1.0 | 0.25 | 1.0 | uA | Internal pull-down resistor |
| DINC | Digital Input capacitance | | 5 | 8 | pF | |
| **DIGITAL OUTPUTS (CL = 10 pF)** | | | | | | |
| DOHV | Digital Output High Voltage | DVdd -0.4V | DVdd-0.3V | | V | IOH = 1.5 mA |
| DOLV | Digital Output Low Voltage | | 0.3 | 0.4 | V | IOL = 1.5 mA |
| IOZ | High-Z Leakage | -100 | 0.2 | 100 | nA | |

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**ELECTRICAL CHARACTERISTICS TABLE (CONT'D)**

**Test Conditions (Unless Otherwise Specified)**

**$T_A$ = 25°C $AV_{DD}$ = $DV_{DD}$ = +3.0V, VIN = GND to +2.5V, $V_{RLF}$ = GND, $V_{RHF}$ = +2.5V and Fs = 40 MSPS, 50% Duty Cycle, Differential Input Mode**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| $AV_{DD}$ | Analog Power Supply Voltage | 2.7 | 3.0 | 3.3 | V | |
| $DV_{DD}$ | Digital Power Supply Range | 2.7 | $AV_{DD}$ | 3.3 | V | $DV_{DD}$ = $AV_{DD}$ |
| **Fs = 40 MHz, $AV_{DD}$ = $DV_{DD}$ = 2.7V, CL = 10pF, Fin = 10MHz (Includes Iref Current)** | | | | | | |
| AIDD | Analog Supply Current | | 55 | | mA | |
| DIDD | Digital Supply Current | | 13 | | mA | |
| DOIDD | Output Driver Current | | 6 | | mA | |
| PDISS | Power Dissipation | | 200 | | mW | |
| **Fs = 40 MHz, $AV_{DD}$ = $DV_{DD}$ = 3.3V, CL = 10pF, Fin = 10MHz (Includes Iref Current)** | | | | | | |
| AIDD | Analog Supply Current | | 37 | 70 | mA | |
| DIDD | Digital Supply Current | | 15 | 20 | mA | |
| DOIDD | Output Driver Current | | 15 | 20 | mA | |
| PDISS | Power Dissipation | | 225 | 365 | mW | |
| **POWER DOWN CURRENT** | | | | | | |
| IPD | Power Down Current | | 100 | 300 | µA | |

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**ABSOLUTE MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted)[1, 2, 3]**

$V_{DD}$ to GND ..... +7.0V

$V_{RT}$ & $V_{RB}$ ..... $V_{DD}$ +0.5 to GND -0.5V

$V_{IN}$ ..... $V_{DD}$ +0.5 to GND -0.5V

All Inputs ..... $V_{DD}$ +0.5 to GND -0.5V

All Outputs ..... $V_{DD}$ +0.5 to GND -0.5V

Storage Temperature ..... -65°C to 150°C

Lead Temperature (Soldering 10 seconds) ..... 300°C

Maximum Junction Temperature ..... 150°C

Package Power Dissipation Ratings ($T_A$ = +70°C)

TQFP ..... $\theta_{JA}$ = 89.4°C/W

ESD ..... 2000V min

***Notes:***

1. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*
2. *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100ms.*
3. *$V_{DD}$ refers to $AV_{DD}$ and $DV_{DD}$. GND refers to AGND and DGND*

## APPLICATION SECTION

### Voltage References

The top ladder voltage for the XRD64L43 can be provided from an internal bandgap reference. The bandgap reference and its feedback path, Pins 1 and 2 respectively, can be used to set the voltage for VRHF. Select Rf and Ri (if gain is necessary) so that VRHF=VBG(1+Rf/Ri). The internal bandgap voltage is 1.24 volts. The XRD64L43 has a low impedence ladder, therefore, the typical value for Rf and Ri is 10K (Rf and Ri are recommended to be greater than 5K).See Figure 2. for a simplified diagram. Decoupling caps on the sense inputs to AGND should be used to reduce injectioin of high-frequency noise.

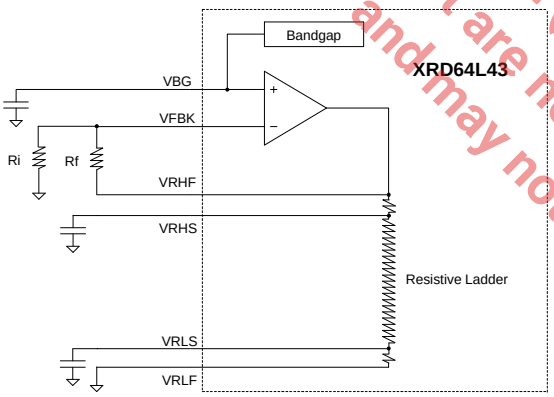



**Figure 2. Voltage Reference Generated from the Internal Bandgap Voltage w/gain**

External voltage references can be forced at VRHF and VRLF. If VRHF and VRLF are driven externally, VFBK should be connected to AVdd, which tri-states the bandgap reference. Direct inputs or inputs driven by external amplifiers can be used to drive the ladder reference voltages of the XRD64L43. See Figure 3. for a simplified diagram. The sense inputs are intended for sensing purposes only and care must be taken to insure that no current flow be present in the sense lines.

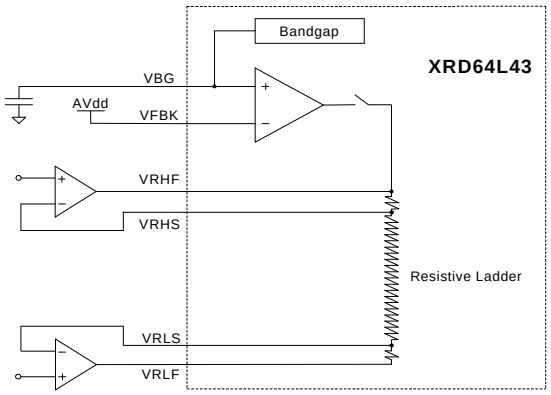



**Figure 3. Voltage Reference Provided by an External Source as Direct Inputs**

### Single-Ended Inputs

The XRD64L43 can be used in either single-ended or differential input mode. For differential inputs, see the Differential Inputs Section. Single-ended inputs minimize the amount of external components necessary to interface with the XRD64L43. The common inputs, VINA(-) and VINB(-) should be tied to ground. VINA(+) and VINB(+) can be used to apply direct inputs to the XRD64L43. Figure 4. is a simplied diagram for single-ended inputs. Pin 16, DIFF should be held low to select single-ended inputs.

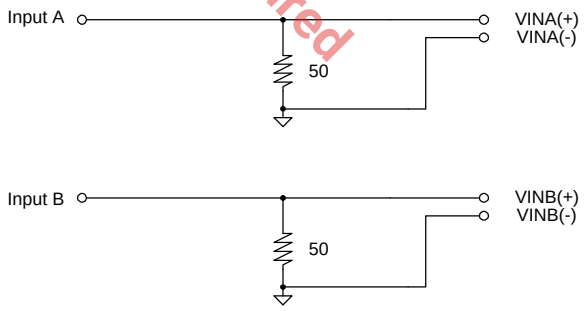



**Figure 4. Single-Ended Inputs for the XRD64L43**

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### Differential Inputs

The XRD64L43 can be used in either differential or single-ended input mode. For single-ended inputs, see the Single-Ended Inputs Section. Differential inputs reduce system noise by removing noise components common at both input pins. Figure 5. is a simplified diagram that is used as a common test circuit with our XRD64L43ES application board. This circuit is used to evaluate the dynamic performance of the XRD64L43 using differential inputs. Pin 16, DIFF should be held high to select differential inputs.

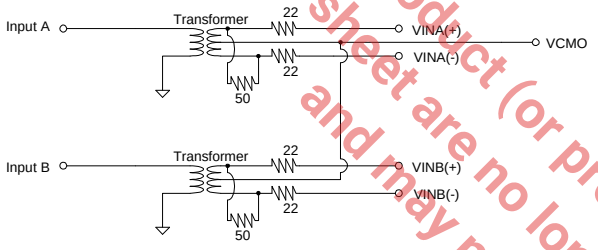



**Figure 5. Common Test Circuit for the Differential Input Mode**

### SYNCO, Data Valid Delay and Latency

SYNCO is an output pin provided by the XRD64L43. Valid data is available on the rising edge of SYNCO, see Figure 6. The Latency for the XRD64L43 is 17 clock cycles.

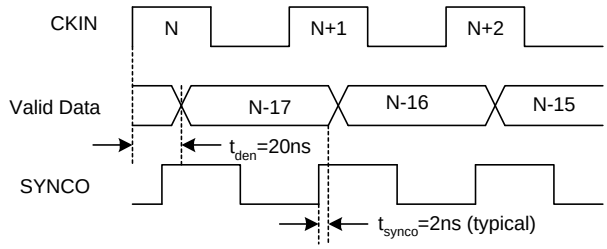



**Figure 6. SYNCO, Data Valid Delay and Latency for the XRD64L43**

### Auto-Calibration

The XRD64L43 incorporates an auto-calibration circuit which continuously adjusts and matches the offset and linearity of each ADC. This auto-calibration circuit is transparent to the user after the initial 4.2ms calibration (168,000 initial clock cycles).

***Note:*** *To avoid auto-calibration after power down, do not disable CKIN. CKIN can be slowed down significantly to save power without losing calibration.*

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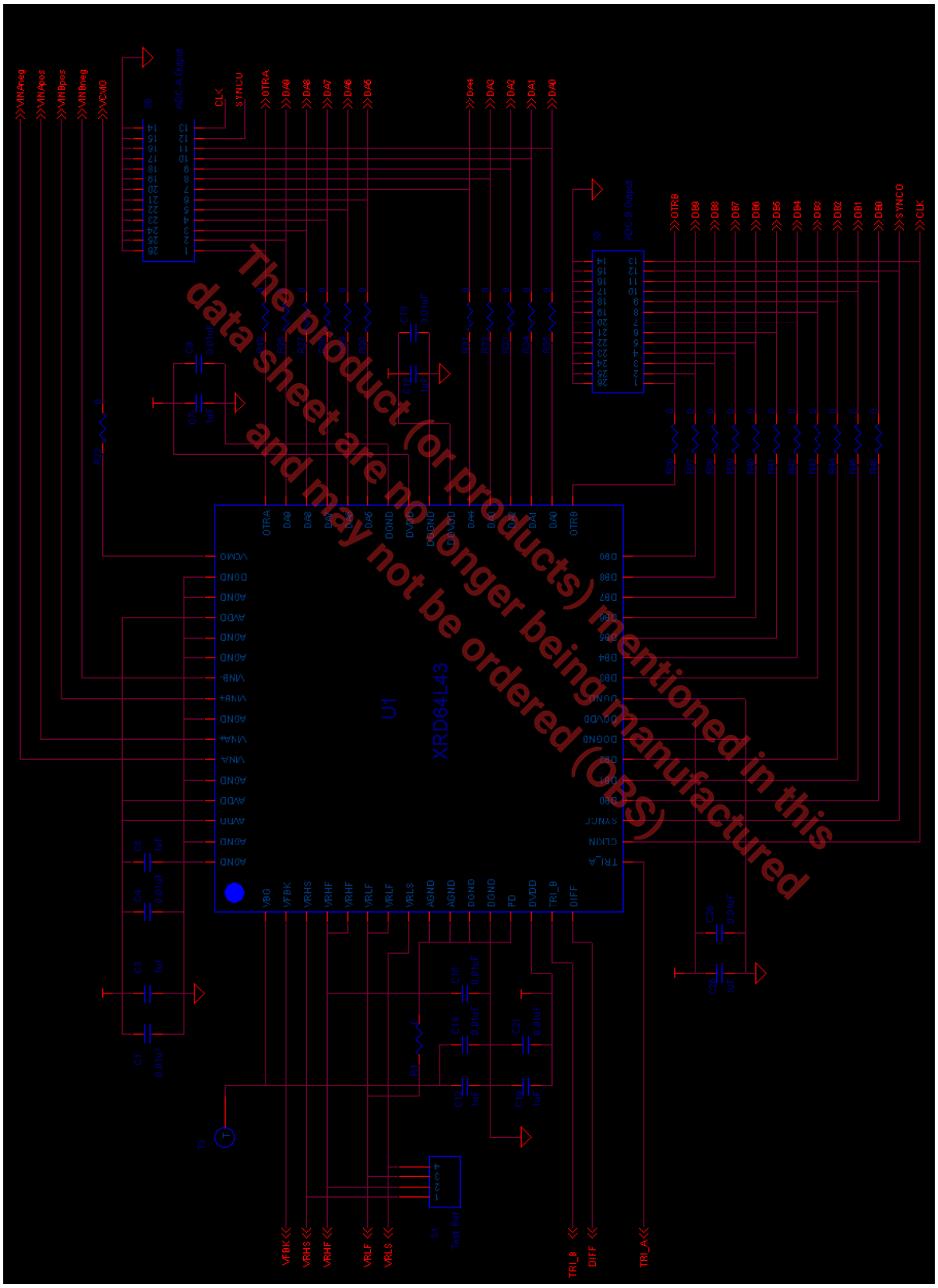
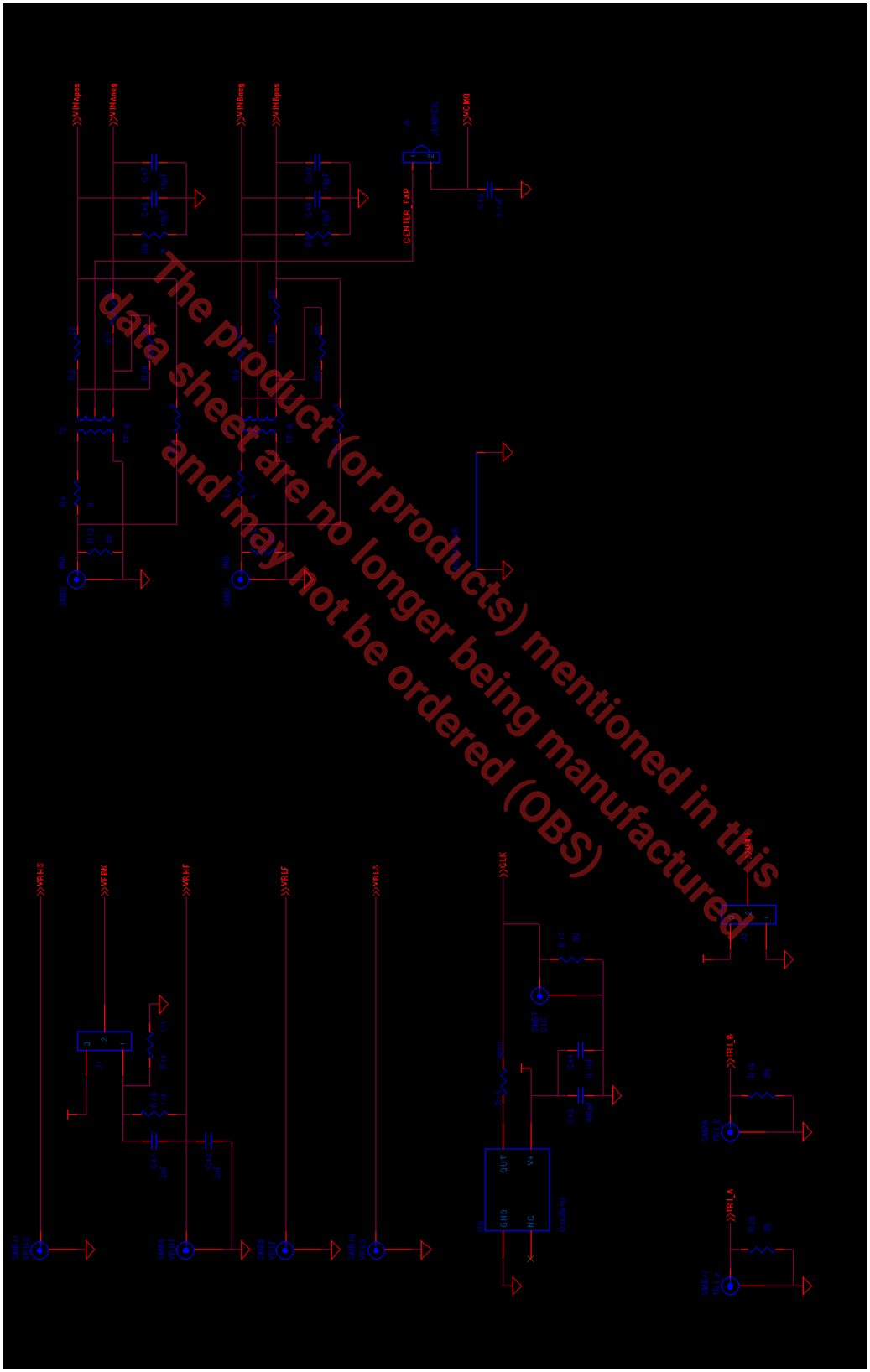



**Figure 7a. XRD64L43ES - Application Circuit for the XRD64L43**




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Figure 7b. XRD64L43ES - Application Circuit for the XRD64L43

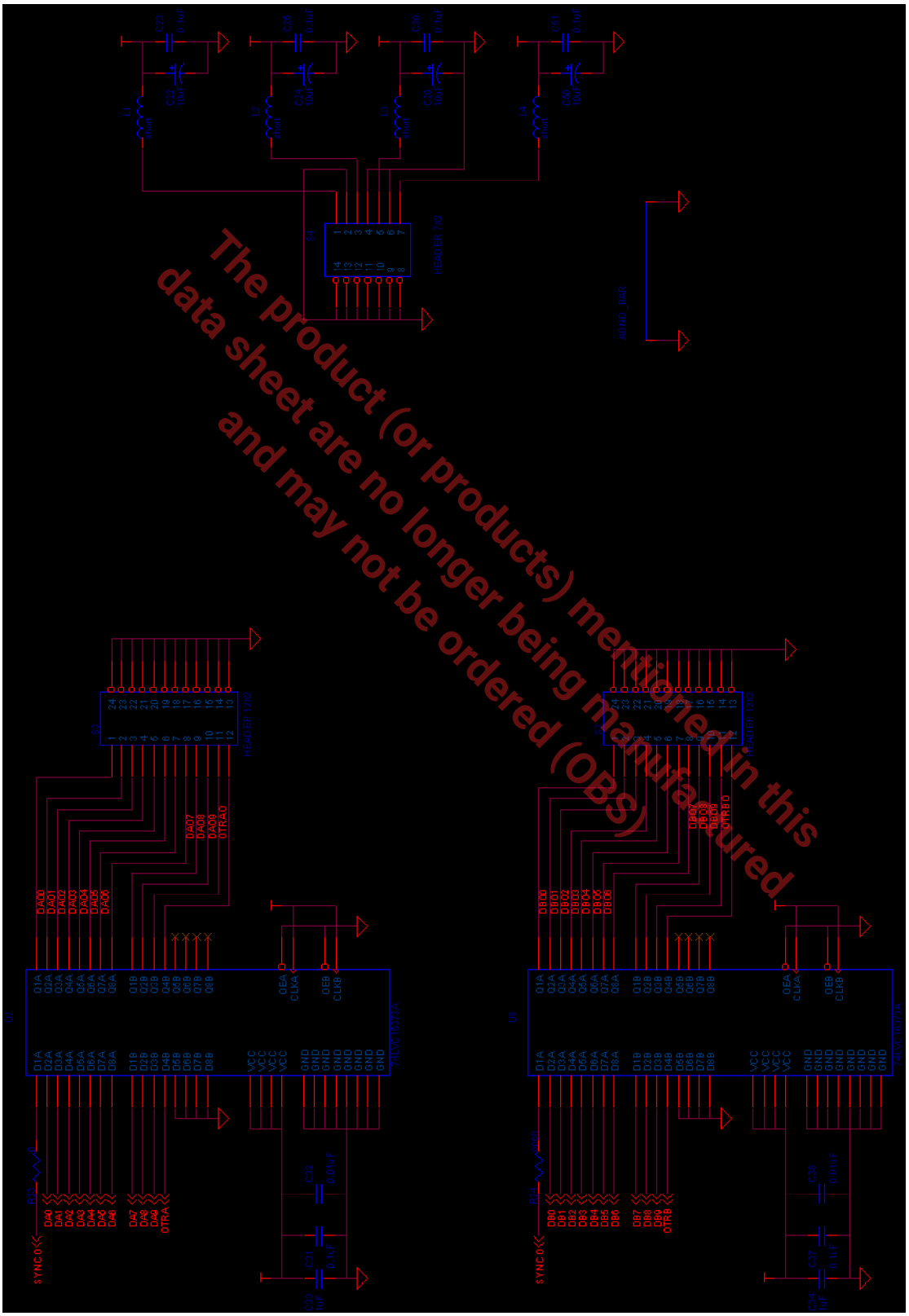



**Figure 7c. XRD64L43ES - Application Circuit for the XRD64L43**

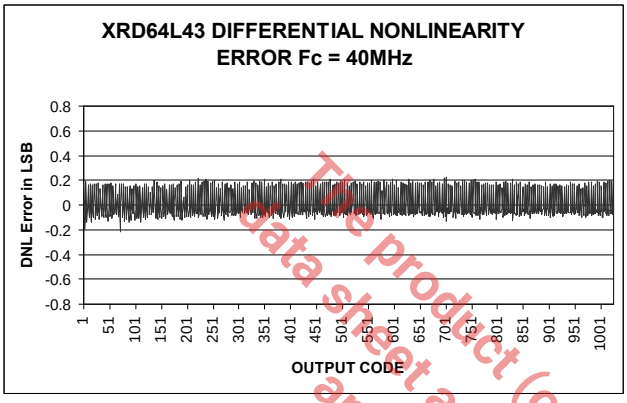



**Figure 8. Differential Non-Linearity, Differential Input Mode, Fc=40MHz, Fin=1.5kHz, VRHF=2.5V, $V_{DD}$=3V**

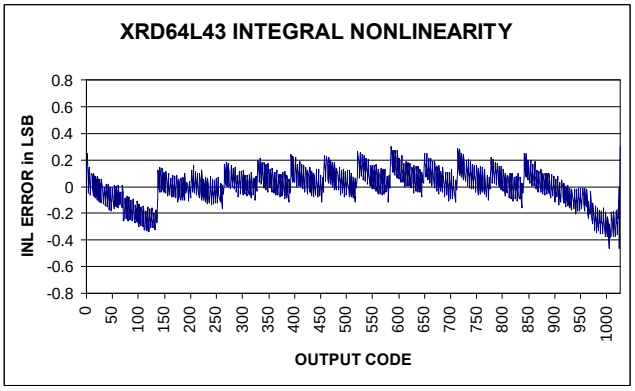



**Figure 9. Integral Non-Linearity, Differential Input Mode, Fc=40MHz, Fin=1.5kHz, VRHF=2.5V, $V_{DD}$=3V**

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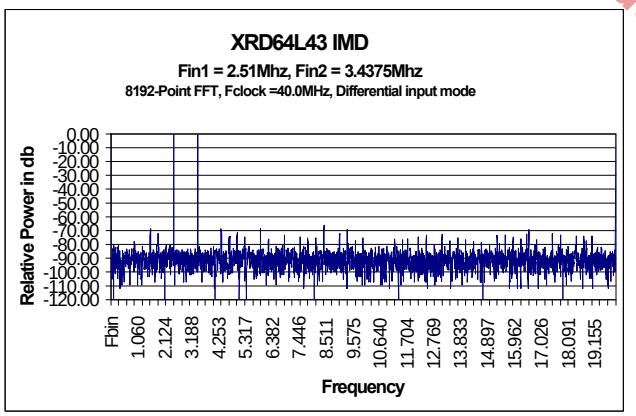



**Figure 10. Intermodulation Distortion, Fin1=2.51MHz, Fin2=3.4375MHz, 8192-point FFT, Fc=40MHz, Differential Input Mode**

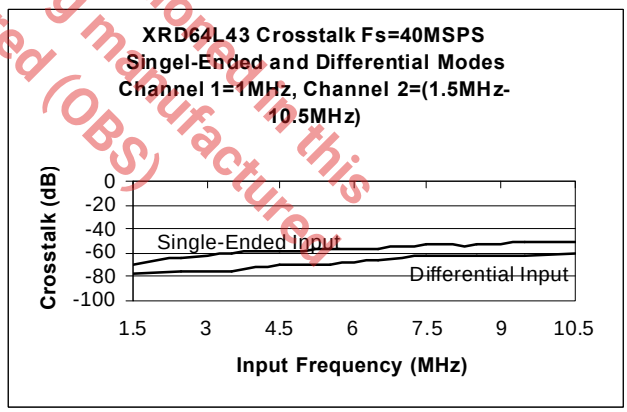



**Figure 11. Crosstalk vs Input Frequency, $V_{DD}$=3V, Differential and Single Ended Inputs**

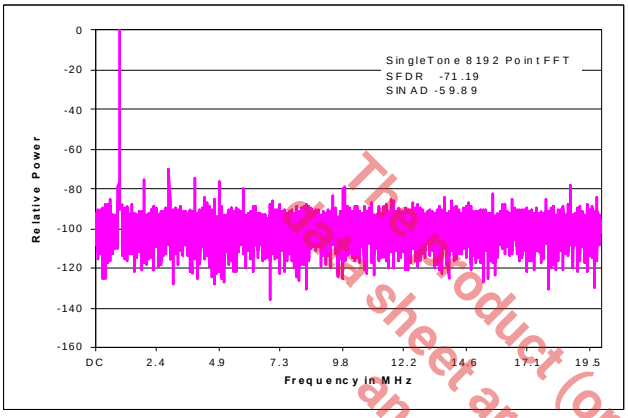



**Figure 12. FFT Spectrum @Fclock = 40.0MHz, Fin = 1.0MHz, DIFFERENTIAL INPUT MODE**

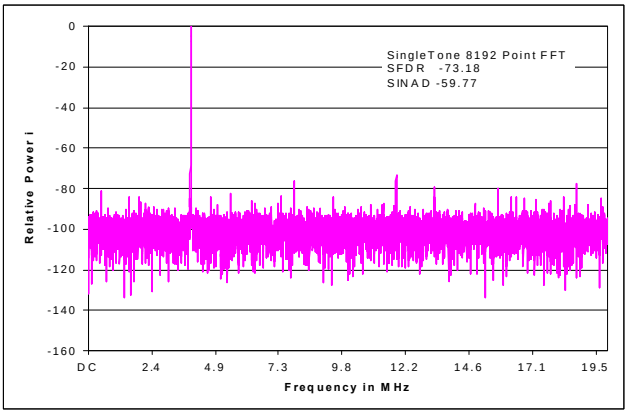



**Figure 13. FFT Spectrum @Fclock = 40.0MHz, Fin = 4.0MHz, DIFFERENTIAL INPUT MODE**

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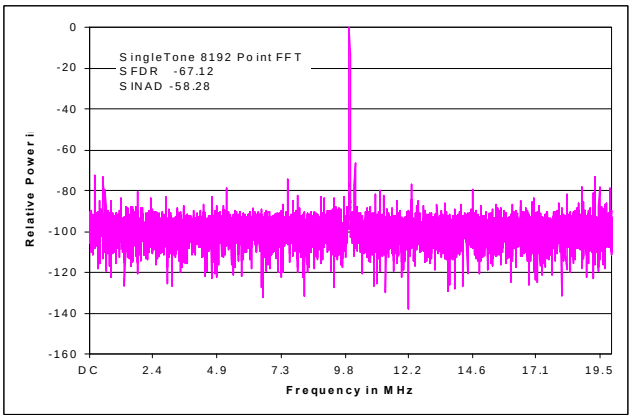



**Figure 14. FFT Spectrum @Fclock = 40.0MHz, Fin = 10.0MHz, DIFFERENTIAL INPUT MODE**

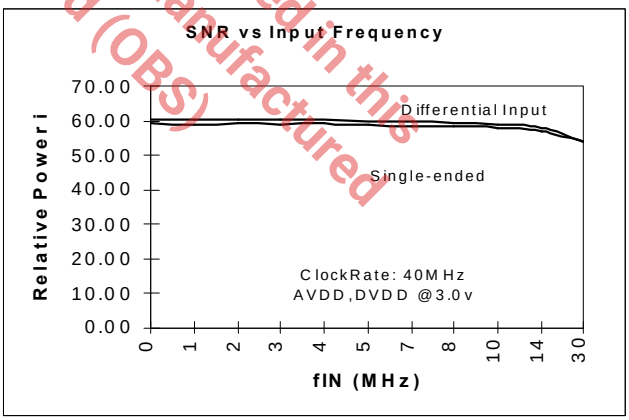



**Figure 15. SNR vs Input Frequency, Differential and Single Ended Inputs, $V_{DD}$=3V**

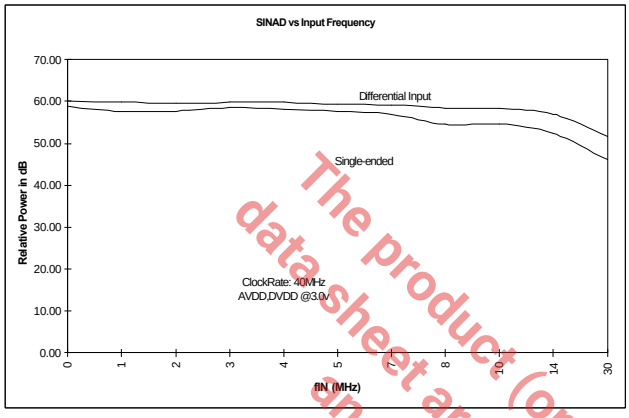



Figure 16. SINAD vs Input Frequency, Differential and Single Ended Inputs, $V_{DD}$=3V

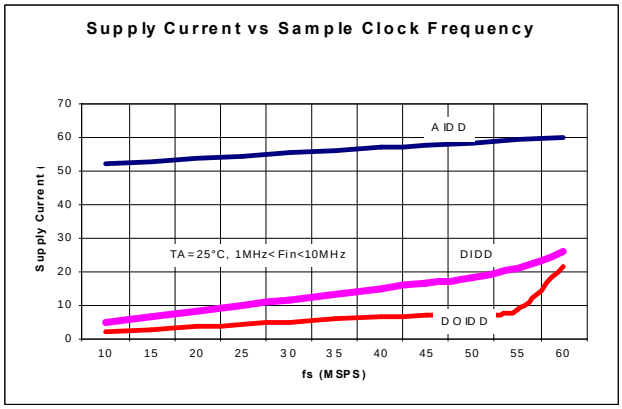



Figure 17. Supply Current vs Sample Clock Frequency

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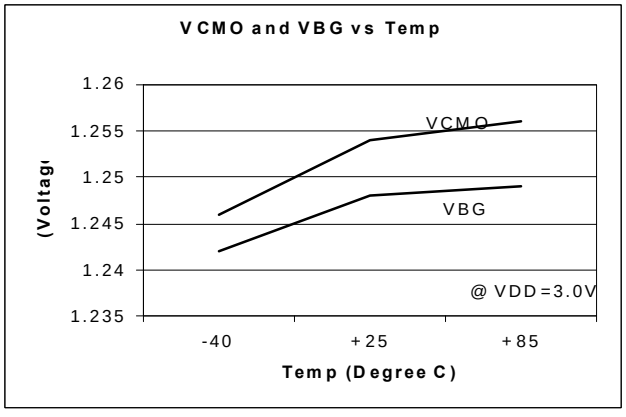



Figure 18. VCMO and VBG vs Temperature

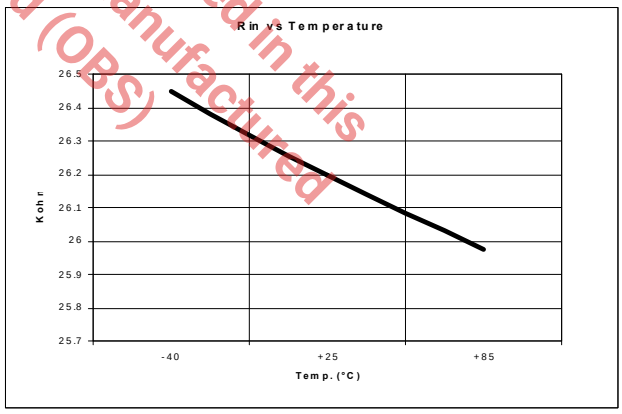
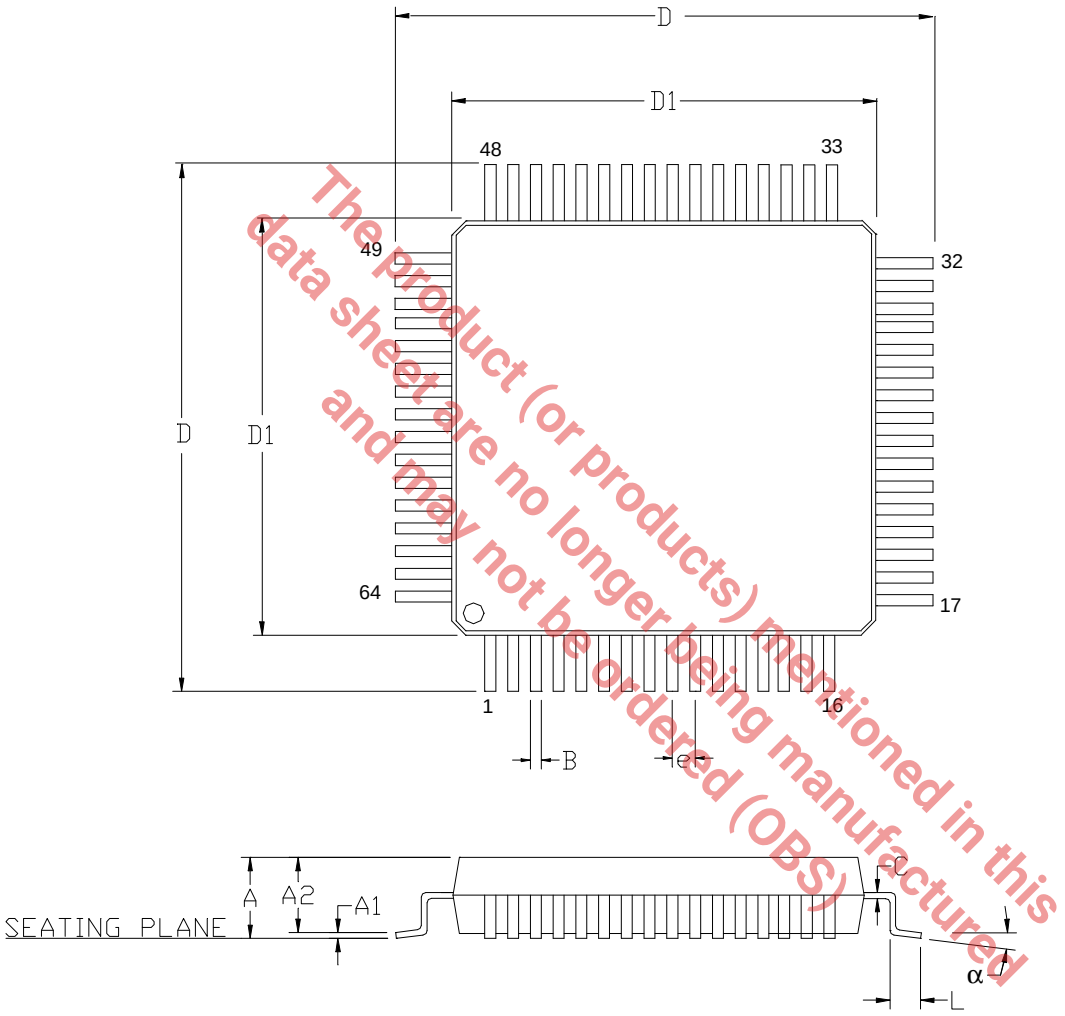



Figure 19. Rin of VINA+, VINB+ vs Temperature at Fc=40MSPS

## 64 LEAD LOW-PROFILE QUAD FLAT PACK
## (10 mm x 10 mm X 1.4 mm LQFP, 1.0 mm Form)

*Rev. 3.00*




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*Note: The control dimension is in millimeters.*

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| **SYMBOL** | **MIN** | **MAX** | **MIN** | **MAX** |
| A | 0.055 | 0.063 | 1.40 | 1.60 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.053 | 0.057 | 1.35 | 1.45 |
| B | 0.007 | 0.011 | 0.17 | 0.27 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.465 | 0.480 | 11.80 | 12.20 |
| D1 | 0.390 | 0.398 | 9.90 | 10.10 |
| e | 0.020 BSC | | 0.50 BSC | |
| L | 0.018 | 0.030 | 0.45 | 0.75 |
| α | 0° | 7° | 0° | 7° |

## Notes

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