

Low Voltage, Rail-to-Rail Operational Amplifiers

MC33201, MC33202, MC33204, NCV33201, NCV33202, NCV33204

The MC33201/2/4 family of operational amplifiers provide rail-to-rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (± 0.9 V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

Features

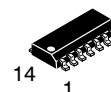
- Low Voltage, Single Supply Operation
(+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over-driven Input Signals
- High Output Current ($I_{SC} = 80$ mA, Typ)
- Low Supply Current ($I_D = 0.9$ mA, Typ)
- 600 Ω Output Drive Capability
- Extended Operating Temperature Ranges
(-40° to $+105^\circ\text{C}$ and -55° to $+125^\circ\text{C}$)
- Typical Gain Bandwidth Product = 2.2 MHz
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant



SOIC-8
D, VD SUFFIX
CASE 751



Micro8
DM SUFFIX
CASE 846A



SOIC-14
D, VD SUFFIX
CASE 751A



TSSOP-14
DTB SUFFIX
CASE 948G

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 10 of this data sheet.

PIN CONNECTIONS

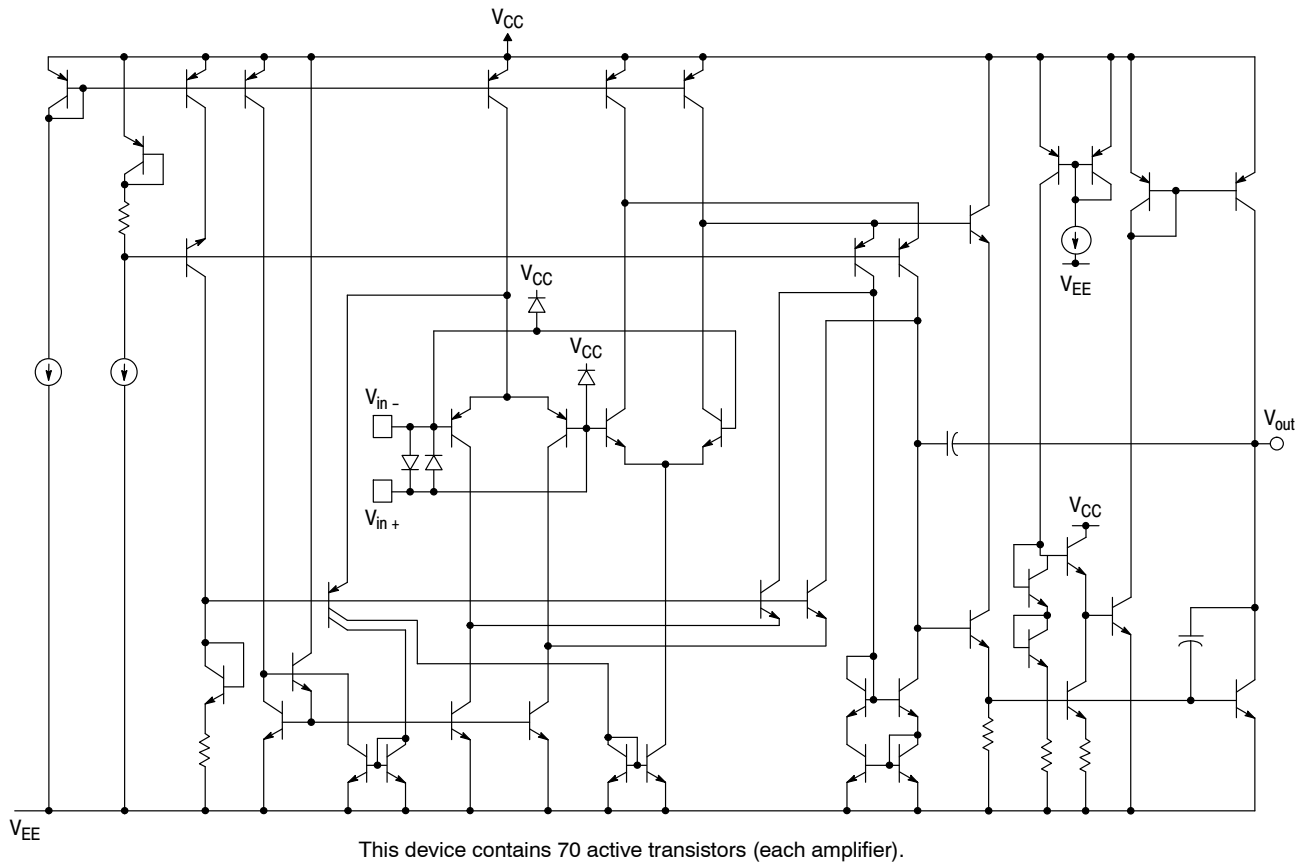
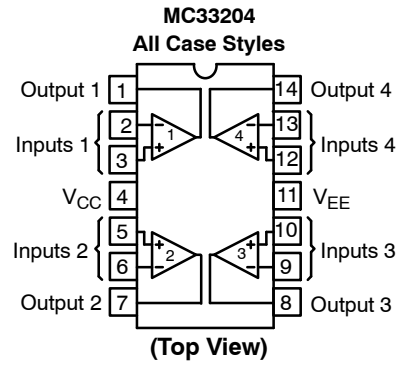
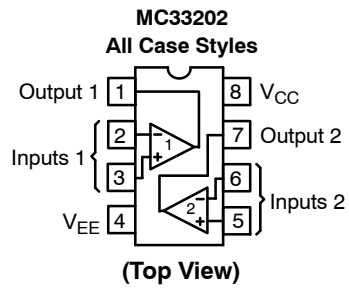
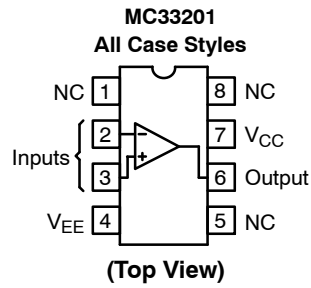


Figure 1. Circuit Schematic
(Each Amplifier)

MC33201, MC33202, MC33204, NCV33201, NCV33202, NCV33204

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+13	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Common Mode Input Voltage Range (Note 2)	V_{CM}	$V_{CC} + 0.5$ V to $V_{EE} - 0.5$ V	V
Output Short Circuit Duration	t_s	Note 3	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	- 65 to +150	°C
Maximum Power Dissipation	P_D	Note 3	mW

DC ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Characteristic	$V_{CC} = 2.0$ V	$V_{CC} = 3.3$ V	$V_{CC} = 5.0$ V	Unit
Input Offset Voltage $V_{IO}(\text{max})$ MC33201, NCV33201V MC33202, NCV33202, V MC33204, NCV33204, V	± 8.0 ± 10 ± 12	± 8.0 ± 10 ± 12	± 6.0 ± 8.0 ± 10	mV
Output Voltage Swing V_{OH} ($R_L = 10$ k Ω) V_{OL} ($R_L = 10$ k Ω)	1.9 0.10	3.15 0.15	4.85 0.15	$V_{\min}$ $V_{\max}$
Power Supply Current per Amplifier (I_D)	1.125	1.125	1.125	mA

Specifications at $V_{CC} = 3.3$ V are guaranteed by the 2.0 V and 5.0 V tests. $V_{EE} = \text{GND}$.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0$ V, $V_{EE} = \text{Ground}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($V_{CM} = 0$ V to 0.5 V, $V_{CM} = 1.0$ V to 5.0 V) MC33201/NCV33201V: $T_A = +25^\circ\text{C}$ MC33201: $T_A = -40^\circ$ to $+105^\circ\text{C}$ MC33201V/NCV33201V: $T_A = -55^\circ$ to $+125^\circ\text{C}$ MC33202/NCV33202, V: $T_A = +25^\circ\text{C}$ MC33202/NCV33202: $T_A = -40^\circ$ to $+105^\circ\text{C}$ MC33202V/NCV33202V: $T_A = -55^\circ$ to $+125^\circ\text{C}$ (Note 4) MC33204/NCV33204V: $T_A = +25^\circ\text{C}$ MC33204: $T_A = -40^\circ$ to $+105^\circ\text{C}$ MC33204V/NCV33204V: $T_A = -55^\circ$ to $+125^\circ\text{C}$ (Note 4)	3	$ V_{IO} $	- - - - - - - -	- - - - - - - -	6.0 9.0 13 8.0 11 14 10 13 17	mV
Input Offset Voltage Temperature Coefficient ($R_S = 50$ Ω) $T_A = -40^\circ$ to $+105^\circ\text{C}$ $T_A = -55^\circ$ to $+125^\circ\text{C}$	4	$\Delta V_{IO}/\Delta T$	- -	2.0 2.0	- -	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0$ V to 0.5 V, $V_{CM} = 1.0$ V to 5.0 V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+105^\circ\text{C}$ $T_A = -55^\circ$ to $+125^\circ\text{C}$	5, 6	$ I_{IB} $	- - -	80 100 -	200 250 500	nA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The differential input voltage of each amplifier is limited by two internal parallel back-to-back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 2)
4. All NCV devices are qualified for Automotive use.

MC33201, MC33202, MC33204, NCV33201, NCV33202, NCV33204

DC ELECTRICAL CHARACTERISTICS (cont.) ($V_{CC} = +5.0\text{ V}$, $V_{EE} = \text{Ground}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Current ($V_{CM} = 0\text{ V to } 0.5\text{ V}$, $V_{CM} = 1.0\text{ V to } 5.0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to } +105^\circ\text{C}$ $T_A = -55^\circ\text{ to } +125^\circ\text{C}$	–	$ I_{IO} $	– – –	5.0 10 –	50 100 200	nA
Common Mode Input Voltage Range	–	V_{ICR}	V_{EE}	–	V_{CC}	V
Large Signal Voltage Gain ($V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$) $R_L = 10\text{ k}\Omega$ $R_L = 600\text{ }\Omega$	7	A_{VOL}	50 25	300 250	– –	kV/V
Output Voltage Swing ($V_{ID} = \pm 0.2\text{ V}$) $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ $R_L = 600\text{ }\Omega$ $R_L = 600\text{ }\Omega$	8, 9, 10	V_{OH} V_{OL} V_{OH} V_{OL}	4.85 – 4.75 –	4.95 0.05 4.85 0.15	– 0.15 – 0.25	V
Common Mode Rejection ($V_{in} = 0\text{ V to } 5.0\text{ V}$)	11	CMR	60	90	–	dB
Power Supply Rejection Ratio $V_{CC}/V_{EE} = 5.0\text{ V/GND to } 3.0\text{ V/GND}$	12	PSRR	500	25	–	$\mu\text{V/V}$
Output Short Circuit Current (Source and Sink)	13, 14	I_{SC}	50	80	–	mA
Power Supply Current per Amplifier ($V_O = 0\text{ V}$) $T_A = -40^\circ\text{ to } +105^\circ\text{C}$ $T_A = -55^\circ\text{ to } +125^\circ\text{C}$	15	I_D	– –	0.9 0.9	1.125 1.125	mA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0\text{ V}$, $V_{EE} = \text{Ground}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_S = \pm 2.5\text{ V}$, $V_O = -2.0\text{ V to } +2.0\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $A_V = +1.0$)	16, 26	SR	0.5	1.0	–	V/ μs
Gain Bandwidth Product ($f = 100\text{ kHz}$)	17	GBW	–	2.2	–	MHz
Gain Margin ($R_L = 600\text{ }\Omega$, $C_L = 0\text{ pF}$)	20, 21, 22	A_M	–	12	–	dB
Phase Margin ($R_L = 600\text{ }\Omega$, $C_L = 0\text{ pF}$)	20, 21, 22	ϕ_M	–	65	–	Deg
Channel Separation ($f = 1.0\text{ Hz to } 20\text{ kHz}$, $A_V = 100$)	23	CS	–	90	–	dB
Power Bandwidth ($V_O = 4.0\text{ V}_{pp}$, $R_L = 600\text{ }\Omega$, $\text{THD} \leq 1\%$)		BW_P	–	28	–	kHz
Total Harmonic Distortion ($R_L = 600\text{ }\Omega$, $V_O = 1.0\text{ V}_{pp}$, $A_V = 1.0$) $f = 1.0\text{ kHz}$ $f = 10\text{ kHz}$	24	THD	– –	0.002 0.008	– –	%
Open Loop Output Impedance ($V_O = 0\text{ V}$, $f = 2.0\text{ MHz}$, $A_V = 10$)		$ Z_O $	–	100	–	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)		R_{in}	–	200	–	k Ω
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)		C_{in}	–	8.0	–	pF
Equivalent Input Noise Voltage ($R_S = 100\text{ }\Omega$) $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	25	e_n	– –	25 20	– –	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	25	i_n	– –	0.8 0.2	– –	pA/ $\sqrt{\text{Hz}}$

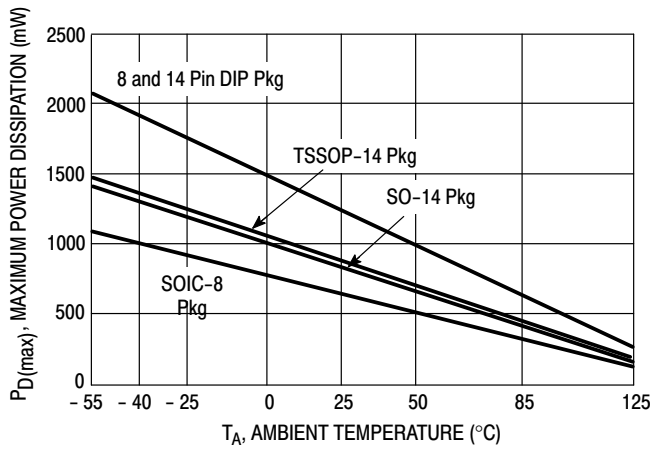


Figure 2. Maximum Power Dissipation versus Temperature

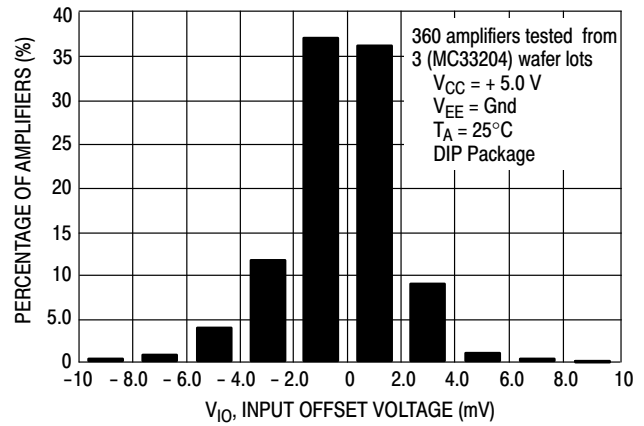


Figure 3. Input Offset Voltage Distribution

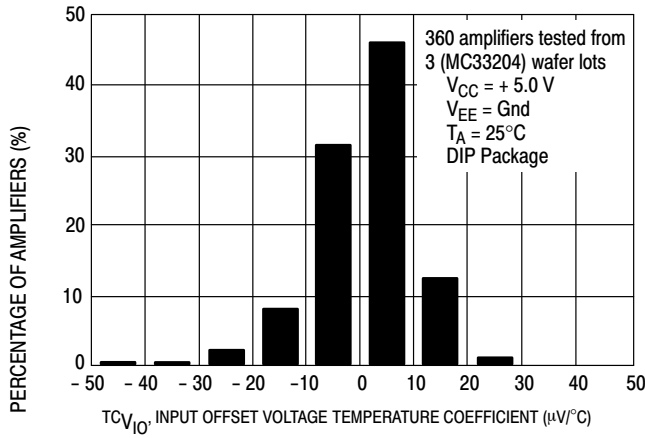


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

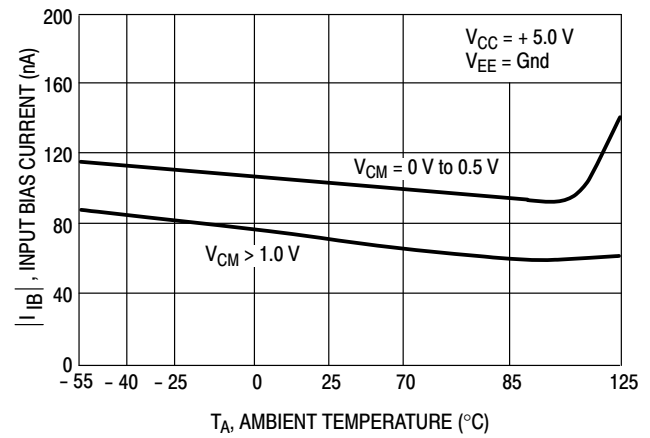


Figure 5. Input Bias Current versus Temperature

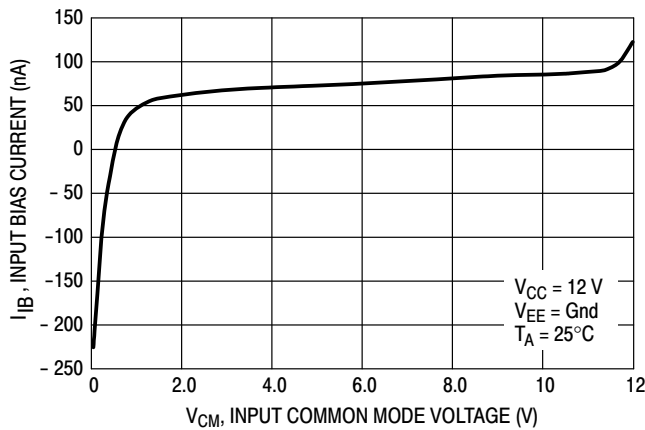


Figure 6. Input Bias Current versus Common Mode Voltage

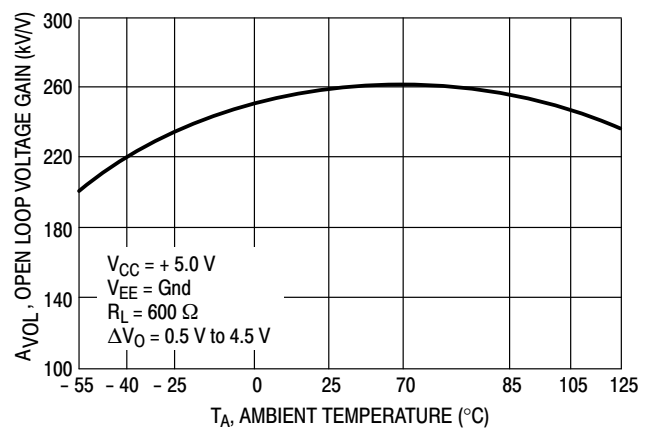


Figure 7. Open Loop Voltage Gain versus Temperature

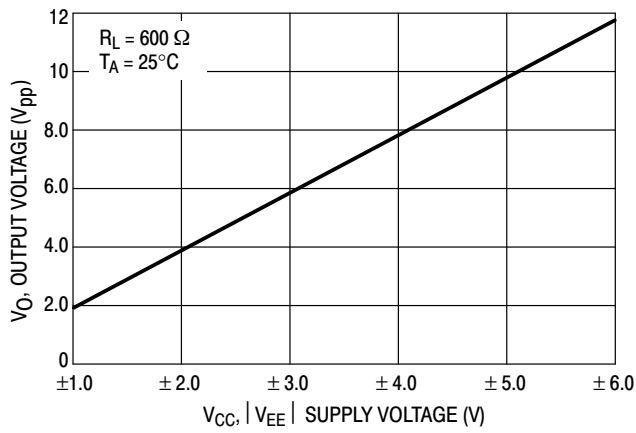


Figure 8. Output Voltage Swing versus Supply Voltage

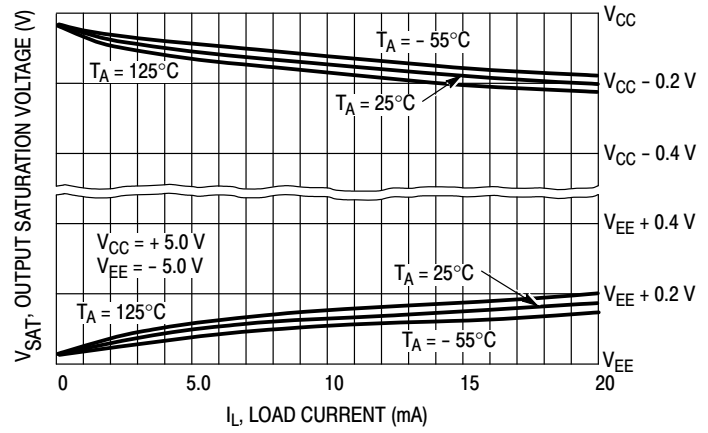


Figure 9. Output Saturation Voltage versus Load Current

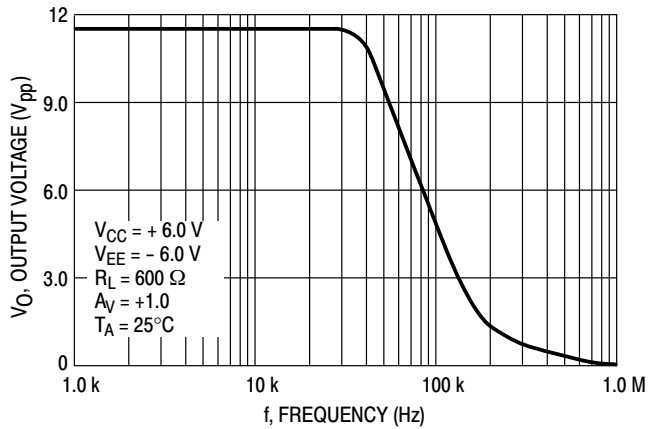


Figure 10. Output Voltage versus Frequency

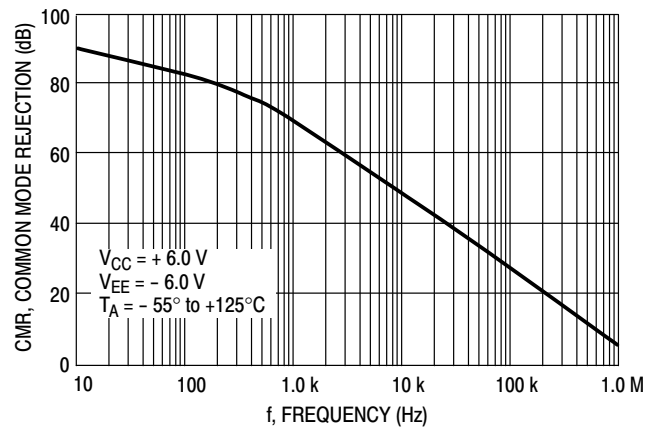


Figure 11. Common Mode Rejection versus Frequency

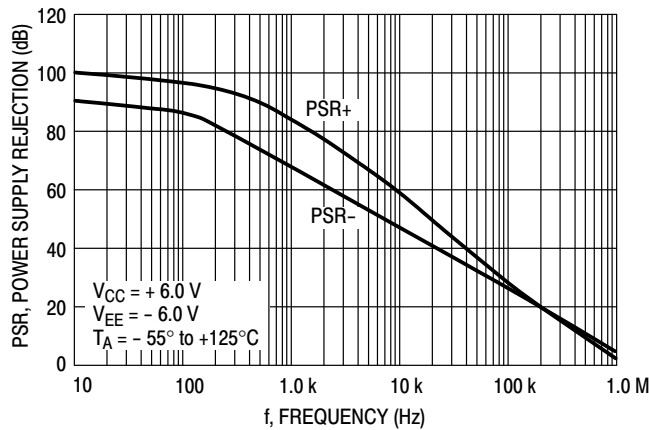


Figure 12. Power Supply Rejection versus Frequency

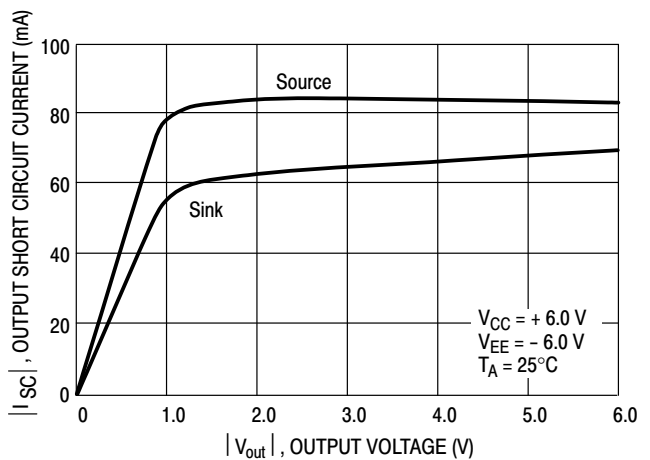


Figure 13. Output Short Circuit Current versus Output Voltage

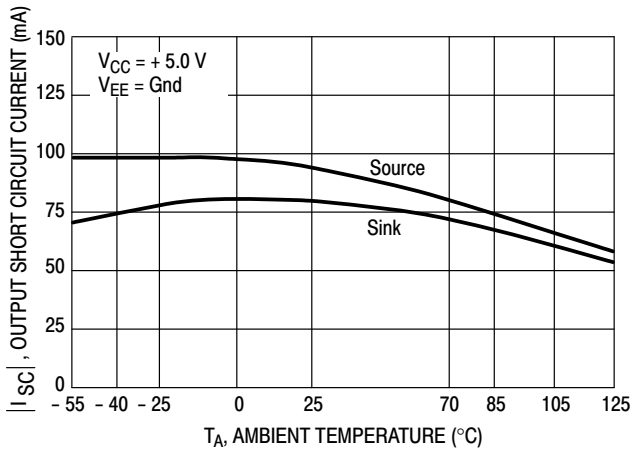


Figure 14. Output Short Circuit Current versus Temperature

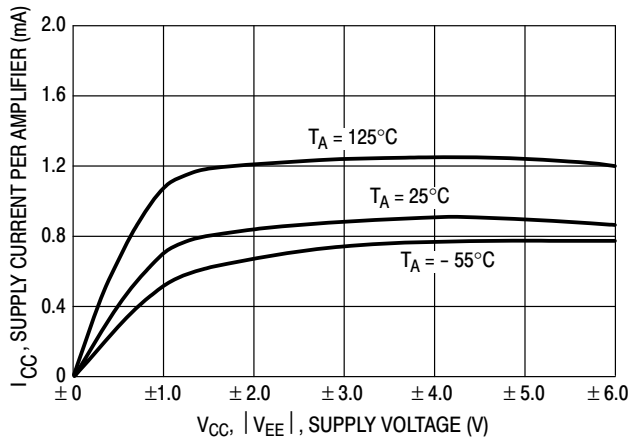


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

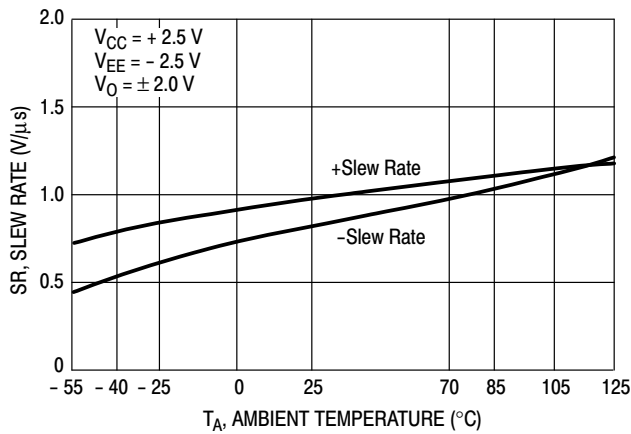


Figure 16. Slew Rate versus Temperature

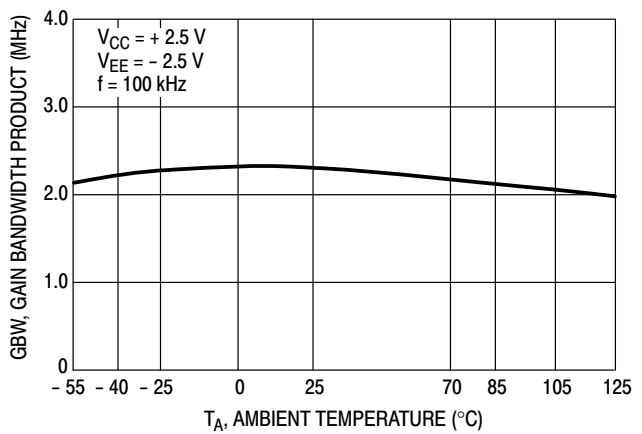


Figure 17. Gain Bandwidth Product versus Temperature

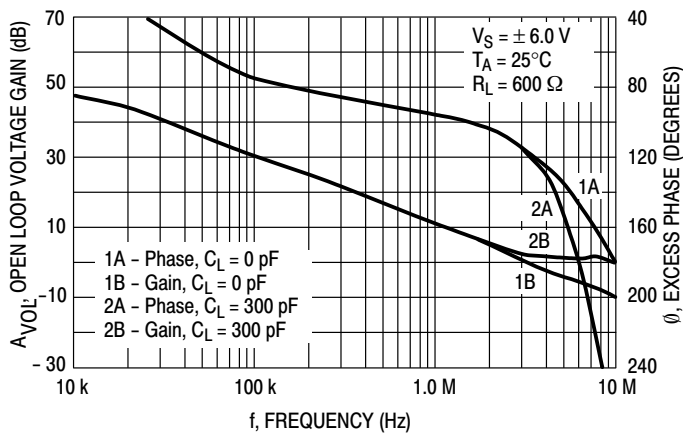


Figure 18. Voltage Gain and Phase versus Frequency

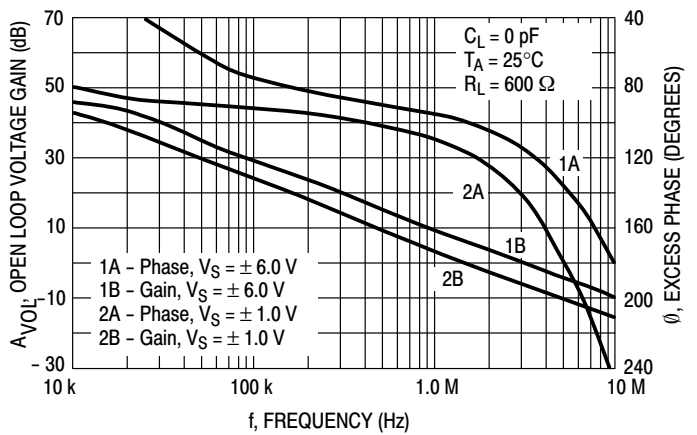


Figure 19. Voltage Gain and Phase versus Frequency

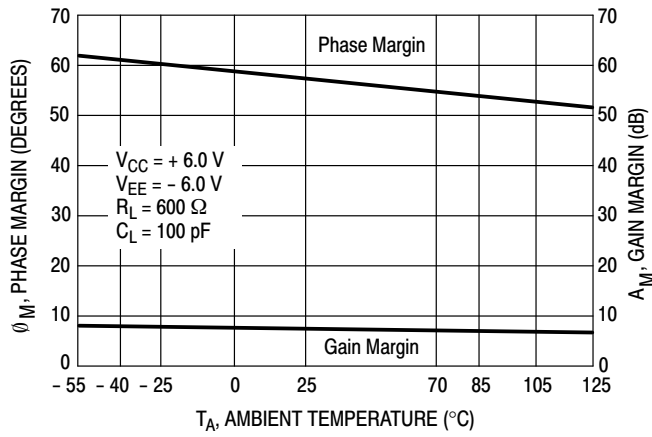


Figure 20. Gain and Phase Margin versus Temperature

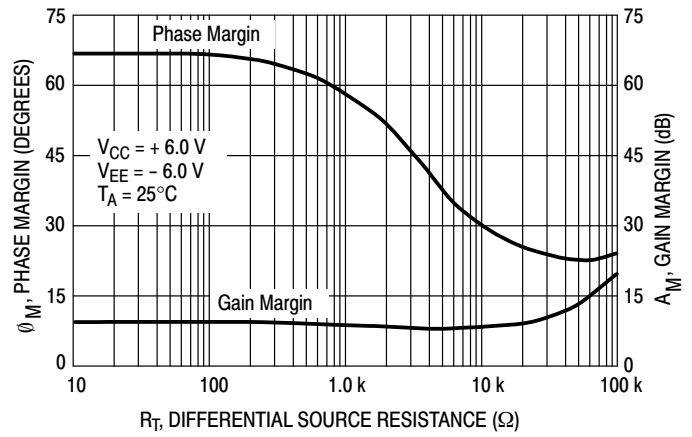


Figure 21. Gain and Phase Margin versus Differential Source Resistance

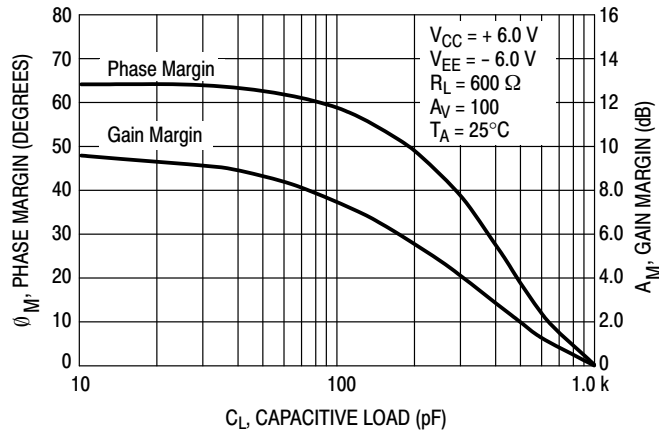


Figure 22. Gain and Phase Margin versus Capacitive Load

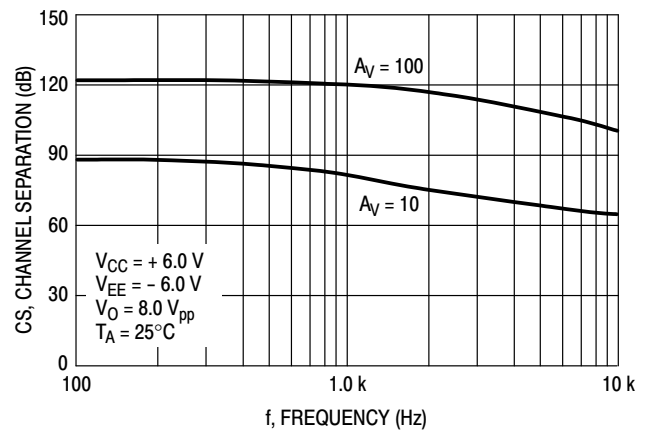


Figure 23. Channel Separation versus Frequency

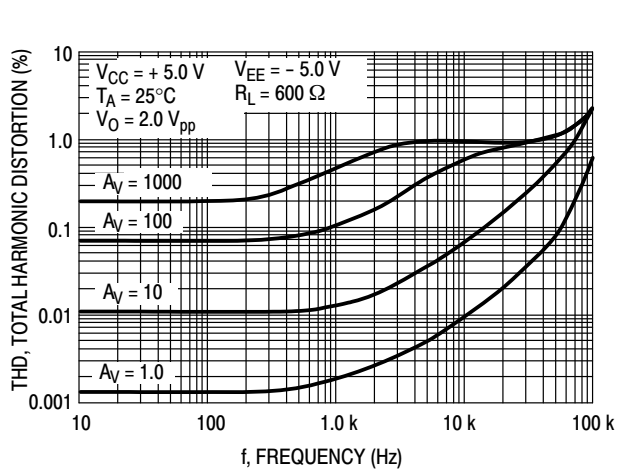


Figure 24. Total Harmonic Distortion versus Frequency

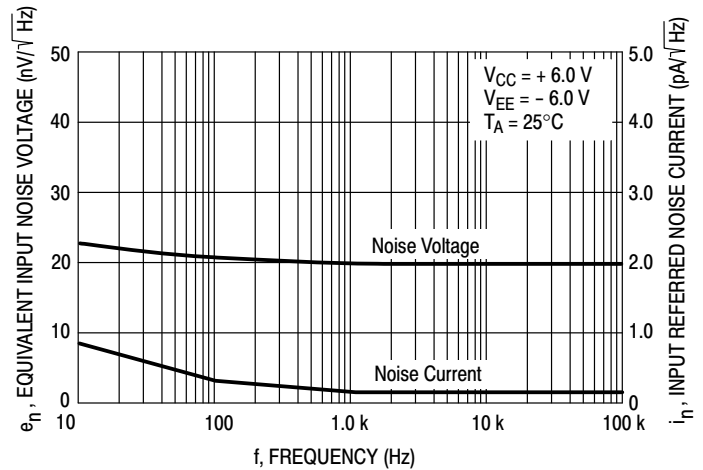


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency

DETAILED OPERATING DESCRIPTION

General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail-to-rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE} , it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail-to-rail performance is achieved at the input of the amplifiers by using parallel NPN-PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE} , the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross-coupling techniques have been used to keep this change to a minimum.

In addition to its rail-to-rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

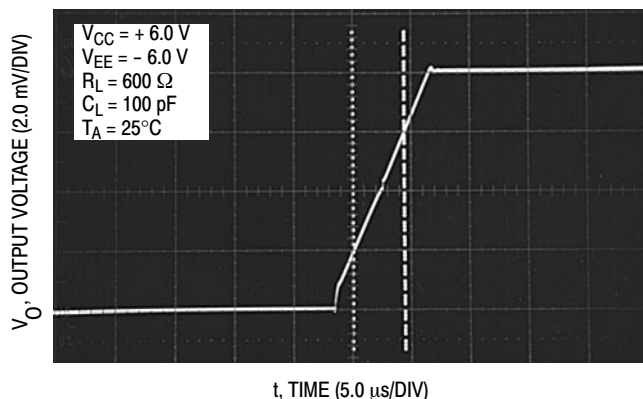


Figure 26. Noninverting Amplifier Slew Rate

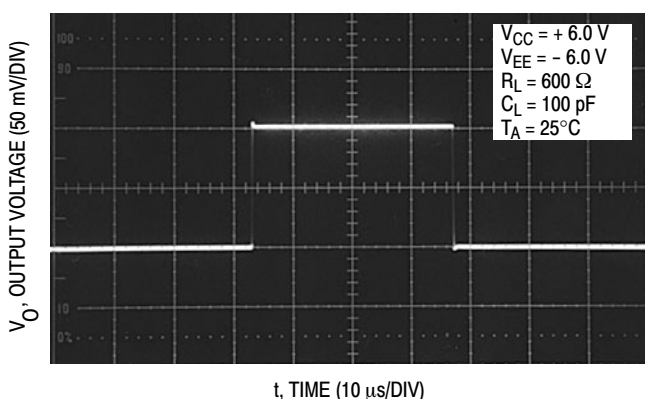


Figure 27. Small Signal Transient Response

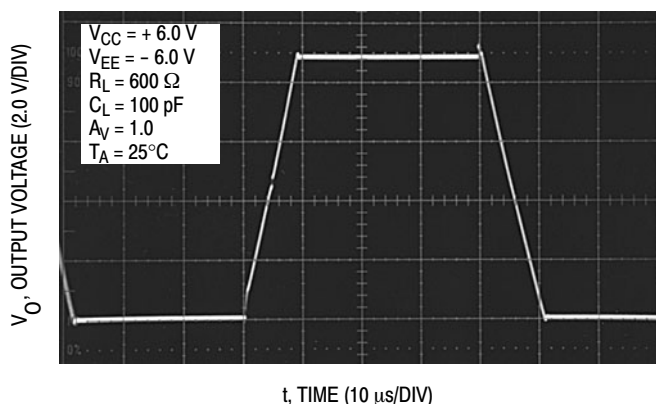


Figure 28. Large Signal Transient Response

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface

between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.

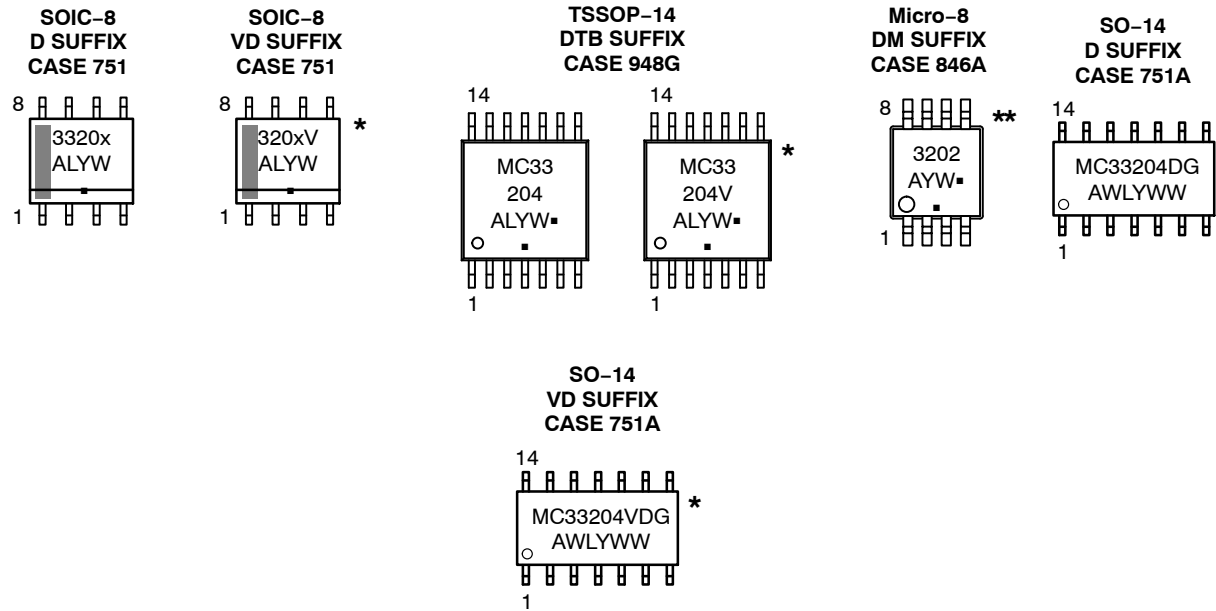
ORDERING INFORMATION

Operational Amplifier Function	Device	Operating Temperature Range	Package	Shipping†
Single	MC33201DR2G	$T_A = -40^{\circ}$ to $+105^{\circ}\text{C}$	SOIC-8 (Pb-Free)	2500 / Tape & Reel
	MC33201VDR2G	$T_A = -55^{\circ}$ to 125°C		2500 / Tape & Reel
	NCV33201VDR2G			2500 / Tape & Reel
Dual	MC33202DR2G	$T_A = -40^{\circ}$ to $+105^{\circ}\text{C}$	SOIC-8 (Pb-Free)	2500 / Tape & Reel
	MC33202DMR2G		Micro-8 (Pb-Free)	4000 / Tape & Reel
	NCV33202DMR2G*			
	MC33202VDR2G	$T_A = -55^{\circ}$ to 125°C	SOIC-8 (Pb-Free)	2500 / Tape & Reel
	NCV33202VDR2G*			
Quad	MC33204DR2G	$T_A = -40^{\circ}$ to $+105^{\circ}\text{C}$	SO-14 (Pb-Free)	2500 Units / Tape & Reel
	MC33204DTBR2G		TSSOP-14 (Pb-Free)	2500 Units / Tape & Reel
	NCV33204DR2G*	$T_A = -55^{\circ}$ to 125°C	SO-14 (Pb-Free)	2500 Units / Tape & Reel
	NCV33204DTBR2G*		TSSOP-14 (Pb-Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MARKING DIAGRAMS

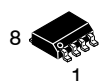


x = 1 or 2
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package
■ = Pb-Free Package

(Note: Microdot may be in either location)

*This marking diagram applies to NCV3320xV

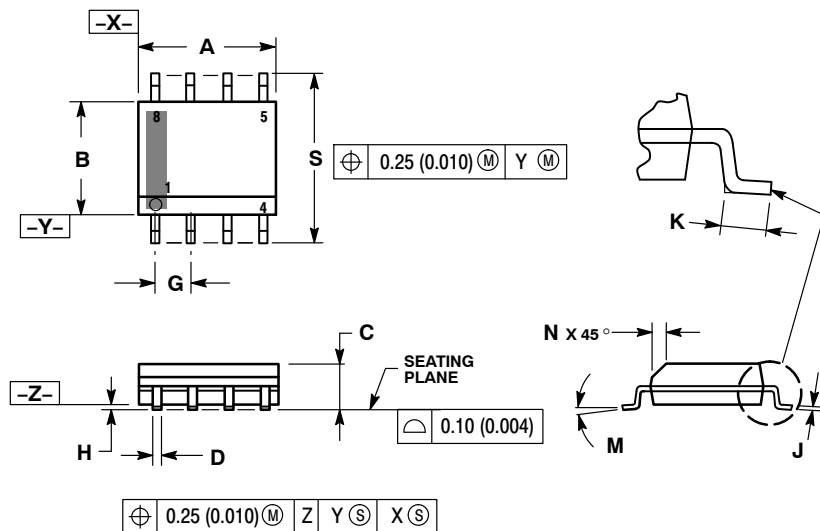
**This marking diagram applies to NCV33202DMR2G



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

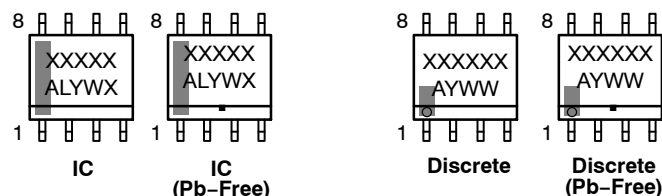
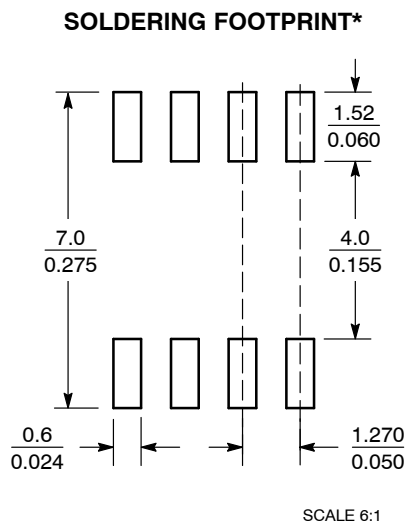


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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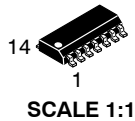
SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

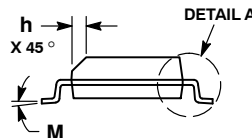
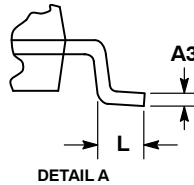
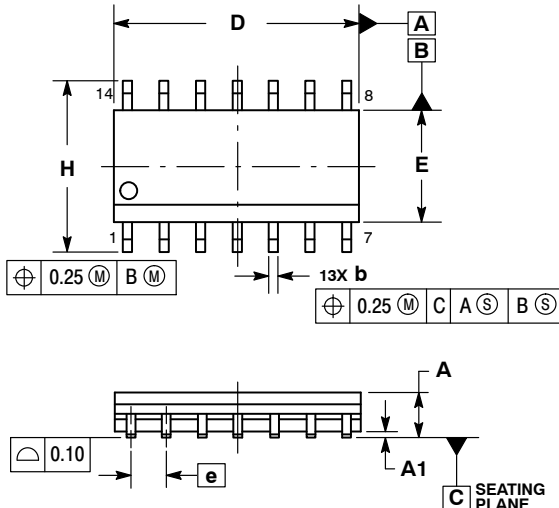
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SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

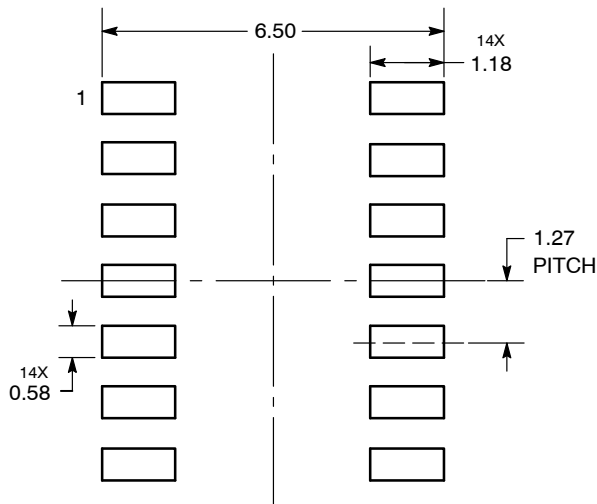


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

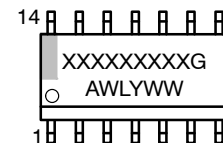
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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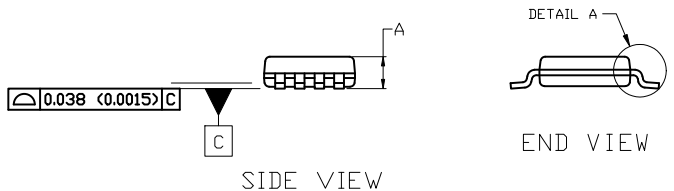
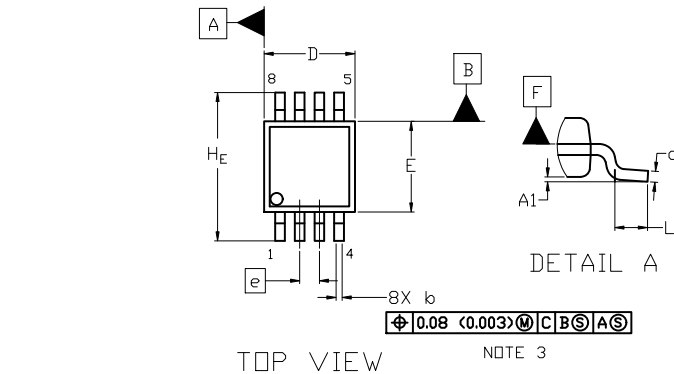
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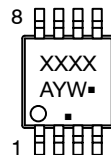
SCALE 2:1

Micro8
CASE 846A-02
ISSUE K

DATE 16 JUL 2020



GENERIC
MARKING DIAGRAM*



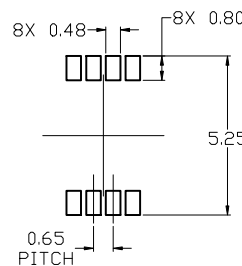
XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F .
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F .
6. $A1$ IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM-10.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H _E	4.75	4.90	5.05
L	0.40	0.55	0.70

STYLE 1:

- PIN 1. SOURCE
- SOURCE
- SOURCE
- GATE
- DRAIN
- DRAIN
- DRAIN
- DRAIN

STYLE 2:

- PIN 1. SOURCE 1
- GATE 1
- SOURCE 2
- GATE 2
- DRAIN 2
- DRAIN 2
- DRAIN 1
- DRAIN 1

STYLE 3:

- PIN 1. N-SOURCE
- N-GATE
- P-SOURCE
- P-GATE
- P-DRAIN
- P-DRAIN
- N-DRAIN
- N-DRAIN

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