A Product Line of
Diodes Incorporated

PI6CL10806/PI6CL10808

6/8 Output Low Voltage 200MHz LVCMOS Clock Buffer with Level Shift

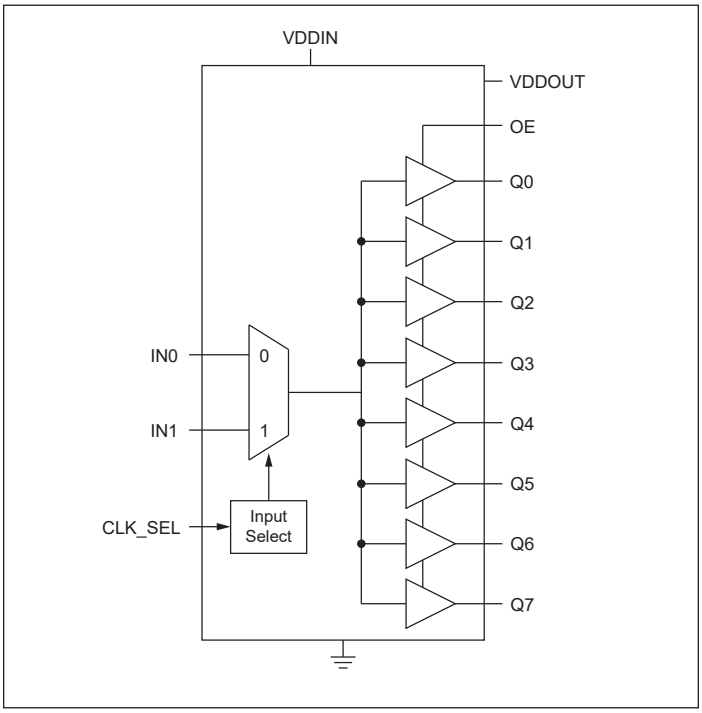
Description

The PI6CL10806/PI6CL10808 is a low voltage high-speed, low-noise non-inverting LVCMOS 6/8 output clock buffer with level translation.

It supports 1.0V to 1.8V power supply. The key goal in designing the PI6CL10806/PI6CL10808 is to target applications that require low voltage power supply, low-jitter, and the capability to bridge the power supply mismatch between clock source and clock sink devices.

It has a built-in LDO that enhances jitter performance in noisy environment. With output-to-output skew as low as 40ps, the PI6CL10806/PI6CL10808 is an ideal clock distribution device for synchronous systems which requires a tight level of skew from a large number of outputs.

Block Diagram



Features

- High-Speed, Low-Noise, Non-Inverting Buffer with 6/8 Outputs
- Maximum Frequency Up to 200MHz
- 1.0 to 1.8V Power Supply
- Low to High or High to Low LVCMOS Clock Level Translation
  - Low to High 0.9V to 1.8V
  - High to Low 1.8V to 1.2V
- 2-input Clock Mux
- Clock Input Power Down Tolerant
- Low Output Skew: <40ps
- Low Propagation Delay: <2ns
- Low Additive Jitter: 90fs RMS (typical)
- Operating Temperature: –40˚C to 105˚C
- Packaging (Pb-free & Green):
  - 16-Pin, QFN 3x3mm
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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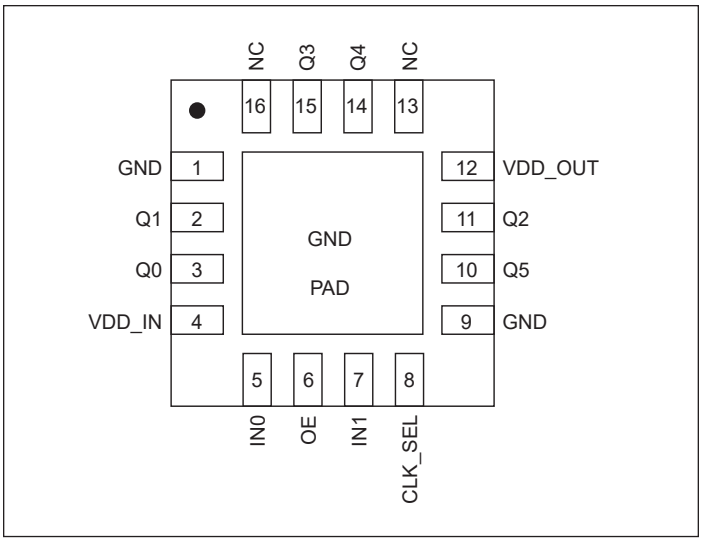
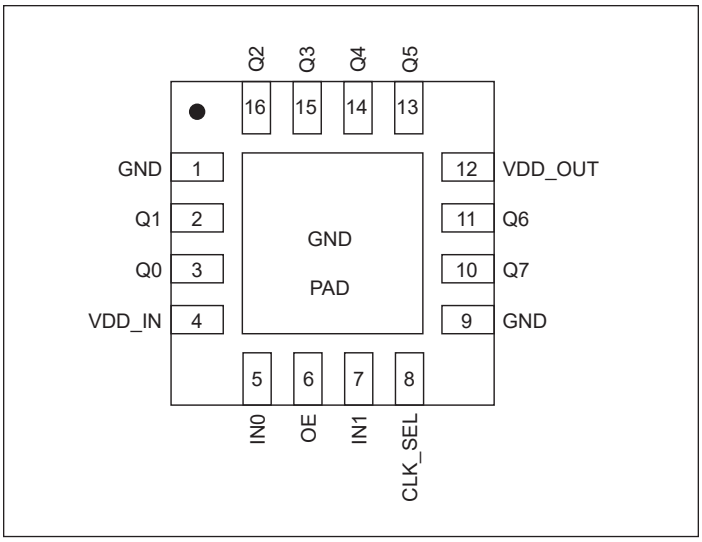
Pin Configuration

PI6CL10806



PI6CL10808



Pin Description

Pin Number		Pin Name	Type	Description
PI6CL10806	PI6CL10808			
5	5	IN0	Input	Input Clock 0.
7	7	IN1	Input	Input Clock 1.
6	6	OE	Input	Output enable. When OE = high, the clock outputs are enabled. When OE = low, the clock outputs are tri-stated. OE has an internal variable pull-up resistor to VDD_OUT, and may be left unconnected.
8	8	CLK_SEL	Input	Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL has an internal variable pull-up resistor to VDD_OUT.
3	3	Q0	Output	Output Clock 0.
2	2	Q1	Output	Output Clock 1.
11	16	Q2	Output	Output Clock 2.
15	15	Q3	Output	Output Clock 3.
14	14	Q4	Output	Output Clock 4.
10	13	Q5	Output	Output Clock 5.
—	11	Q6	Output	Output Clock 6.
—	10	Q7	Output	Output Clock 7.
4	4	VDD_IN	Power	Core voltage supply.
12	12	VDD_OUT	Power	Output voltage supply.
1, 9, ePad	1, 9, ePad	GND	GND	Ground.
13, 16	—	NC		No Connect.

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Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... 150°C Max.
Input Voltage (IN0, IN1) ..... –0.5V to +2.5V
Input Voltage (OE, CLK_SEL) ..... –0.5V to +3.6V
Output Voltage ..... –0.5V to +2.5V
VDD_IN ..... –0.5V to +2.5V
VDD_OUT ..... –0.5V to +2.5V
Output Current ..... –50mA to +50mA
ESD Protection (HBM) 2000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics

V_{DD_IN} = 1.2V ± 0.1V, V_{DD_OUT} = 1.8V ± 0.1V, T_A = –40° to 105°C

Parameters	Description	Test Conditions(1)		Min.	Typ.(2)	Max.	Units
V_{DD_IN}	Input Supply Voltage			0.9	1.2	1.98	V
V_{DD_OUT}	Output Supply Voltage			1.1	1.8	1.98	V
V_{IH}	Input High Voltage for IN0/IN1	Logic HIGH level		0.8 x V_{DD_IN}			V
V_{IL}	Input Low Voltage for IN0/IN1	Logic LOW level				0.2 x V_{DD_IN}	V
V_{IH}	Input High for OE and CLK_SEL	Logic HIGH level		0.9			V
V_{IL}	Input Low for OE and CLK_SEL	Logic LOW level				0.25	V
I_{DD_IN}	Input Current	Both input and output clocks are toggling. 5pF load termination. f_0 = 24MHz.				200	µA
I_{DD_OUT}	Output Current	Both input and output clocks are toggling. 5pF load termination.	f_0 = 12MHz			6	mA
			f_0 = 24MHz			10	mA
			f_0 = 48MHz			20	mA
			f_0 = 125MHz			45	mA
I_{IH}	Input Current High for IN0/IN1					+5	uA
I_{IL}	Input Current Low for IN0/IN1			-5			uA

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Input Current High(I_{IH})/Low(I_{IL}) for OE/SEL Pin

		OE/SEL = VDD_IN	OE/SEL = GND
VDD_IN	**VDD_OUT**	**I_{IH} (uA)**	**I_{IL} (uA)**
0.9	1.98	21.6	7.1
0.9	1.8	14.2	5.6
0.9	1.5	3.5	3.3
0.9	1.2	0.1	1.4
0.9	0.9	0	0.3
1.2	1.98	9.9	7.1
1.2	1.8	3.6	5.6
1.2	1.5	0.1	3.3
1.2	1.2	0	1.4
1.8	1.98	0.1	7.1
1.8	1.8	0	5.6
1.8	1.5	0	3.3
1.8	1.2	0	1.4

Notes
1. OE/SEL pins are pull high to VDD_OUT when floating or Input = hiZ.
2. OE/SEL Vth = 0.72V when VDD_OUT = 1.98V at typical case.
3. OE/SEL Vth = 0.47V when VDD_OUT = 1.08V at typical case.

Parameters	Description	Test Conditions(1)	Min.	Typ.(2)	Max.	Units
V_{OH}	Output High Voltage	Low VDD_IN to High VDD_OUT				
		$V_I = V_{IH}$, I_{OH} = -100µA, V_{DD_OUT} = 1.62V-1.98V	V_{DD_OUT} -0.1			V
		$V_I = V_{IH}$, I_{OH} = -8mA, V_{DD_OUT} = 1.62V	1.2			V
		High VDD_IN to Low VDD_OUT				
		$V_I = V_{IH}$, I_{OH} = -100µA, V_{DD_OUT} = 1.08V-1.2V	V_{DD_OUT} -0.1			V
		$V_I = V_{IH}$, I_{OH} = -4mA, V_{DD_OUT} = 1.08V	0.75			V
V_{OL}	Output LOW Voltage	Low VDD_IN to High VDD_OUT				
		$V_I = V_{IL}$, I_{OL} = 100µA, V_{DD_OUT} = 1.62V-1.98V			0.1	V
		$V_I = V_{IL}$, I_{OL} = 8mA, V_{DD_VOUT} = 1.62V			0.45	V
		High VDD_IN to Low VDD_OUT				
		$V_I = VI_L$, I_{OL} = 100µA, V_{DD_OUT} = 1.08V-1.2V			0.1	V
		$V_I = V_{IL}$, I_{OL} = 4mA, V_{DD_VOUT} = 1.08V			0.25	V

Notes:

1. For Max. or Min. conditions, use appropriate operating range values.

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AC Characteristics

V_{DD_IN} = 1.2V ± 0.1V, V_{DD_OUT} = 1.8V ± 0.1V, T_A = –40° to 105°C

Parameters	Description	Test Conditions[1]	Min.	Typ	Max.	Units
F_{IN}	Input Frequency		DC		200	MHz
$t_{R/tF}$	CLKn Rise/Fall Time	20% to 80%		2		ns
t_{PD}	Propagation Delay	C_L = 5pF, 125MHz Outputs are measured @ Vdd/2			2	ns
t_{dc_in}	Duty Cycle In @ 1ns edge rate		45		55	%
t_{dc_out}	Duty Cycle Out		40		60	%
$T_{startup}$	Time after power supply exceeds 0.5V before applying input clock, to ensure glitch free output.				225	us
R_{out}	Output Impedance			34		Ω
Add_Jitter RMS	12kHz to 20MHz additive RMS random jitter.	f_0 = 24MHz, input slew rate ≥ 0.2V/ns, V_{IH}-V_{IL} ≥ 850mVpp		0.09	0.2	ps

Notes:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grad

Capacitance

T_A = 25°C, f = 1MHz

Parameters[1]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0	2.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	2.5		

Note:

1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
I_{DDQ}	Quiescent Power Supply Current	VDD_IN = 1.2V, VDD_OUT = 1.8V	IN0/IN1 = GND, OE/CLK_SEL = floating			20	µA
		VDD_IN = 1.8V, VDD_OUT = 1.2V				10	µA
I_{DD_TOT}	Total Power Supply Current	V_{DD_OUT} = 1.8V	All Outputs Toggling, C_L = 5pF, F_{IN} = 125MHz			45	mA
		V_{DD_OUT} = 1.5V				35	
		V_{DD_OUT} = 1.2V				25	

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 1.2V or 1.5V, and +25°C ambient.

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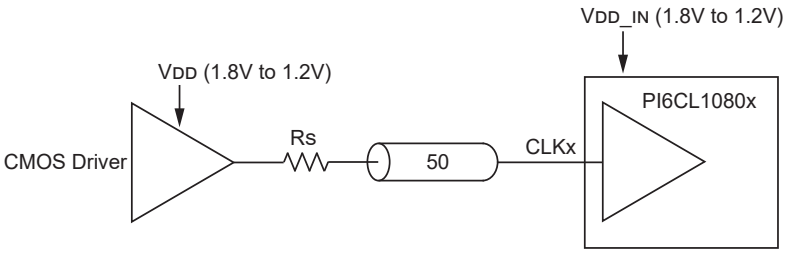

Note: Value for Rs should be chosen so that the total source impedance matches the characteristic impedance of the PCB trace.

Figure 1. Input Clock Termination

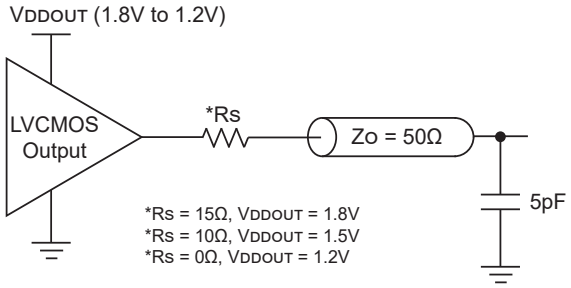

Figure 2. Product Test Diagram

Table 1. Input Clock Mux Logic

CLK_SEL	CLK0	CLK1	Q
L	L	x	L
L	H	x	H
H	x	L	L
H	x	H	H

Typical Application

Figure below shows an example of PI6CL10806/PI6CL10808 being used in a clock level translation application.

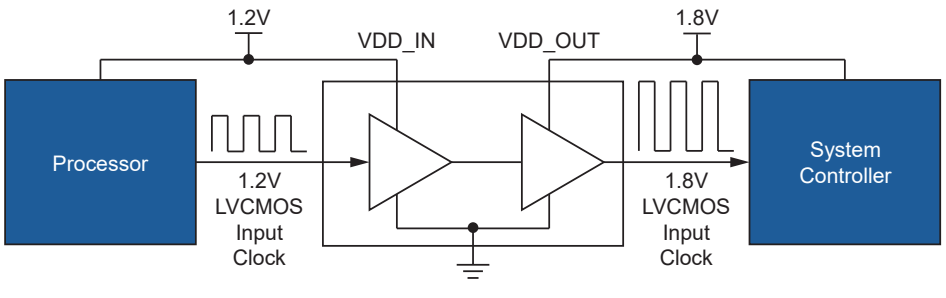

Figure 3. Processor Clock Level Translation Application

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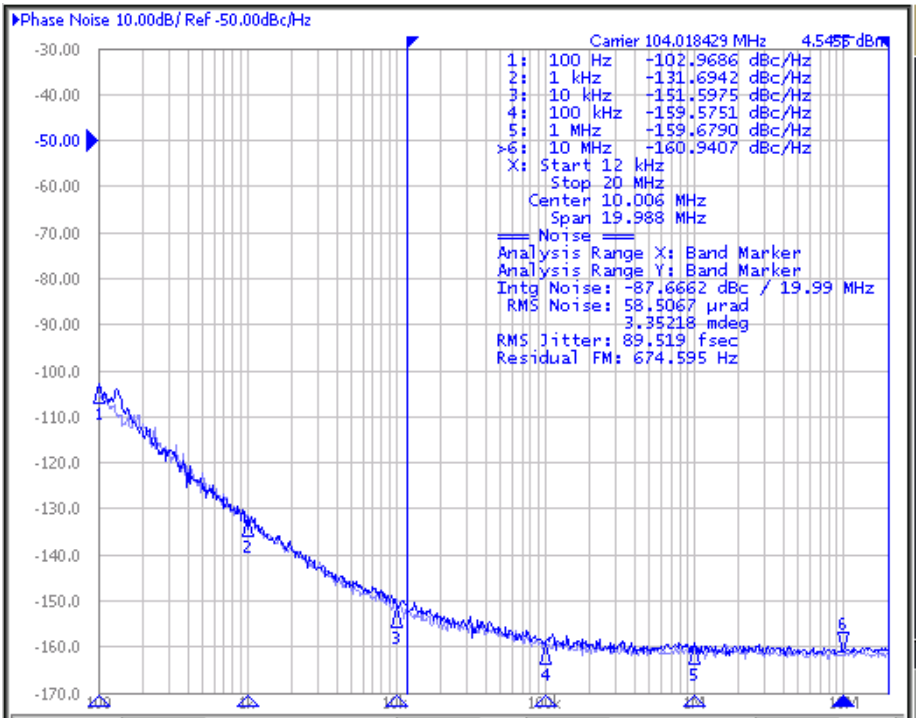
Phase Noise



Switching Waveforms

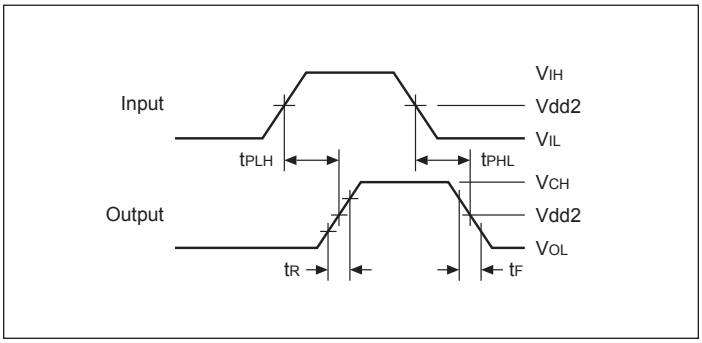


Figure 4. Propagation Delay

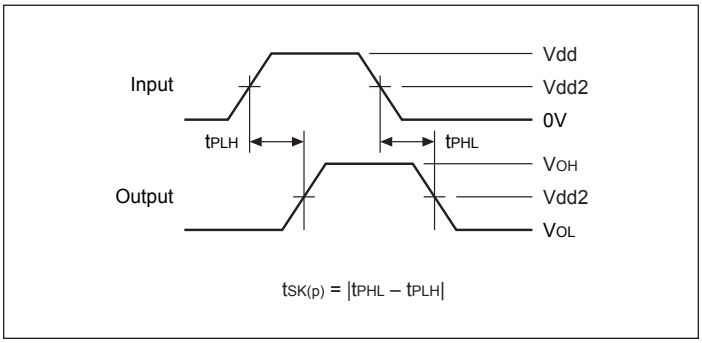


Figure 5. Pulse Skew – $t_{SK(P)}$

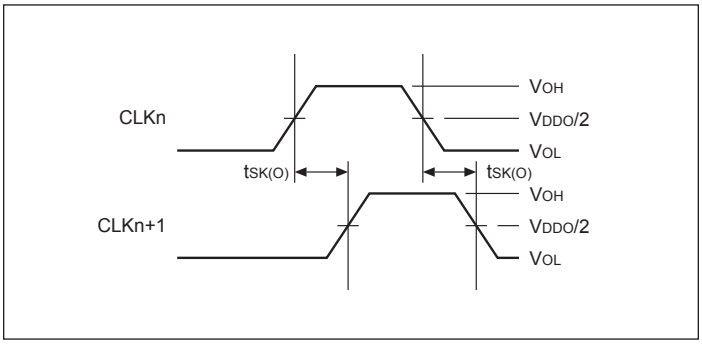


Figure 6. Output Skew – $t_{SK(O)}$

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Part Marking

PI6CL10806/ZH Package



Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code

PI6CL10808/ZH Package



Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code

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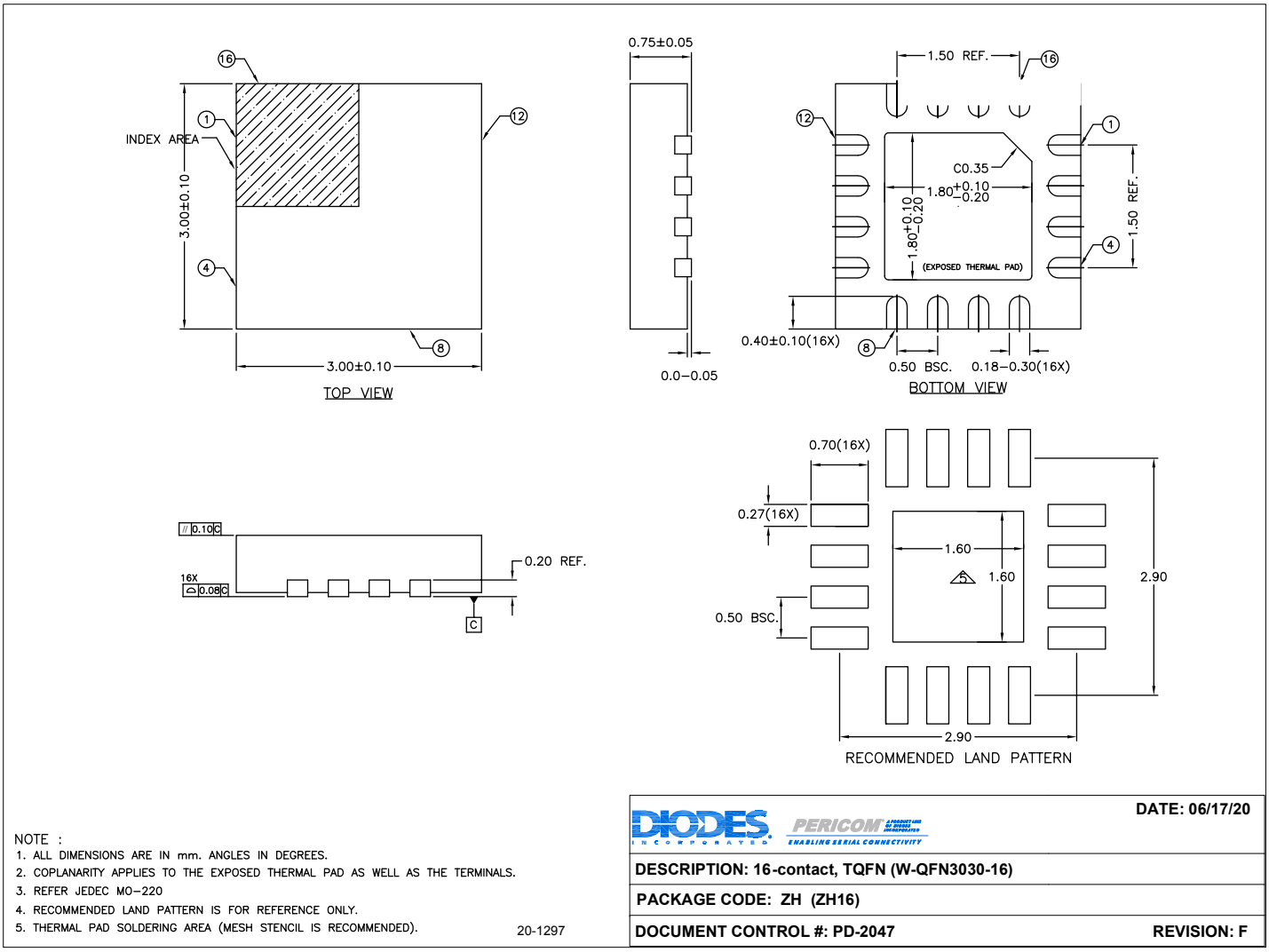
Packaging Mechanical

16-TQFN (ZH)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL IS RECOMMENDED).

20-1297

	DATE: 06/17/20
DESCRIPTION: 16-contact, TQFN (W-QFN3030-16)	
PACKAGE CODE: ZH (ZH16)	
DOCUMENT CONTROL #: PD-2047	REVISION: F

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Sn Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.036 grams (PI6CL10806ZHEX)
  0.035 grams (PI6CL10808ZHEX)

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Ordering Information

Orderable Part Number	Package Code	Package Description	Temperature
PI6CL10806ZHEX	ZH	16-Contact, TQFN (W-QFN3030-16)	–40°C to 105°C
PI6CL10808ZHEX	ZH	16-Contact, TQFN (W-QFN3030-16)	–40°C to 105°C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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