DRAM Development

① HBM Digital Design (RTL Design)
② HBM Digital Design (SoC Design)
③ HBM Digital Design (Verification)
④ HBM Digital Design (Front-end)
⑤ HBM Digital Design (Back-end)
⑥ HBM Digital Design (Strategy)
⑦ Circuit Design (HBM)



Beyond Boundaries
Toward Innovation

HBM Digital Design (RTL Design)

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About Us

Our team is a key organization responsible for HBM Base Die Digital Design. We enhance HBM performance and technical competitiveness through ultra-high-speed interface design and low-power, high-reliability logic design, and realize next-generation memory technologies.

What We Do

- Communicating with customers to translate their requirements into detailed specifications
- Defining the architecture and IP functions through PPA evaluations
- Performing RTL design and verification, logical integration, and physical design guide preparation
- Working with relevant teams to define the floorplan and wafer test flow, oversee physical implementation, and perform silicon verification and issue analysis

What We Need to See

- Strong expertise in engineering fields such as Semiconductor, Electrical/Electronic Engineering, or Physics, with 5+ years of relevant experience
- Designing and verifying RTL with Verilog/SystemVerilog
- Analyzing requirements to define IP structure and functions, and leading design and debugging
- Understanding clock, reset, and timing constraints and applying them to design
- Analyzing Lint, CDC/RDC, STA, and EQ results and resolving design issues
- Documenting design intent and verification results, and communicating with customers and relevant teams

Ways to Stand Out

- Experience in DRAM controller or DRAM DFT/DFD design and analysis
- Experience in leading digital design covering interface/memory PHYs and analog IPs
- Experience in PHY/TSV bit macro, TSV PHY hard macro, and 3D PHY design
- Experience in analog IP integration, full-custom co-design, or full-chip integration
- Experience in LLM/AI-based design and verification automation, with accuracy and productivity evaluation
- Experience in PPA-based architecture optimization, customer spec alignment, and technical leadership
- Experience in wafer test flow definition, silicon verification, and failure analysis

HBM Digital Design (SoC Design)

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About Us

Our team is responsible for researching SK hynix's Custom HBM (CHBM) Base-Die Architecture and driving full-chip design based on it. CHBM integrates key IPs, including the Host IP, chiplet interface IPs, DRAM controller/PHY IPs, and a wide range of logic and analog IPs.

What We Do

- Developing digital logic IP/SoC designs based on hardware description languages (Verilog, VHDL)
- Full-chip design based on in-house & 3rd-party IPs and subsystems
- Subsystem and full-chip design considering physical design aspects (Package – bump, probe-pad, etc., Synthesis)
- Integrating and verifying chiplet interface PHY/Link/Protocol IPs (e.g., UCIe, OpenHBI, BoW)
- Integrating and verifying off-chip interface PHY/Link/Transaction IPs (e.g., PCIe, CXL, USB, MIPI)
- In-chip and inter-chiplet DFT architecture/design, RTL-level DFT logic insertion, and DFT flow development (e.g., IEEE 1687 ICL/PDL, IEEE 1838-based DFT architecture)
- Establishing 3DIC SoC design flows and designing related IPs and logic
- Integrating and verifying DRAM controller/PHY IPs (LPDDR, DDR, GDDR, HBM)
- Analyzing RAS requirements and defining policies, and developing and verifying hardware IPs or firmware
- Developing test firmware (e.g., ARM, RISC-V) to operate and verify full chips, subsystems, and IPs
- Subsystem and full-chip architecture (Power/Debug/Security/DFT)

HBM Digital Design (SoC Design)

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What We Need to See

- Strong expertise in engineering fields such as Semiconductor, Electrical/Electronic Engineering, Physics, or Mechanical Engineering
- 5+ years of experience, with one or more of the following capabilities:

1) Performance, Power & Area (PPA) estimation and synthesis for IP/Subsystem/Full-chip
2) Off-chip/chiplet interface PHY/Link layer design, or IP integration and verification/evaluation
3) Media controller (NAND, DRAM) design, or IP integration and verification/evaluation
4) Establishing on-chip and inter-chiplet DFT architecture and design/insertion flows based on IEEE 1687, IEEE 1838 and IEEE 1500
5) Logic and physical design for 3DIC SoCs
6) Implementing security scenarios (Secure Boot, TrustZone, Attack Detect) to protect SoCs from hacking
7) Establishing memory and system-level RAS policies and designing/verifying/evaluating them
8) System-level clock/reset and power control logic design and evaluation
9) Designing and operating P/V/T sensor-based monitoring systems in SoCs
10) Designing on-chip interconnects (e.g., AMBA bus, NoC) based on full-chip requirements and IP/subsystem specifications
11) Subsystem and full-chip architecture design

HBM Digital Design (Verification)

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About Us

We are responsible for verifying mixed-signal IPs, digital IPs, and subsystem/top-level designs to secure SK hynix's unrivaled competitive edge in HBM. With design integrity as our goal, we drive end-to-end design verification across the HBM product development process—building the verification systems and environments, and developing verification models.

What We Do

HBM Digital Design Verification

1) Verifying in-house and 3rd-party digital IPs and mixed-signal designs within HBM
2) Developing in-house VIPs and integrating and utilizing 3rd-party VIPs
3) Developing UVM-based verification environments and test cases
4) Achieving code/functional coverage closure through regression testing

What We Need to See

Strong expertise in engineering fields such as Semiconductor, Electrical/Electronic Engineering, or Computer Engineering, with 4+ years of experience in the semiconductor industry (Master's/Ph.D. study periods counted as experience), plus the following capabilities:

1) SystemVerilog/UVM VIP, testbench, and test case development
2) Verification planning based on digital IP specifications, and understanding of verification processes
3) Design and implementation of UVM agents for new protocols or custom IPs
4) Code/functional coverage closure

Ways to Stand Out

1) End-to-end (A-to-Z) development of custom UVM agents based on specifications
2) HBM and DDR/LPDDR memory verification
3) Full-chip mixed-level design (schematic & RTL) verification

HBM Digital Design (Front-end)

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About Us

Our team is responsible for SK hynix's HBM Digital Implementation. We oversee digital front-end and back-end design using the latest process technologies and EDA tools, and build efficient development processes to secure next-generation HBM competitiveness.

What We Do

【 Digital Implementation (Front-end) 】

We are responsible for the entire implementation flow for digital blocks, covering DFT architecture, synthesis, and STA. We develop interface IPs, such as PCIe and UCIe, based on the HPDF architecture, and implement various types of digital designs. Leveraging advanced process technologies and the latest EDA tools, we develop competitive, customer-tailored HBM solutions optimized for PPAT (Performance, Power, Area, TAT).

What We Need to See

- Strong expertise in engineering fields such as Semiconductor or Electrical/Electronic Engineering
- 3+ years of experience, with one or more of the following capabilities:
  1) Implementation experience with PPAT improvement on sub-5nm processes
  2) Experience in HPDF design top and block implementation flow
  3) Experience with EDA tools required for implementation, including synthesis, STA, and DFT
  4) Experience in DFT implementation and verification (e.g., MBIST, Tessent SSH/SSN, TestMAX)
  5) Experience in design analysis and environment improvement using AI and Tcl/Python scripts

Ways to Stand Out

- Experience with TSMC 3nm project implementation
- Experience in HPDF top project management
- Experience with Tessent SSH/SSN-based DFT implementation and verification
- Experience with HBM IP (HBM PHY, TSV PHY, 3D PHY) projects
- Experience in interfacing and collaborating with global customers

HBM Digital Design (Back-end)

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About Us

Our team is responsible for SK hynix's HBM Digital Implementation. We oversee digital front-end and back-end design using the latest process technologies and EDA tools, and build efficient development processes to secure next-generation HBM competitiveness.

What We Do

【 Digital Implementation (Back-end) 】

We manage Digital Auto Place & Route (P&R) for digital blocks in HBM logic die. We perform various forms of digital implementation across our HBM product portfolio, covering both standard and custom HBM. Based on customer requirements, we implement interface IPs, such as PCIe, UCIe, and CXL. We also handle the DTCO domain, driving process improvement and optimization, as well as early-stage research on advanced process technologies, to develop competitive, customer-tailored HBM solutions optimized for PPAT (Performance, Power, Area, TAT).

What We Need to See

- Strong expertise in engineering fields such as Semiconductor or Electrical/Electronic Engineering
- 3+ years of experience, with one or more of the following capabilities:
  1) HPDF (Tiled) top design or project management
  2) Top bus/async bridge implementation
  3) 2GHz or higher high-speed digital design development
  4) LLM/Agent-based EDA flow automation and operation
  5) Design Technology Co-Optimization (DTCO)
  6) Design analysis and environment improvement using Tcl/Python scripts
  7) Application of the latest FE/BE/PDN/DFT technologies and operation of related environments using AI and EDA tools

Ways to Stand Out

- Experience with HBM IP (HBM PHY, TSV PHY, 3D PHY) projects
- Experience with sub-3nm nanosheet technology development
- Experience with CPU/GPU/NPU implementation
- Experience in interfacing and collaborating with global customers

HBM Digital Design (Strategy)

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About Us

Our team is responsible for providing design direction for SK hynix's Custom HBM product development through technical discussions with customers. We work closely with customers to determine design specifications for Custom HBM products and provide the necessary information at the appropriate design phases.

What We Do

We define the HBM Base Die architecture, translate global customers' requirements into design specifications, and lead the entire product development process from a technical perspective. Key responsibilities include:

1) Establishing Custom HBM architecture and defining design spec items
2) Conducting technical discussions with Custom HBM customers
3) Managing design milestones, driving technical decisions, and coordinating internal alignment

What We Need to See

- Strong expertise in engineering fields such as Semiconductor, Electrical/Electronic Engineering, or Physics
- 5+ years of experience, with one or more of the following capabilities:

1) Overall understanding of HBM development and specifications
2) Base die or core die design experience within the HBM design process
3) Full-custom and semi-custom design experience

Ways to Stand Out

1) HBM Base Die architecture design experience, along with PDN (Power Delivery Network) analysis and SI/PI (Signal/Power Integrity) experience
2) Experience in managing schedules and resources with a solid understanding of key design milestones, ensuring design quality within target deadlines
3) Business English proficiency: the ability to discuss professional topics with US engineering teams and clearly convey our company's position, both verbally and in writing

Circuit Design (HBM)

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About Us

As a key organization driving SK hynix's HBM competitiveness, our team is responsible for designing and analyzing HBM products and delivering them on time to maximize customer value. Partnering with the world's top AI customers, we lead HBM technology innovation through cutting-edge circuit design expertise and rigorous analysis, building global No. 1 competitiveness.

What We Do

- Designing circuits that meet internal and external specification requirements for DRAM/HBM products
- Improving design quality and enhancing yield for mass production during DRAM/HBM product development
- Analyzing characteristics at the wafer, KGSD (Known Good Stack Die), and package assembly stages, and verifying compliance with product specifications
- Enhancing performance and ensuring stable operation throughout product development and in customer systems to deliver customer satisfaction

What We Need to See

- Strong expertise in engineering fields such as Semiconductor, Electrical/Electronic Engineering, Physics, or Computer Engineering

- 4+ years of relevant experience (Master's/Ph.D. study periods counted as experience), with one or more of the following capabilities:

1) DRAM or HBM architecture review and design experience

2) Full-custom and digital co-design experience, with PDN analysis

3) Full-custom logic design experience on foundry processes

4) Experience with various tools and equipment for DRAM/HBM product failure analysis

Ways to Stand Out

- Extensive experience in DRAM/HBM product development and analysis
- Experience in HBM-mounted system analysis
- Proficiency in Python, Spotfire, Verilog, and circuit simulators (e.g., Hspice, Csim, PrimeSim, Spectre)

Solution Development

① SoC Design
② High-Speed Interface
③ Digital IP Design(RTL)
④ SoC Design Verification
⑤ SoC Silicon Validation
⑥ Logical Implementation
⑦ AI Research



Beyond Boundaries
Toward Innovation

SoC Design

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About Us

Our team designs controllers installed in NAND Solution products. We perform the end-to-end process from IP design to SoC integration, and optimize HW-SW interaction through close collaboration with the Firmware team. We also implement high-efficiency, low-power, high-performance controllers through RTL design considering PPA (Power, Performance, Area) and architecture research.

What We Do

We construct the overall SoC architecture by integrating diverse IPs and subsystems, performing interface definition and High-Level RTL design. Through close collaboration with cross-functional teams such as FW, Verification, PD, and DFT, we aim to achieve a successful tape-out of a PPA-optimized SoC controller.

What We Need to See

- At least 3 years of professional experience with expertise in electrical and electronic engineering, semiconductor engineering, or a related field.
- Experience in RTL design and verification using Verilog/SystemVerilog.
- Ability to analyze design specifications and define and implement microarchitecture and interfaces.

Ways to Stand Out

- Experience in designing SSD controllers, NAND Flash controllers, or storage-related SoCs.
- Experience in designing PCIe/NVMe-based host interfaces.
- Experience in designing NAND or DRAM interfaces.
- Experience in SoC design and tape-out using logic process technology.
- Experience in low-power design through clock, reset, and power domain optimization.
- Understanding of synthesis and timing.
- Experience in using AI tools to improve design and verification productivity and integrating them into workflows.
- Foreign language proficiency to collaborate with global R&D teams.
- Strong problem-solving skills and a teamwork-oriented mindset.

High-Speed Interface

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About Us

We design high-speed interfaces for next-generation mobile storage. Our team specializes in mixed-signal design for MPHY PHY, with ongoing development of MPHY 6.0 for mass production and advanced development of MPHY 7.0. System, digital, and analog engineers collaborate across the full development cycle—from architecture definition and circuit design to silicon validation—to deliver high-speed, low-power SerDes solutions using cutting-edge FinFET process technology.

What We Do

- Design high-speed SERDES circuit architecture compliant with the MPHY 7.0 specification
- Define SERDES channel architecture to support increasing data transfer rates and establish link budget EQ strategies
- Design DSP-based CDR architecture and optimize jitter/BER performance
- Perform full-custom circuit design considering FinFET process characteristics and provide layout direction
- Verify system operation including power management domains (AON/PSW) and confirm specification compliance through mixed-signal simulation

What We Need to See

- Hands-on experience in SERDES circuit design and circuit design using FinFET process technology.
- Expertise in one or more of the following areas: SERDES architecture, DSP-based clock and data recovery (CDR), or FinFET circuit design.
- Ability to collaborate effectively based on an understanding of analog circuits and SERDES operation.
- A master’s or doctoral degree in a related field, or equivalent professional experience.

Ways to Stand Out

- Experience developing standard high-speed interface specifications such as MIPI MPHY, PCIe, and USB
- Experience in equalization (CTLE, DFE, FFE) and channel compensation circuit design
- Experience in jitter and Signal Integrity analysis, as well as measurement and debugging
- Experience in mass-production chip development and silicon evaluation
- Experience in multi-power domain and ULP (Ultra-Low Power) design

Digital IP Design(RTL)

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About Us

As a leading research organization of SK hynix, we are pioneering the research and development of High Speed Interface IPs required for a wide range of products, including Chiplet, Mobile, and SSD. We develop key IPs such as Chiplet D2D IP, UFS MIPI IP, TSV PHY, and NAND PHY, as well as platforms to test these various IPs. Join us in our journey as we aim for innovative technology development.

What We Do

You will be responsible for HBF TSV PHY circuit design, verification, and implementation. Your primary responsibility will be digital TSV PHY RTL design, including low-power design with power, performance, and area (PPA) considerations. The role also involves collaborating with simulation/FPGA verification and implementation teams, drawing on an understanding of the RTL-to-GDS SoC development flow, as well as analyzing issues identified during silicon chip validation.

What We Need to See

Expertise in a relevant technical field, such as semiconductors, electronics, electrical engineering, computer engineering, physics, or mechanical engineering.

Proficiency in at least one of the following areas:

1) Digital circuit design for high-speed SERDES interfaces.

2) Design and verification of chiplet IP (e.g., UCIe).

3) Design and verification of memory interface PHYs for NAND, DRAM, or similar memory technologies.

Ways to Stand Out

1) Experience in IP design, including memory PHYs and digital IP.

2) Experience in developing or verifying chiplet interfaces, or integrating third-party IP into designs.

3) Experience in developing and leading SoC platform projects involving ARM cores, AMBA buses, and related technologies.

4) Experience in digital circuit design and front-end implementation.

5) Proficiency in using AI tools and strong English language skills are preferred.

SoC Design Verification

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About Us

Our team specializes in R&D on next-generation SoCs for future industries such as AI, autonomous driving, and hyperconnectivity. Leveraging world-class verification methodologies and automation environments, we create semiconductor solutions with maximized performance and power efficiency. We are looking for passionate talent to push the boundaries of technology together with us.

What We Do

You will play a key role in ensuring the functional accuracy and reliability of SoCs.

- Verification Environment Setup: Design and implement reusable verification environments (testbenches) based on SystemVerilog and UVM.
- Test Strategy Development: Analyze specifications to establish verification plans and develop test scenarios for coverage achievement.
- Simulation and Debugging: Proactively identify bugs through simulation and collaborate with design teams to resolve issues.
- Verification Convergence (Sign-off): Analyze functional and code coverage to meet verification completion criteria and proceed with final sign-off.
- Process Enhancement: Improve overall development productivity by developing verification automation scripts and introducing new methodologies.

What We Need to See

- Expertise in Electrical/Electronic/Semiconductor Engineering or related fields
- 3+ years of hands-on experience in SoC verification
- Problem-solving mindset and strong emphasis on teamwork

Ways to Stand Out

Preferred: AI competency and English proficiency

SoC Silicon Validation

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About Our Organization

We validate controllers in DRAM/NAND solutions and ensure that each IP operates as designed. We develop and evaluate firmware and test cases for FPGA, Emulator, and ASIC environments.

Responsibilities

Perform Unit-, Subsystem-, and End-to-End (E2E)-level validation of Host Interfaces (PCIe), Media Interfaces (DRAM/NAND), and other controller IPs.

Who We're Looking For

- Background in Semiconductor, Electrical/Electronic, or Computer Engineering
- One or more of the following skills:

1. PCIe understanding and validation experience
2. DRAM/NAND understanding and validation experience
3. Proficiency in C, C++, or Python
4. Knowledge of ARM processors, Assembly, Compilers, Linkers, and Loaders
5. Solution FW development and TRACE32 debugging skills
6. PCB experience and schematic analysis skills

Preferred Experience

1. PCIe/NAND interface design and validation experience
2. ARM-based Embedded FW development and TRACE32 debugging experience

Logical Implementation

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About Us

Our team handles the full ASIC design flow—from full-chip design through implementation and sign-off—for a range of SoCs, including SSD and UFS chips, as well as HBF. We integrate various analog and digital IP blocks into SoCs, including PCIe and DDR PHYs/controllers and NAND PHYs, and are responsible for digital physical design, design for test (DFT), IR drop analysis, and bump design and verification.

Throughout this process, we work closely with cross-functional teams responsible for RTL design, analog and digital IP development, and testing to enhance the overall design quality and robustness of our SoCs.

What We Do

We carry out a broad range of SoC implementation tasks based on the ASIC flow, including top-level implementation, block-level timing sign-off, physical design, PV, and tape-out. These tasks encompass synthesis, static timing analysis, logic equivalence checking (LEC), floorplanning, P&R, DFT(BIST/SCAN), IR drop optimization, and bump-related work.

As needed, we also harden third-party IP and develop hard macros for internally developed IP. These responsibilities require effective communication and collaboration with FE, BE, DFT, and power teams, as well as design, IP, and other relevant departments.

What We Need to See

Candidates should have specialized knowledge in semiconductor, electronics, electrical engineering, or a related engineering discipline, along with at least four years of implementation experience.

1) Experience with TSMC process nodes ranging from 12 nm to 3 nm or below, and with HPDF at the top or block level.

2) Proficiency in scripting languages such as shell, Tcl, Python, and Perl.

Ways to Stand Out

1) Experience in SoC chip top-level implementation (HPDF or flat design) and block-level implementation.

2) Experience in floorplanning, placement and routing (P&R), verification, and optimization, as well as IR drop analysis and mitigation.

3) Experience in hardening high-speed interface (HSI) IP, such as DDR PHY, PCIe PHY, NAND PHY, and M-PHY.

4) Understanding of DFT (BIST/scan) and experience with DFT implementation flows.

AI Research

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About Us

We analyze AI and LLM workloads to define the performance requirements and value proposition of next-generation memory. Drawing on the principles of training, fine-tuning, and inference, we implement and evaluate models and optimization techniques. Through system-level experiments, we analyze memory bottlenecks and system limitations and assess the impact of memory characteristics.

What We Do

We leverage our domain expertise in AI and LLMs to analyze the memory requirements of representative workloads and conduct research to quantitatively validate the value of next-generation memory.

- **Defining and analyzing AI workloads:** We select key scenarios—such as LLM training, fine-tuning, and inference, long-context processing, and multi-model/multi-agent systems—and analyze memory demand and data movement characteristics.
- **Analyzing the link between AI optimizations and memory requirements:** We compare memory usage, data movement, and performance before and after applying optimizations such as PEFT and quantization, and identify remaining bottlenecks and memory requirements while accounting for model quality and service requirements.
- **Validating next-generation memory impact:** We use real-system experiments, workload traces, and simulations to evaluate how changes in memory capacity, bandwidth, and latency affect inference throughput, time to first token (TTFT), time per output token (TPOT), and service-level objective (SLO) attainment rates.

What We Need to See

- Candidates with expertise and research and development capabilities in computer science, artificial intelligence, electrical and electronic engineering, or a related field
- Candidates who understand LLM training, fine-tuning, and inference architectures and can analyze model behavior in terms of computational cost, memory usage, and data movement
- Candidates with extensive research and development experience in one or more of the following: memory-efficient training, PEFT, LLM inference optimization, or AI system performance analysis

Ways to Stand Out

- Candidates with research and development experience in one or more of the following: memory-efficient training, PEFT, LLM inference optimization, or AI system performance analysis
- Candidates with experience in prefix caching, KV cache management, reuse, and offloading, and inference optimization across multiple agents sharing a common prefix